



# Product Specification

512MB 64MX72 ECC SDRAM PC100/PC133 DIMM

Revision: 1.2

## General Information

VL374S6553-GLS

### 512MB 64Mx72 ECC SDRAM PC100/PC133 DIMM

**Description:** The VL 374S6553 is a 64M x 72 Synchronous Dynamic RAM high density memory module. This memory module consists of eighteen CMOS 32Mx8 bits with 4 banks Synchronous DRAMs in TSOP-II 400mil packages and a 2K EEPROM in 8-pin TSSOP package. This module is a 168-pin Dual In-line Memory Module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

#### Features:

- Unbuffered 8 byte SDRAM 168pin DIMM
- High Speed - 100MHz CL3
- Burst Mode Operation
- Auto & Self refresh Capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V  $\pm 0.3$  V power supply
- 13/10/2 Addressing (Row/Column/Bank)
- MRS cycle with address key programs
- EPROM Serial presence Detect
- Gold (Au) contacts
- Lead-free/RoHS compliant
- PCB height: **1158 (mil)**, single sided component

#### Pin Names:

Pin Name	Function
A0-A12	Address Input
BA0,BA1	Select Bank
DQ0-DQ63	Data Input/output
CB0-CB7	Check bits for ECC
CLK0-CLK3	Clock Input
CKE0-CKE1	Clock Enable Input
/CS0-/CS3	Chip Select Input
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DQM0-7	DQM
V <sub>DD</sub>	Power supply (3.3V)
V <sub>SS</sub>	Ground
NC	No connection
DU	Don't Use

#### Ordering Information:

VL374S6553-GLS      64MX72 100MHz @ CL3

Add brand option suffix to the Virtium Part Number:

**S = Samsung**



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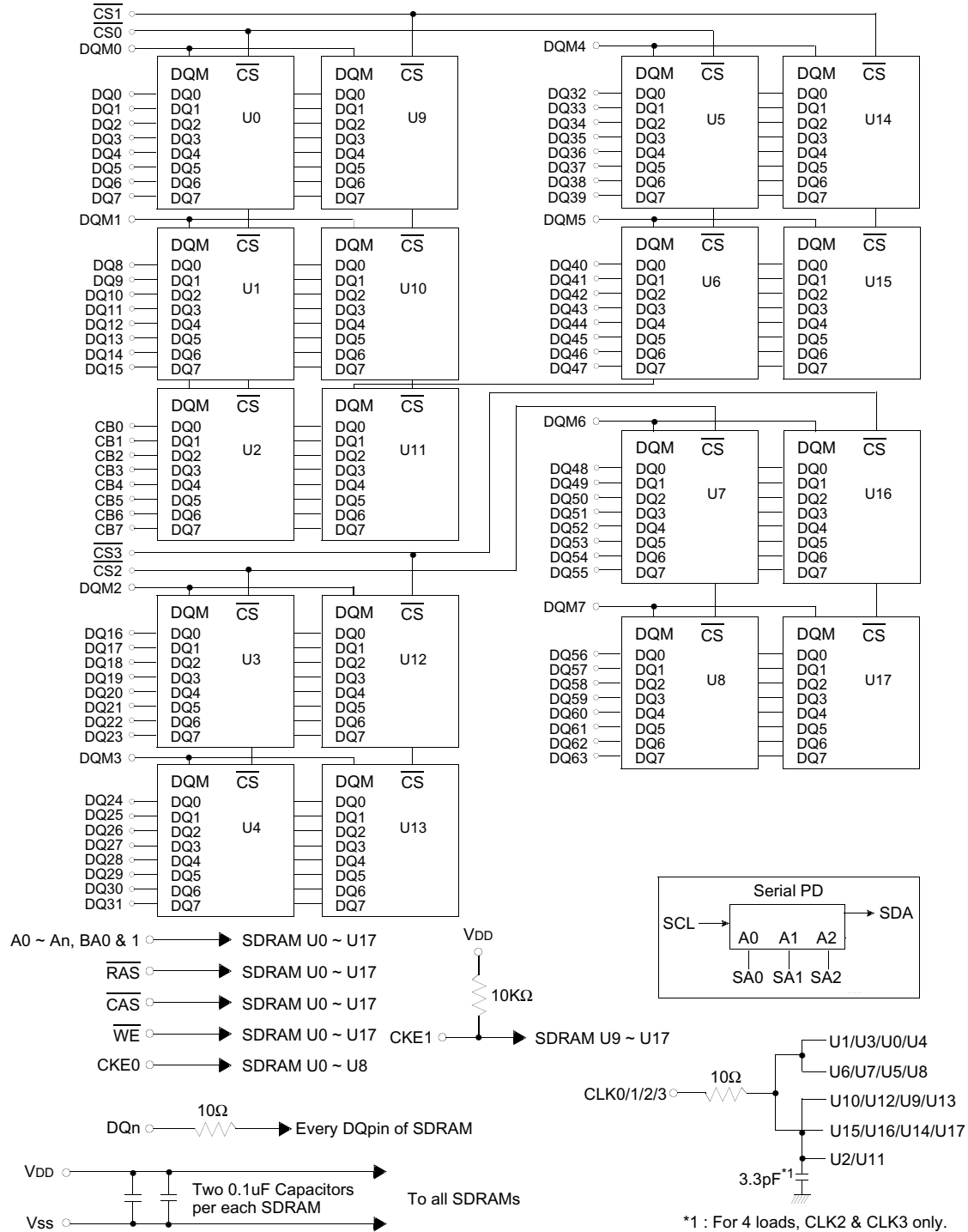
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## Pin Configuration

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Pin Number	Front Side	Pin Number	Front Side	Pin Number	Back Side	Pin Number	Back Side
1	V <sub>SS</sub>	43	V <sub>SS</sub>	85	V <sub>SS</sub>	127	V <sub>SS</sub>
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	/CS2	87	DQ33	129	/CS3
4	DQ2	46	DQM2	88	DQ34	130	DQM6
5	DQ3	47	DQM3	89	DQ35	131	DQM7
6	V <sub>DD</sub>	48	DU	90	V <sub>DD</sub>	132	NC
7	DQ4	49	V <sub>DD</sub>	91	DQ36	133	V <sub>DD</sub>
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V <sub>SS</sub>	54	V <sub>SS</sub>	96	V <sub>SS</sub>	138	V <sub>SS</sub>
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V <sub>DD</sub>	101	DQ45	143	V <sub>DD</sub>
18	V <sub>DD</sub>	60	DQ20	102	V <sub>DD</sub>	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	V <sub>SS</sub>	106	CB5	148	V <sub>SS</sub>
23	V <sub>SS</sub>	65	DQ21	107	V <sub>SS</sub>	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V <sub>DD</sub>	68	V <sub>SS</sub>	110	V <sub>DD</sub>	152	V <sub>SS</sub>
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQM0	70	DQ25	112	DQM4	154	DQ57
29	DQM1	71	DQ26	113	DQM5	155	DQ58
30	/CS0	72	DQ27	114	/CS1	156	DQ59
31	DU	73	V <sub>DD</sub>	115	/RAS	157	V <sub>DD</sub>
32	V <sub>SS</sub>	74	DQ28	116	V <sub>SS</sub>	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V <sub>SS</sub>	120	A7	162	V <sub>SS</sub>
37	A8	79	CLK2	121	A9	163	CLK3
38	A10/AP	80	NC	122	BA0	164	NC
39	BA1	81	N/C	123	A11	165	SA0
40	V <sub>DD</sub>	82	SDA	124	V <sub>DD</sub>	166	SA1
41	V <sub>DD</sub>	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V <sub>DD</sub>	126	A12	168	V <sub>DD</sub>

## Functional Block Diagram

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## Absolute Maximum Ratings

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Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	18	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## Recommended DC Operating Conditions (T<sub>A</sub>=0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>DD</sub> , V <sub>DDQ</sub>	3.0	3.3	3.6	V	
Input logic high voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DDQ</sub> +0.3	V	1
Input logic low voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output logic high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output logic low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input leakage current	I <sub>LI</sub>	-10	-	10	µA	3

**Notes :** 1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## Capacitance

(T<sub>A</sub>=25, f=1MHz, V<sub>DD</sub>=3.3V)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C <sub>ADD</sub>	85	105	pF
RAS, CAS, WE	C <sub>IN</sub>	85	105	pF
CKE (CKE0 ~ CKE1)	C <sub>CKE</sub>	50	65	pF
Clock (CLK0 ~ CLK3)	C <sub>CLK</sub>	40	45	pF
CS (CS0 ~ CS3)	C <sub>CS</sub>	30	40	pF
DQM (DQM0 ~ DQM7)	C <sub>DQM</sub>	25	30	pF
DQ (DQ0 ~ DQ63)	C <sub>OUT1</sub>	10	15	pF
CB (CB0 ~ CB7)	C <sub>OUT2</sub>	10	15	pF



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## DC Characteristics

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Parameter	Symbol	Test Condition	Version	Unit	Note
			-GL		
Operating current (One bank active)	I <sub>CC1</sub>	Burst length = 1 t <sub>RC</sub> ≥ t <sub>RC</sub> (min) I <sub>O</sub> = 0 mA	1170	mA	1
Precharge standby current in power-down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns	36	mA	
	I <sub>CC2PS</sub>	CKE & CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞	36		
Precharge standby current in non power-down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH</sub> (min), $\overline{CS}$ ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	360	mA	
	I <sub>CC2NS</sub>	CKE ≥ V <sub>IH</sub> (min), CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞ Input signals are stable	180		
Active standby current in power-down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns	108	mA	
	I <sub>CC3PS</sub>	CKE & CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞	108		
Active standby current in non power-down mode (One bank active)	I <sub>CC3N</sub>	CKE ≥ V <sub>IH</sub> (min), $\overline{CS}$ ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	540	mA	
	I <sub>CC3NS</sub>	CKE ≥ V <sub>IH</sub> (min), CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞ Input signals are stable	450	mA	
Operating current (Burst mode)	I <sub>CC4</sub>	I <sub>O</sub> = 0 mA Page burst 4banks Activated. t <sub>CCD</sub> = 2CLKs	1,260	mA	1
Refresh current	I <sub>CC5</sub>	t <sub>RC</sub> ≥ t <sub>RC</sub> (min)	1,980	mA	2
Self refresh current	I <sub>CC6</sub>	CKE ≤ 0.2V	54	mA	

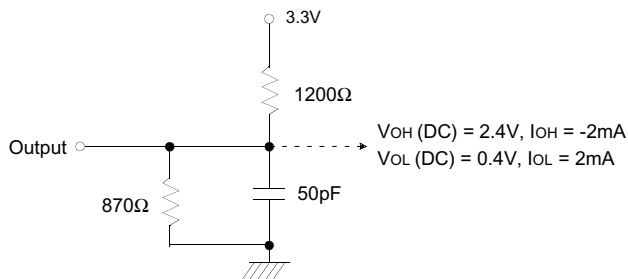
**Notes :**

1. Measured with outputs open.
2. Refresh period is 64ms.

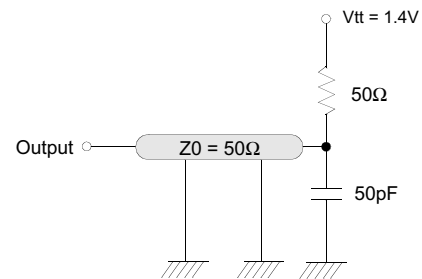
## AC Operating Test Conditions (V<sub>dd</sub>=3.3v, 0 - 70C)

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Parameter	Value	Unit
AC input levels (V <sub>ih</sub> /V <sub>il</sub> )	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

## Operating AC Parameter

Parameter	Symbol	Version				Unit	Note
		-G7	-GA	-GH	-GL		
Row active to row active delay	tRRD(min)	15	15	20	20	ns	1
RAS to CAS delay	tRCD(min)	15	20	20	20	ns	1
Row precharge time	tRP(min)	15	20	20	20	ns	1
Row active time	tRAS(min)	45	45	50	50	ns	1
	tRAS(max)	100				us	
Row cycle time	tRC(min)	60	65	70	70	ns	1
Last data in to row precharge	tRDL(min)	2				CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + tRP				-	
Last data in to new col. address delay	tCDL(min)	1				CLK	2
Last data in to burst stop	tBDL(min)	1				CLK	2
Col. address to col. address delay	tCCD(min)	1				CLK	3
Number of valid output data	CAS latency=3	2				ea	4
	CAS latency=2	1					

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  2. Minimum delay is required to complete write.
  3. All parts allow every cycle column address change.
  4. In case of row precharge interrupt, auto precharge and read burst stop.



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## Operating AC Parameters

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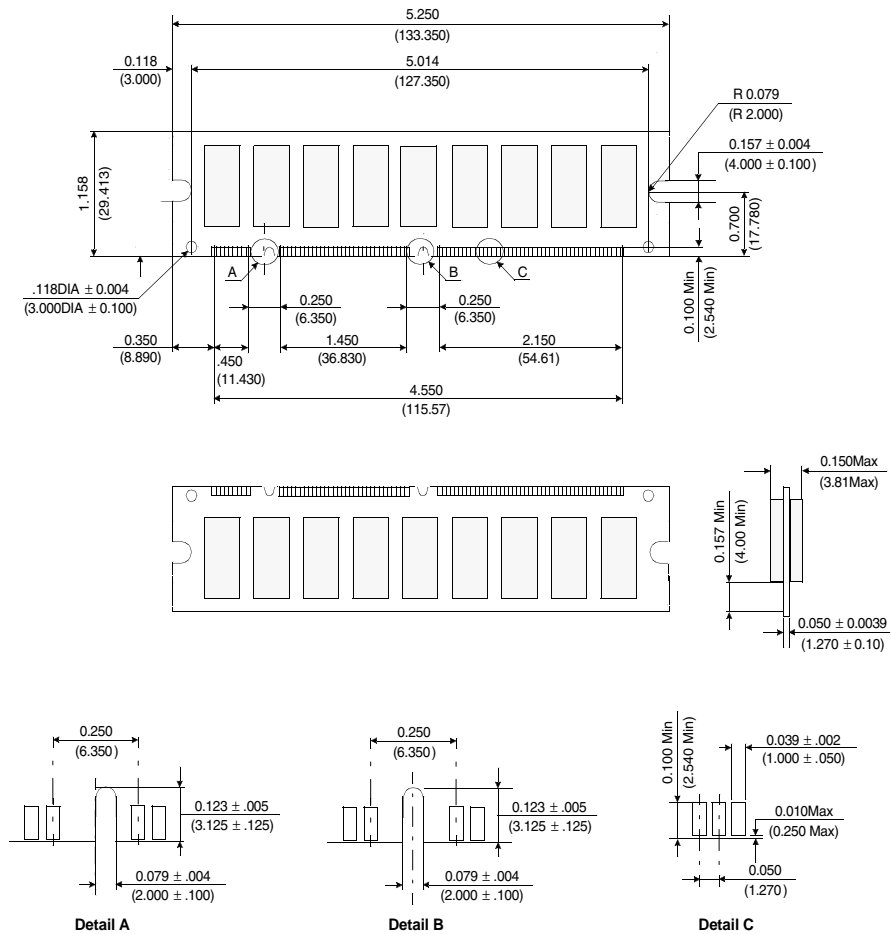
Parameter		Symbol	-G7		-GA		-GH		-GL		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	7.5	1000	10	1000	10	1000	ns	1
	CAS latency=2		7.5		10		10		12			
CLK to valid output delay	CAS latency=3	tsac		5.4		5.4		6		6	ns	1,2
	CAS latency=2			5.4		6		6		7		
Output data hold time	CAS latency=3	toH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
CLK high pulse width		tCH	2.5		2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		2.5		3		3		ns	3
Input setup time		tSS	1.5		1.5		2		2		ns	3
Input hold time		tSH	0.8		0.8		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		5.4		6		6	ns	
	CAS latency=2			5.4		6		6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
  - If clock rising time is longer than 1ns,  $(tr/2-0.5)ns$  should be added to the parameter.
  - Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, i.e.,  $[(tr + tf)/2-1]ns$  should be added to the parameter.

## Package Dimensions

**VL374S6553-GLS**

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

## Revision History:

Date	Rev.	Page	Changes
09/23/2010	1.2	All	Update datasheet