Product Specifications

PART NO: **VL466S924-GAS/GHS/GLS** | **REV: 1.4**

General Information

64MB 8Mx64 SDRAM PC100/PC133 NON-ECC UNBUFFERED SODIMM 144-PIN

Description: The VM466S924 is a 8M x 64 Synchronous Dynamic RAM high density memory module. This memory module consists of 4 CMOS 8Mx16 bits with 4 banks Synchronous DRAMs in TSOP-II 400mil packages and a 2K EEPROM in 8-pin TSSOP package. This module is a 144-pin small-outline dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

Features:

- Unbuffered 8 byte SDRAM 144pin SODIMM
- High Speed - 100MHz/133MHz CL2/CL3
- Burst Mode Operation
- Auto & Self refresh Capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ±0.3 V power supply
- 12/10/4 Addressing (Row/Column/Bank)
- MRS cycle with address key programs
- EPROM Serial Presence Detect
- Gold (Au) contacts
- Lead-free/RoHS compliant
- PCB height: **1050 (mil)**, double sided component

Pin Name	Function
A0-A11	Address inputs
BA0,BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CLK0, CLK1	Clock Input
CKE0	Clock Enable Input
CS0#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Input
WE#	Write Enable
DQM0-DQM7	Data Mask
VDD	Power Supply
VSS	Ground
SDA	Serial Data Input/Output
SCL	SPD Clock Input
NC	No Connect
* These pins are not used in this module.	

Order Information:

VL 466S924- GA S X

- DRAM DIE (Option)
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  GA: PC133 @ CL3
  GH: PC100 @ CL2
  GL: PC100 @ CL3
- VL: Lead-free/RoHS

Pin Configuration

Pin Number	Front Side
1	VSS
3	DQ0
5	DQ1
7	DQ2
9	DQ3
11	VDD
13	DQ4
15	DQ5
17	DQ6
19	DQ7
21	VSS
23	DQM0
25	DQM1
27	VDD
29	A0
31	A1
33	A2
35	VSS
37	DQ8
39	DQ9
41	DQ10
43	DQ11
45	VDD
47	DQ12
49	DQ13
51	DQ14
53	DQ15
55	VSS
57	NC
59	NC
61	CLK0
63	VDD
65	RAS#
67	WE#
69	CS0#
71	*CS1#

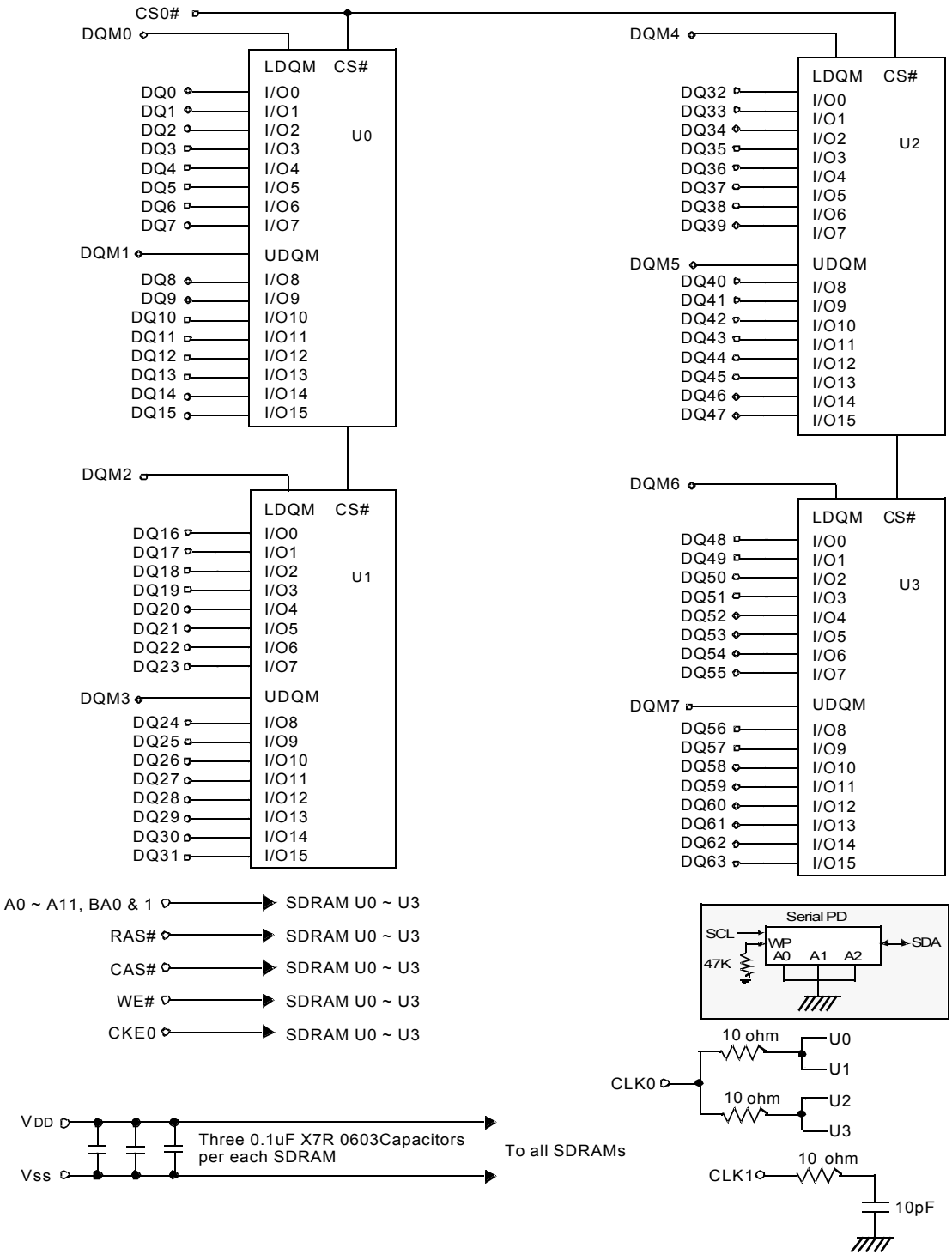
Pin Number	Back Side
2	VSS
4	DQ32
6	DQ33
8	DQ34
10	DQ35
12	VDD
14	DQ36
16	DQ37
18	DQ38
20	DQ39
22	VSS
24	DQM4
26	DQM5
28	VDD
30	A3
32	A4
34	A5
36	VSS
38	DQ40
40	DQ41
42	DQ42
44	DQ43
46	VDD
48	DQ44
50	DQ45
52	DQ46
54	DQ47
56	VSS
58	NC
60	NC
62	CKE0
64	VDD
66	CAS#
68	*CKE1
70	*A12
72	*A13

Pin Number	Front Side
73	NC
75	VSS
77	NC
79	NC
81	VDD
83	DQ16
85	DQ17
87	DQ18
89	DQ19
91	VSS
93	DQ20
95`	DQ21
97	DQ22
99	DQ23
101	VDD
103	A6
105	A8
107	VSS
109	A9
111	A10/AP
113	VDD
115	DQM2
117	DQM3
119	VSS
121	DQ24
123	DQ25
125	DQ26
127	DQ27
129	VDD
131	DQ28
133	DQ29
135	DQ30
137	DQ31
139	VSS
141	SDA
143	VDD

Pin Number	Back Side
74	CLK1
76	VSS
78	NC
80	NC
82	VDD
84	DQ48
86	DQ49
88	DQ50
90	DQ51
92	VSS
94	DQ52
96	DQ53
98	DQ54
100	DQ55
102	VDD
104	A7
106	BA0
108	VSS
110	BA1
112	A11
114	VDD
116	DQM6
118	DQM7
120	VSS
122	DQ56
124	DQ57
126	DQ58
128	DQ59
130	VDD
132	DQ60
134	DQ61
136	DQ62
138	DQ63
140	VSS
142	SCL
144	VDD

* These pins are not used in this module

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	^{0}C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions (T_A = 0^{0}C to 70^{0}C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	IoL = 2mA
Input leakage current (Inputs)	I_{IL}	-10	-	10	uA	3

Notes: 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is <= 3ns.
2. V_{IL} (min) = 2.0V AC. The undershoot voltage duration is <= 3ns.
3. Any input 0V <= V_{IN} <= V_{DDQ}.

Capacitance (T_A = 25^{0}C, f = 1MHz, V_{DD} = 3.3V)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	15	25	pF
Input capacitance (RAS#, CAS#, WE#)	C_{IN2}	15	25	pF
Input capacitance (CKE0)	C_{IN3}	15	25	pF
Input capacitance (CLK0)	C_{IN4}	15	21	pF
Input capacitance (CS0#)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	10	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	10	12	pF

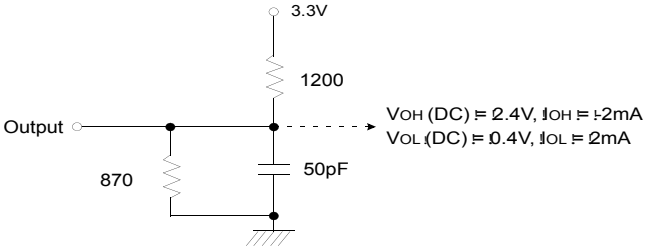
DC Characteristics (Recommended operation condition unless otherwise noted, T_A = 0°C to 70°C)

Parameter	Symbol	Test Condion	Version			Unit	Note
			-GA	-GH	-GL		
Operating current (One bank active)	I_{CC1}	Burst length = 1 t_{RC} >= t_{RC}(min) I_{OL} = 0 mA	400			mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE <= V_{IL}(max), t_{CC} = 15ns	8			mA	
	I_{CC2PS}	CKE & CLK <= V_{IL}(max), t_{CC} = 00	8			mA	
Precharge standby current in non power-down mode	I_{CC2N}	CKE >= V_{IH}(min), CS# >= V_{IH}(min), t_{CC} = 15ns Input signals are charged one time during 30ns	80			mA	
	I_{CC2NS}	CKE >= V_{IH}(min), CLK <= V_{IL}(max), t_{CC} = 00 Input signals ar stable	40			mA	
Active standby current in power-down mode	I_{CC3P}	CKE <= V_{IL}(max), t_{CC} = 15ns	20			mA	
	I_{CC3PS}	CKE & CLK <= V_{IL}(max), t_{CC} = 00	20			mA	
Active standby current in non-power down mode (One bank active)	I_{CC3N}	CKE >= V_{IH}(min), CS# >= V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns	120			mA	
	I_{CC3NS}	CKE >= V_{IH}(min), CLK <= V_{IL}(max), t_{CC}= 00 Input signals are stable	100			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2 Banks actived t_{CCD} = 2CLKs	560	520	520	mA	1
Refresh current	I_{CC5}	t_{RC} >= t_{RC}(min)	800	760	760	mA	2
Self refresh current	I_{CC6}	CKE <= 0.2V	8			mA	

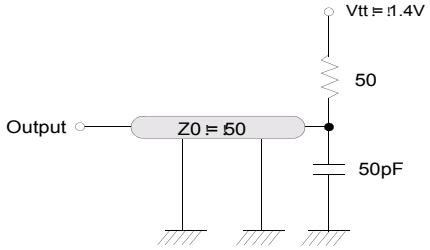
Note: 1. Measured with outputs open.
2.Refresh period is 64ms.

AC Operating Test Conditions (VDD = 3.3V, TA = 0°C to 70°C)

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

Operating AC Parameter

Parameter		Symbol	Version			Unit	Note
			-GA	-GH	-GL		
Row active to row active delay		t_{RRD}(min)	15	20	20	ns	1
RAS# to CAS# delay		t_{RCD}(min)	20	20	20	ns	1
Row precharge time		t_{RP}(min)	20	20	20	ns	1
Row active time		t_{RAS}(min)	45	50	50	ns	1
		t_{RAS}(max)	100			us	
Row cycle time		t_{RC}(min)	65	70	70	ns	1
Last data in to row precharge		t_{RDL}(min)	2			CLK	2
Last data in to Active delay		t_{DAL}(min)	2 CLK + 20ns				
Last data in to new col. addrees delay		t_{CDL}(min)	1			CLK	1
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. address to col. address delay		t_{CCD}(min)	1			CLK	2
Number of valid output data	CAS Latency = 3		2			CLK	3
	CAS Latency =2		1			ea	4

Notes: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

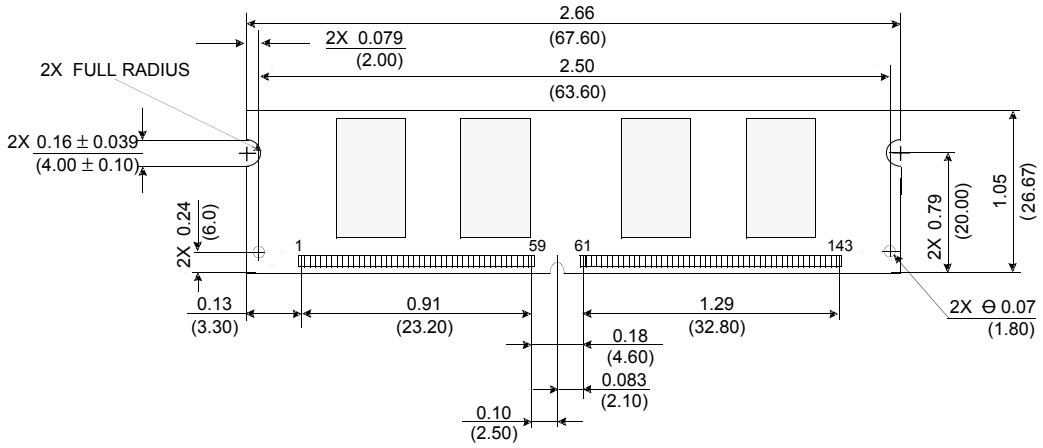
Operating AC Parameter

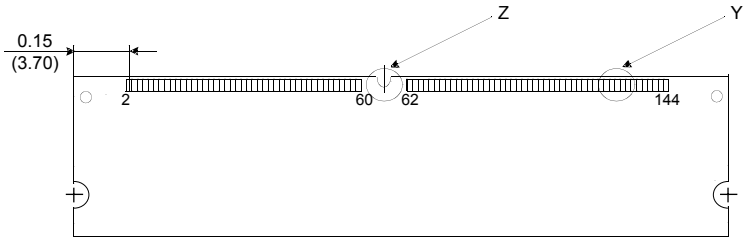
Parameter		Symbol	-GA		-GH		-GL		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency = 3	tCC	7.5	1000	10	1000	10	1000	ns	1
	CAS latency = 2		-		10		10			
CLK to valid output delay	CAS latency = 3	tSAC		5.4		6		6	ns	1,2
	CAS latency = 2			6		6		7		
Output data hold time	CAS latency = 3	tOH	3		3		3		ns	2
	CAS latency = 2		-		3		3			
CLK high pulse width		tCH	2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		ns	3
Input setup time		tSS	1.5		2		2		ns	3
Input hold time		tSH	0.8		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-z	CAS latency = 3	tSHZ		5.4		6		6	ns	
	CAS latency = 2			6		6		7		

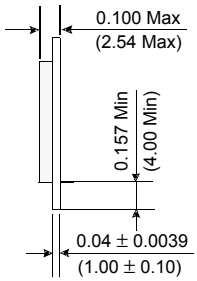
Notes: 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
if tr & tf is longer than 1ns, transient timecompensation should be considered,
i.e. ,[(tr + tf)/2-1]ns should be added to the parameter.

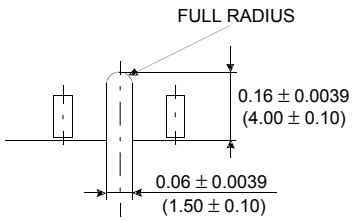
Package Dimensions

Units : Inches (Millimeters)

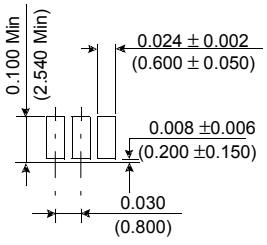








Detail Z



Detail Y

Tolerances : ±.006(.15) unless otherwise specified

Revision History:

Date	Rev.	Page	Changes
03/23/2006	1.2	All	Released spec
10/10/2006	1.3	9	Added History Revision
09/24/2010	1.6	All	Update datasheet