

**Features**

- Operating voltage: 5V
- Low power consumption at 400mW (Typ.)
- Power-down mode: Under 2mA (Typ.)
- 16-bit 30 MSPS A/D converter
- Guaranteed won't miss codes
- 1~6 programmable gain
- Correlated Double Sampling
- $\pm 250\text{mV}$  programmable offset
- Input clamp circuitry
- Internal voltage reference
- Multiplexed byte-wide output (8+8 format)
- Programmable 3-wire serial interface
- 3V/5V digital I/O compatibility
- 3-channel operation up to 30 MSPS
- 2-channel (Even-Odd) operation up to 30 MSPS
- 1-channel operation up to 25 MSPS
- 28-pin SSOP/SOP package (lead-free on request)

**Applications**

Flatbed document scanners

Film scanners

Digital color copiers

Multifunction peripherals

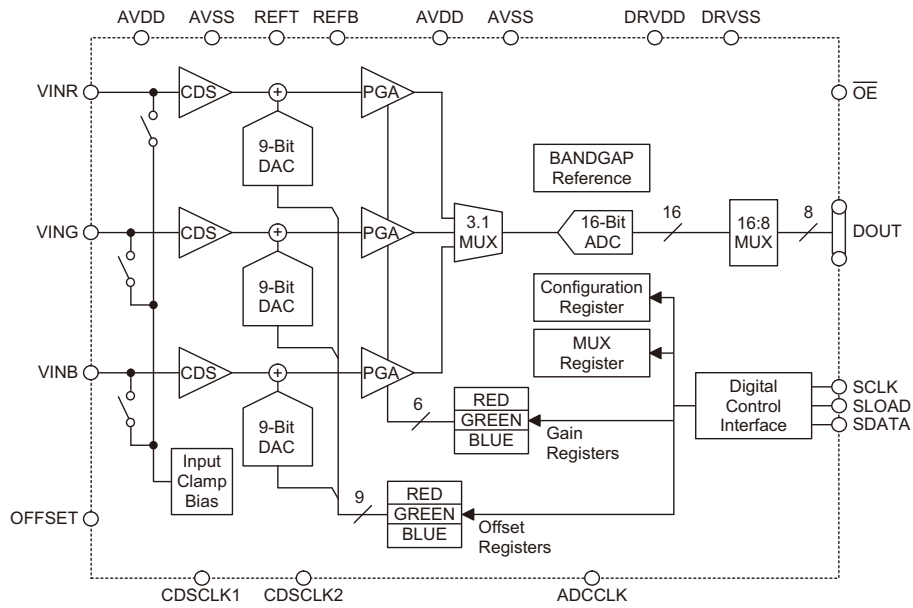
**General Description**

The HT82V26A is a complete analog signal processor for CCD imaging applications. It features a 3-channel architecture designed to sample and condition the outputs of tri-linear color CCD arrays. Each channel consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), and a high performance 16-bit A/D converter.

The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS.

The 16-bit digital output is multiplexed into an 8-bit output word that is accessed using two read cycles. The internal registers are programmed through a 3-wire serial interface, which provides gain, offset and operating mode adjustments.

The HT82V26A operates from a single 5V power supply, typically consumes 400mW of power.

**Block Diagram**

**Pin Assignment**

|          |    |    |        |
|----------|----|----|--------|
| CDSCLK1  | 1  | 28 | AVDD   |
| CDSCLK2  | 2  | 27 | AVSS   |
| ADCCLK   | 3  | 26 | VINR   |
| OE       | 4  | 25 | OFFSET |
| DRVDD    | 5  | 24 | VING   |
| DRVSS    | 6  | 23 | CML    |
| D7 (MSB) | 7  | 22 | VINB   |
| D6       | 8  | 21 | REFT   |
| D5       | 9  | 20 | REFB   |
| D4       | 10 | 19 | AVSS   |
| D3       | 11 | 18 | AVDD   |
| D2       | 12 | 17 | SLOAD  |
| D1       | 13 | 16 | SCLK   |
| D0 (LSB) | 14 | 15 | SDATA  |

**HT82V26A**  
28 SSOP-A/SOP-A

**Pin Description**

| Pin No. | Pin Name        | I/O   | Description                                |
|---------|-----------------|-------|--|
| 1       | CDSCLK1         | DI    | CDS reference clock pulse input            |
| 2       | CDSCLK2         | DI    | CDS data clock pulse input                 |
| 3       | ADCCLK          | DI    | A/D sample clock input for 3-channels mode |
| 4       | $\overline{OE}$ | DI    | Output enable, active low                  |
| 5       | DRVDD           | P     | Digital driver power                       |
| 6       | DRVSS           | P     | Digital driver ground                      |
| 7~14    | D7~D0           | DO    | Digital data output                        |
| 15      | SDATA           | DI/DO | Serial data input/output                   |
| 16      | SCLK            | DI    | Clock input for serial interface           |
| 17      | SLOAD           | DI    | Serial interface load pulse                |
| 19, 27  | AVSS            | P     | Analog ground                              |
| 18, 28  | AVDD            | P     | Analog supply                              |
| 20      | REFB            | AO    | Reference decoupling                       |
| 21      | REFT            | AO    | Reference decoupling                       |
| 22      | VINB            | AI    | Analog input, blue                         |
| 23      | CML             | AO    | Internal reference output                  |
| 24      | VING            | AI    | Analog input, green                        |
| 25      | OFFSET          | AO    | Clamp bias level decoupling                |
| 26      | VINR            | AI    | Analog input, red                          |

**Absolute Maximum Ratings**

|                      |                                |                             |                                  |
|----------------------|--------------------------------|-----------------------------|----------------------------------|
| Supply Voltage ..... | $V_{SS}-0.3V$ to $V_{SS}+5.5V$ | Storage Temperature .....   | $-50^{\circ}C$ to $125^{\circ}C$ |
| Input Voltage .....  | $V_{SS}-0.3V$ to $V_{DD}+0.3V$ | Operating Temperature ..... | $-25^{\circ}C$ to $75^{\circ}C$  |

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**D.C. Characteristics**

| Symbol              | Parameter   | Test Conditions |            | Min. | Typ. | Max. | Unit    |
|---------------------|---|-----------------|------------|------|------|------|---------|
|                     |   | $V_{DD}$        | Conditions |      |      |      |         |
| <b>Logic Inputs</b> |   |                 |            |      |      |      |         |
| $V_{IH}$            | High Level Input Voltage (CDSCLK1, CDSCLK2, ADCCLK, $\overline{OE}$ , SCK, SLOAD) | —               | —          | 2    | —    | —    | V       |
| $V_{IL}$            | Low Level Input Voltage (CDSCLK1, CDSCLK2, ADCCLK, $\overline{OE}$ , SCK, SLOAD)  | —               | —          | —    | —    | 0.8  | V       |
| $V_{IH1}$           | High Level Input Voltage (SDATA)  | —               | —          | 2.5  | —    | —    | V       |
| $V_{IL1}$           | Low Level Input Voltage (SDATA)   | —               | —          | —    | —    | 1.5  | V       |
| $I_{IH}$            | High Level Input Current  | —               | —          | —    | 10   | —    | $\mu A$ |
| $I_{IL}$            | Low Level Input Current   | —               | —          | —    | 10   | —    | $\mu A$ |
| $C_{IN}$            | Input Capacitance   | —               | —          | —    | 10   | —    | pF      |

| Symbol               | Parameter                                | Test Conditions |            | Min.                   | Typ. | Max. | Unit |
|----------------------|--|-----------------|------------|------------------------|------|------|------|
|                      |  | V <sub>DD</sub> | Conditions |                        |      |      |      |
| <b>Logic Outputs</b> |  |                 |            |                        |      |      |      |
| V <sub>OH</sub>      | High Level Output Voltage (SDATA, D0-D7) | —               | —          | DRV <sub>DD</sub> -0.5 | —    | —    | V    |
| V <sub>OL</sub>      | Low Level Output Voltage (SDATA, D0-D7)  | —               | —          | —                      | —    | 0.5  | V    |
| I <sub>OH</sub>      | High Level Output Current                | —               | —          | —                      | 1    | —    | mA   |
| I <sub>OL</sub>      | Low Level Output Current                 | —               | —          | —                      | 1    | —    | mA   |

**A.C. Characteristics**

| Symbol                               | Parameter                      | Test Conditions |            | Min.                  | Typ. | Max.                  | Unit |
|--------------------------------------|--------------------------------|-----------------|------------|-----------------------|------|-----------------------|------|
|                                      |                                | V <sub>DD</sub> | Conditions |                       |      |                       |      |
| <b>Power Supplies</b>                |                                |                 |            |                       |      |                       |      |
| V <sub>ADD</sub>                     | AVDD                           | —               | —          | 4.75                  | 5    | 5.25                  | V    |
| V <sub>DRDD</sub>                    | DRVDD                          | —               | —          | 3                     | 5    | 5.25                  | V    |
| <b>Maximum Conversion Rate</b>       |                                |                 |            |                       |      |                       |      |
| t <sub>MAX3</sub>                    | 3-channel Mode with CDS        | —               | —          | 30                    | —    | —                     | MSPS |
| t <sub>MAX2</sub>                    | 2-channel Mode with CDS        | —               | —          | 30                    | —    | —                     | MSPS |
| t <sub>MAX1</sub>                    | 1-channel Mode with CDS        | —               | —          | 25                    | —    | —                     | MSPS |
| <b>Accuracy (Entire Signal Path)</b> |                                |                 |            |                       |      |                       |      |
|                                      | ADC Resolution                 | —               | —          | —                     | 16   | —                     | Bits |
|                                      | Integral Nonlinear (INL)       | —               | —          | —                     | ±32  | —                     | LSB  |
|                                      | Differential Nonlinear (DNL)   | —               | —          | -1                    | —    | 1                     | LSB  |
|                                      | Offset Error                   | —               | —          | -100                  | —    | 100                   | mV   |
|                                      | Gain Error                     | —               | —          | —                     | 5    | —                     | %FSR |
| <b>Analog Inputs</b>                 |                                |                 |            |                       |      |                       |      |
| R <sub>FS</sub>                      | Full-scale Input Range         | —               | —          | —                     | 2.0  | —                     | Vp-p |
| V <sub>i</sub>                       | Input Limits                   | —               | —          | A <sub>VSS</sub> -0.3 | —    | A <sub>VDD</sub> +0.3 | V    |
| C <sub>i</sub>                       | Input Capacitance              | —               | —          | —                     | 10   | —                     | pF   |
| I <sub>i</sub>                       | Input Current                  | —               | —          | —                     | 10   | —                     | nA   |
| <b>Amplifiers</b>                    |                                |                 |            |                       |      |                       |      |
|                                      | PGA Gain at Minimum            | —               | —          | —                     | 1    | —                     | V/V  |
|                                      | PGA Gain at Maximum            | —               | —          | —                     | 5.85 | —                     | V/V  |
|                                      | PGA Gain Resolution            | —               | —          | —                     | 6    | —                     | Bits |
|                                      | Programmable Offset at Minimum | —               | —          | —                     | -250 | —                     | mV   |
|                                      | Programmable Offset at Maximum | —               | —          | —                     | 250  | —                     | mV   |
|                                      | Offset Resolution              | —               | —          | —                     | 9    | —                     | Bits |
| <b>Temperature Range</b>             |                                |                 |            |                       |      |                       |      |
| t <sub>A</sub>                       | Operating                      | —               | —          | 0                     | —    | 70                    | °C   |
| <b>Power Consumption</b>             |                                |                 |            |                       |      |                       |      |
| P <sub>tot</sub>                     | Total Power Consumption        | —               | —          | —                     | 400  | —                     | mW   |

**Timing Specification**

| Symbol                     | Parameter                         | Min. | Typ. | Max. | Unit   |
|----------------------------|-----------------------------------|------|------|------|--------|
| <b>Clock Parameters</b>    |                                   |      |      |      |        |
| t <sub>PRA</sub>           | 3-channel pixel rate              | 100  | —    | —    | ns     |
| t <sub>PRB</sub>           | 2-channel (Even-Odd) pixel rate   | 66   | —    | —    | ns     |
| t <sub>PRC</sub>           | 1-channel pixel rate              | 40   | —    | —    | ns     |
| t <sub>ADCLK</sub>         | ADCCLK Pulse Width                | 16   | —    | —    | ns     |
| t <sub>C1</sub>            | CDSCLK1 Pulse Width               | 12   | —    | —    | ns     |
| t <sub>C2</sub>            | CDSCLK2 Pulse Width               | 12   | —    | —    | ns     |
| t <sub>C1C2</sub>          | CDSCLK1 Falling to CDSCLK2 Rising | 0    | —    | —    | ns     |
| t <sub>ADC1</sub>          | ADCCLK Rising to CDSCLK1 Falling  | 0    | —    | —    | ns     |
| t <sub>ADC2</sub>          | ADCCLK Rising to CDSCLK2 Falling  | 0    | —    | —    | ns     |
| t <sub>AD</sub>            | Analog Sampling Delay             | 5    | —    | —    | ns     |
| <b>3-Channel Mode Only</b> |                                   |      |      |      |        |
| t <sub>aC2C1</sub>         | CDSCLK2 Falling to CDSCLK1 Rising | 30   | —    | —    | ns     |
| t <sub>aC2ADR</sub>        | CDSCLK2 Falling to ADCCLK Rising  | 30   | —    | —    | ns     |
| t <sub>C2ADR</sub>         | ADCK Falling to CDS2 Rising       | 4    | —    | —    | ns     |
| <b>2-Channel Mode Only</b> |                                   |      |      |      |        |
| t <sub>bC2ADR</sub>        | CDSCLK2 Falling to ADCCLK Rising  | 30   | —    | —    | ns     |
| t <sub>bC1ADR</sub>        | CDSCLK1 Rising to ADCCLK Rising   | 15   | —    | —    | ns     |
| t <sub>bC2C1</sub>         | CDSCLK2 Falling to CDSCLK1 Rising | 15   | —    | —    | ns     |
| <b>1-Channel Mode Only</b> |                                   |      |      |      |        |
| t <sub>cC2C1</sub>         | CDSCLK2 Falling to CDSCLK1 Rising | 15   | —    | —    | ns     |
| t <sub>cC1ADF</sub>        | CDSCLK1 Rising to ADCCLK Falling  | 0    | —    | —    | ns     |
| t <sub>cC2ADR</sub>        | CDSCLK2 Falling to CDSCLK1 Rising | 20   | —    | —    | ns     |
| <b>Serial Interface</b>    |                                   |      |      |      |        |
| f <sub>SCLK</sub>          | Maximum SCLK Frequency            | 10   | —    | —    | MHz    |
| t <sub>LS</sub>            | SLOAD to SCLK Setup Time          | 10   | —    | —    | ns     |
| t <sub>LH</sub>            | SCLK to SLOAD Hold Time           | 10   | —    | —    | ns     |
| t <sub>DS</sub>            | SDATA to SCLK Rising Setup Time   | 10   | —    | —    | ns     |
| t <sub>DH</sub>            | SCLK Rising to SDATA Hold Time    | 10   | —    | —    | ns     |
| t <sub>RDV</sub>           | Falling to SDATA Valid            | 10   | —    | —    | ns     |
| <b>Data Output</b>         |                                   |      |      |      |        |
| t <sub>OD</sub>            | Output Delay                      | —    | 8    | —    | ns     |
|                            | Latency (Pipeline Delay)          | —    | 9    | —    | Cycles |

## Functional Description

### Integral Nonlinear (INL)

Integral nonlinear error refers to the deviation of each individual code from a line drawn from zero scale through a positive full scale. The point used as zero scale occurs 1/2 LSB before the first code transition. A positive full scale is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

### Differential Nonlinear (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed for the 16-bit resolution indicates that all the 65536 codes respectively, are present in the over-all operating range.

### Offset Error

The first ADC code transition should occur at a level 1/2 LSB above the nominal zero scale voltage.

The offset error is the deviation of the actual first code transition level from the ideal level.

### Gain Error

The last code transition should occur for an analog value of 1/2 LSB below the nominal full-scale voltage.

Gain error is the deviation of the actual difference between the first and the last code transitions and the ideal difference between the first and the last code transitions.

### Aperture Delay

The aperture delay is the time delay that occurs when a sampling edge is applied to the HT82V26A until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low, so the aperture delay is measured from each clock's falling edge to the instant the actual internal sample is taken.

## Internal Register Descriptions

| Register Name | Address |    |    | Data Bits |         |     |       |        |               |                   |               |              |
|---------------|---------|----|----|-----------|---------|-----|-------|--------|---------------|-------------------|---------------|--------------|
|               | A2      | A1 | A0 | D8        | D7      | D6  | D5    | D4     | D3            | D2                | D1            | D0           |
| Configuration | 0       | 0  | 0  | 0         | 0       | 1   | 3-CH  | CDS on | Clamp Voltage | Enable Power Down | Output Delay  | 1 byte out   |
| MUX           | 0       | 0  | 1  | 0         | RGB/BGR | Red | Green | Blue   | Delay enable  | CDSCLK1 delay     | CDSCLK2 delay | ADCCLK delay |
| Red PGA       | 0       | 1  | 0  | 0         | 0       | 0   | MSB   |        |               |                   |               | LSB          |
| Green PGA     | 0       | 1  | 1  | 0         | 0       | 0   | MSB   |        |               |                   |               | LSB          |
| Blue PGA      | 1       | 0  | 0  | 0         | 0       | 0   | MSB   |        |               |                   |               | LSB          |
| Red Offset    | 1       | 0  | 1  | MSB       |         |     |       |        |               |                   |               | LSB          |
| Green Offset  | 1       | 1  | 0  | MSB       |         |     |       |        |               |                   |               | LSB          |
| Blue Offset   | 1       | 1  | 1  | MSB       |         |     |       |        |               |                   |               | LSB          |

### Internal Register Map

#### Configuration Register

The configuration register controls the HT82V26A's operating mode and bias levels. Bits D6 should always be set high. Bit D5 will configure the HT82V26A for the 3-channel (high) mode of operation. Setting the bit D4 high will enable the CDS mode of operation, and setting this bit low will enable the SHA mode of operation.

Bit D3 sets the dc bias level of the HT82V26A's input clamp. This bit should always be set high for the 4V clamp bias, unless a CCD with a reset feed through transient exceeding 2V is used. Setting the bit D3 low, the clamp voltage is 3V. Bit D2 controls the power-down mode. Setting bit D2 high will place the HT82V26A into a very low power "sleep" mode. All register contents are retained while the HT82V26A is in the power-down state. Setting bit D1 high will configure the HT82V26A for the digital output (D0–D7) delay 2ns. Bit D0 controls the output mode of the HT82V26A. Setting bit D0 high will enable a single byte output mode where only 8 MSBs of the 16b ADC is output. If bit D0 is set low, then the 16b ADC output is multiplexed into two bytes.

| D8       | D7       | D6       | D5         | D4            | D3         | D2              | D1           | D0                          |
|----------|----------|----------|------------|---------------|------------|-----------------|--------------|-----------------------------|
| Set to 0 | Set to 0 | Set to 1 | 3 channels | CDS operation | Clamp bias | Power-down      | Output delay | 1 byte out (High-byte only) |
|          |          |          | 1=On*      | 1=CDS mode*   | 1=4V*      | 1=On            | 1=On         | 1=On                        |
|          |          |          | 0=Off      | 0=SHA mode    | 0=3V       | 0=Off (Normal)* | 0=Off*       | 0=Off*                      |

**Configuration Register Settings**

Note: \* Power-on default value

**MUX Register**

The MUX register controls the sampling channel order and the 2-channel mode configuration in the HT82V26A. Bits D8 should always be set low. Bit D7 is used when operating in the 3-channel mode or the 2-channel mode. Setting bit D7 high will sequence the MUX to sample the red channel first, then the green channel, and then the blue channel. When in the 3-channel mode, the CDSCLK2 rising edge always resets the MUX to sample the red channel first (see timing diagrams). When bit D7 is set low, the channel order is reversed to blue first, green second, and red third. The CDSCLK2 rising edge will always reset the MUX to sample the blue channel first. Bits D6, D5 and D4 are used when operating in 1 or 2-channel mode. Bit D6 is set high to sample the red channel. Bit D5 is set high to sample the green channel. Bit D4 is set high to sample the blue channel. The MUX will remain stationary during 1-channel mode. The two channel mode is selected by setting two of the channel select bits (D4~D6) high. The MUX samples the channels in the order selected by bit D7. Bits D0~D3 are used for controlling CDSCLK1, CDSCLK2 and ADCCLK internal delay.

| D8       | D7                  | D6              | D5                 | D4                | D3             | D2              | D1              | D0              |
|----------|---------------------|-----------------|--------------------|-------------------|----------------|-----------------|-----------------|-----------------|
| Set to 0 | MUX Order           | Channel Select  |                    |                   | Enable Delay   | CDS1 Delay      | CDS2 Delay      | ADCK Delay      |
|          | 1=R-G-B*<br>0=B-G-R | 1=RED*<br>0=Off | 1=GREEN*<br>0=Off* | 1=BLUE*<br>0=Off* | 0=Off<br>1=On* | 0=2ns*<br>1=4ns | 0=2ns*<br>1=4ns | 0=0ns*<br>1=2ns |

**MUX Register Settings**

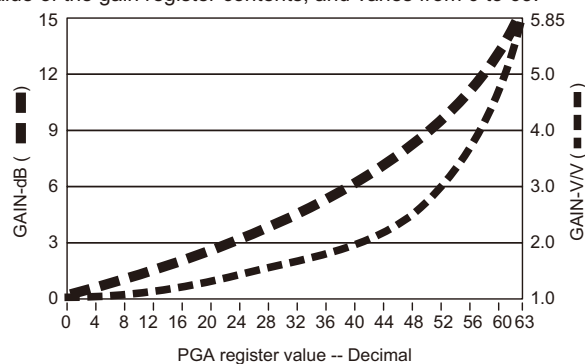
Note: \* Power-on default value

**PGA Gain Registers**

There are three PGA registers for use in individually programming the gain in the red, green and blue channels. Bits D8, D7 and D6 in each register must be set low, and bits D5 through D0 control the gain range in 64 increments. See figure for a graph of the PGA gain versus PGA register code. The coding for the PGA registers is a straight binary, with an all zero words corresponding to the minimum gain setting (1x) and an all one word corresponding to the maximum gain setting (5.85x).

The HT82V26A uses one Programmable Gain Amplifier (PGA) for each channel. Each PGA has a gain range from 1x (0dB) to 5.85x (15.3dB), adjustable in 64 steps. The Figure shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately linear in dB, the gain in V/V varies in nonlinear proportion with the register code, according to the following the equation: 
$$\text{Gain} = \frac{5.85}{1 + 4.85x\left(\frac{63 - G}{63}\right)}$$

Where G is the decimal value of the gain register contents, and varies from 0 to 63.


**PGA Gain Transfer Function**

| D8       | D7       | D6       | D5  | D4 | D3 | D2 | D1 | D0  | Gain (V/V) | Gain (dB) |
|----------|----------|----------|-----|----|----|----|----|-----|------------|-----------|
| Set to 0 | Set to 0 | Set to 0 | MSB |    |    |    |    | LSB |            |           |
| 0        | 0        | 0        | 0   | 0  | 0  | 0  | 0  | 0*  | 1.0        | 0.0       |
| 0        | 0        | 0        | 0   | 0  | 0  | 0  | 0  | 1   | 1.013      | 0.12      |
|          |          |          |     |    | ⋮  |    |    |     | ⋮          | ⋮         |
| 0        | 0        | 0        | 1   | 1  | 1  | 1  | 1  | 0   | 5.43       | 14.7      |
| 0        | 0        | 0        | 1   | 1  | 1  | 1  | 1  | 1   | 5.85       | 15.3      |

**PGA Gain Register Settings**

Note: \* Power-on default value

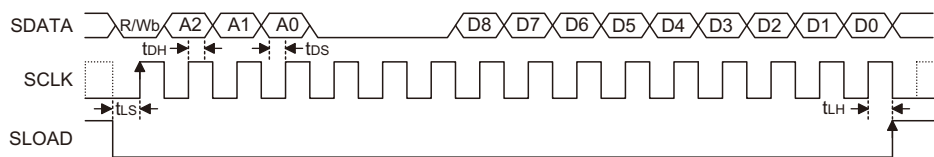
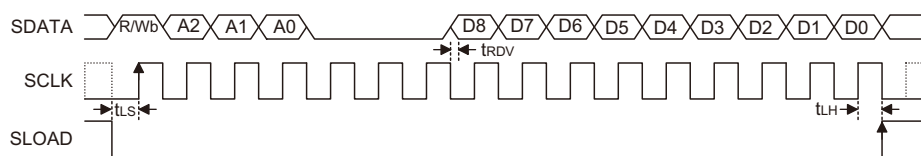
**Offset Registers**

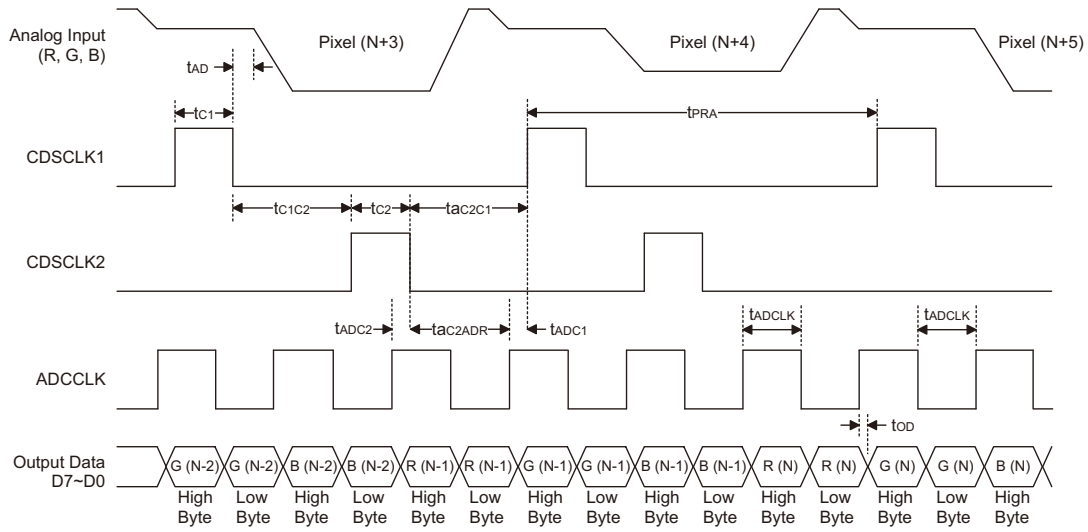
There are three offset registers for use in individually programming the offset in the red, green, and blue channels. Bits D8 through D0 control the offset range from -250mV to 250mV in 512 increments.

The coding for the offset registers is sign magnitude, with D8 as the sign bit. The Table shows the offset range as a function of the bits D8 through D0.

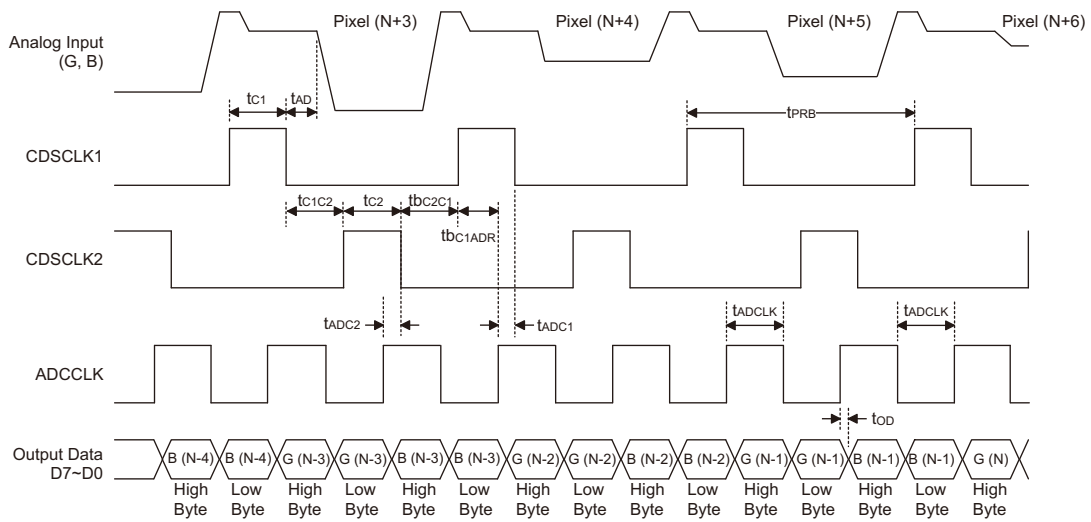
| D8  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0  | Offset (mV) |
|-----|----|----|----|----|----|----|----|-----|-------------|
| MSB |    |    |    |    |    |    |    | LSB |             |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0*  | 0           |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1   | 0.98        |
|     |    |    |    |    | ⋮  |    |    |     | ⋮           |
| 0   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1   | 250         |
| 1   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0   | 0           |
| 1   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1   | -0.98       |
|     |    |    |    |    | ⋮  |    |    |     | ⋮           |
| 1   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1   | -250        |

Note: \* Power-on default value

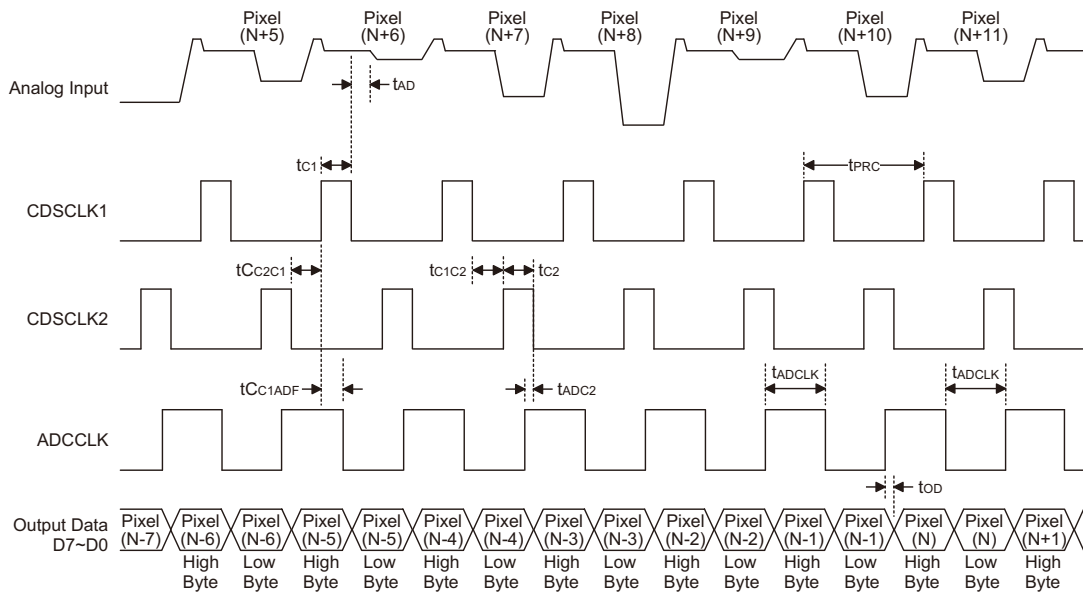
**Timing Diagrams**

**Serial Write Operation Timing**

**Serial Read Operation Timing**



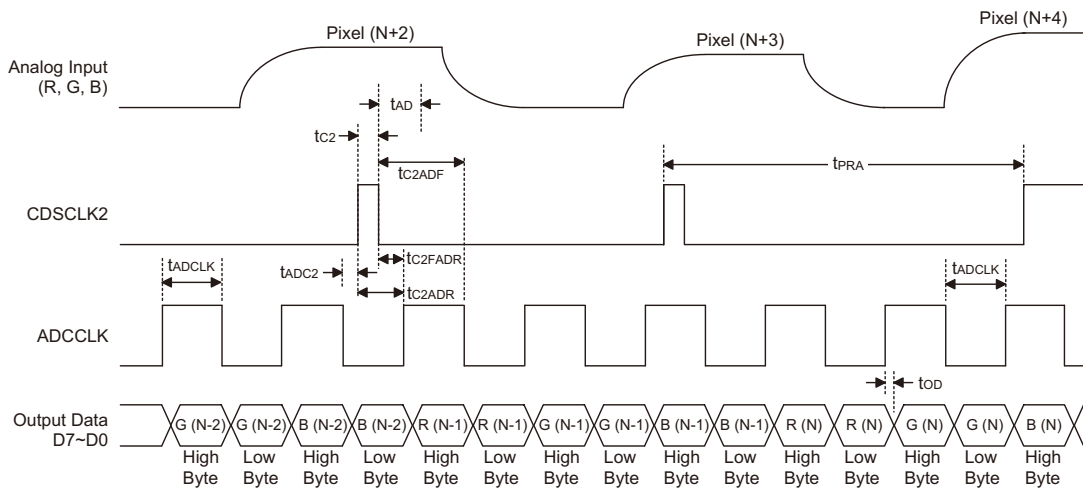
**3-Channel CCD Mode Timing (Select R-G-B Mode)**



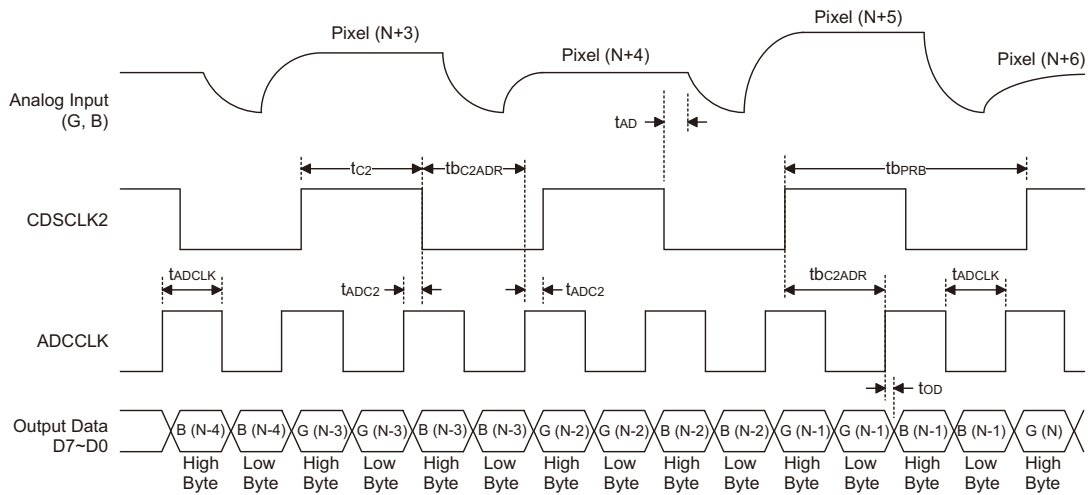
**2-Channel CCD Mode Timing (Select G-B Mode)**



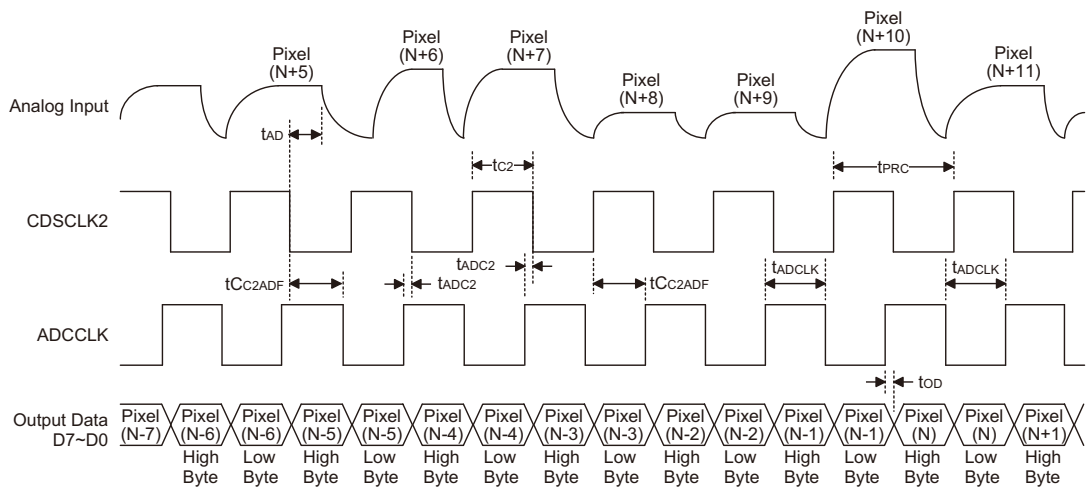
1-Channel CCD Mode Timing



3-Channel SHA Mode Timing (Select R-G-B Mode)



**2-Channel SHA Mode Timing (Select G-B Mode)**

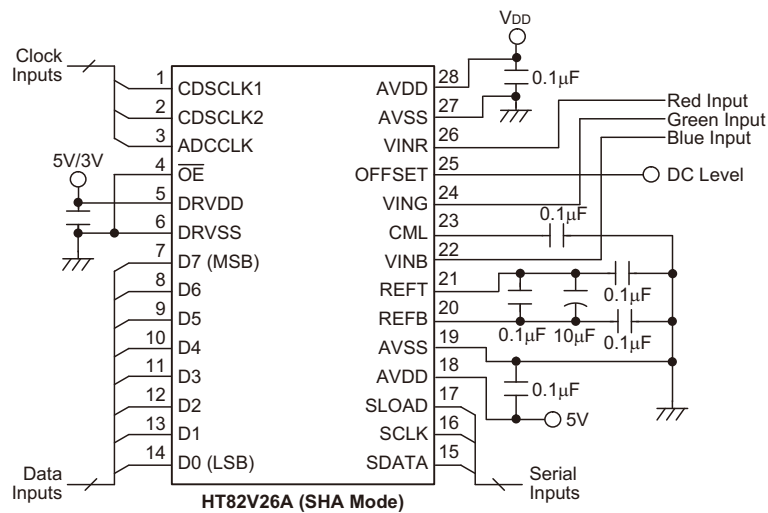
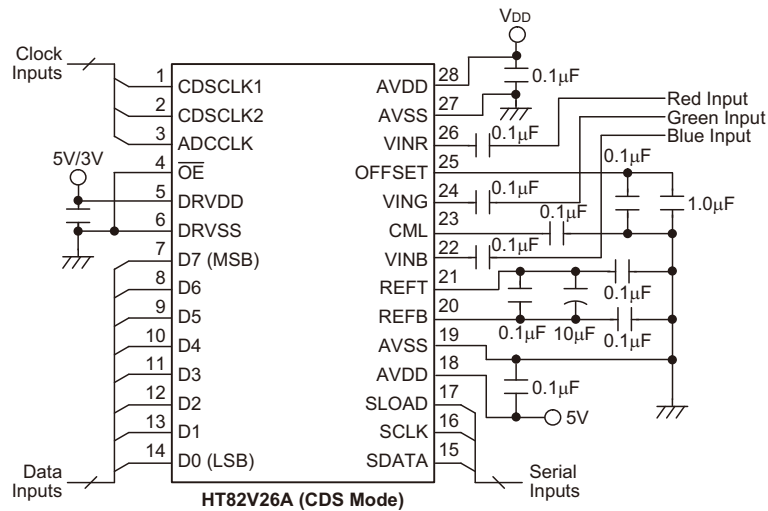


**1-Channel SHA Mode Timing**

### Application Circuits

The recommended circuit configuration for the 3-channel CDS mode operation is shown in the figure below. The recommended input coupling capacitor value is 0.1 $\mu$ F.

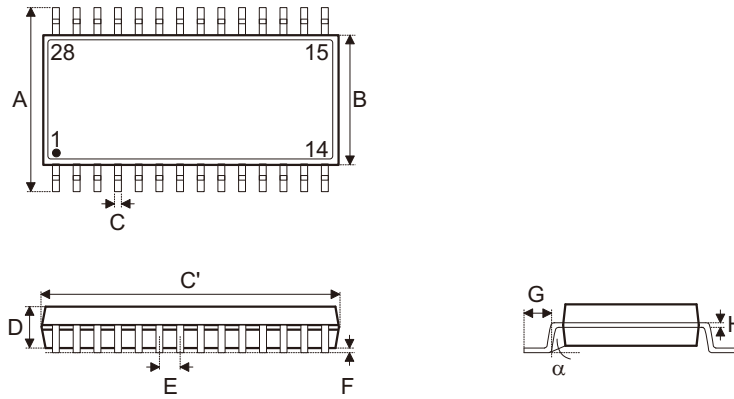
A single ground plane is recommended for the HT82V26A. A separate power supply may be used for DRVDD, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as with the rest of the HT82V26A. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC, or by using external digital buffers. To minimize the effect of digital transients during major output code transitions, the falling edge of the CDSCLK2 should occur in coincidence with or before the rising edge of ADCCLK. All 0.1 $\mu$ F decoupling capacitors should be located as close as possible to the HT82V26A pins. When operating in a single channel mode, the unused analog inputs should be grounded.



**Note:** For the 3-channel SHA mode, all of the above considerations also apply for this configuration, except that the analog input signals are directly connected to the HT82V26A without the use of coupling capacitors. The OFFSET pin should be grounded if the inputs to the HT82V26A are to be referenced to ground, or a DC offset voltage should be applied to the OFFSET pin in the case where a coarse offset needs to be removed from the inputs. The analog input signals must already be dc-biased between 0V and 2V, if OFFSET is connected to ground.

**Package Information**

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website (<http://www.holtek.com.tw/english/literature/package.pdf>) for the latest version of the package information.

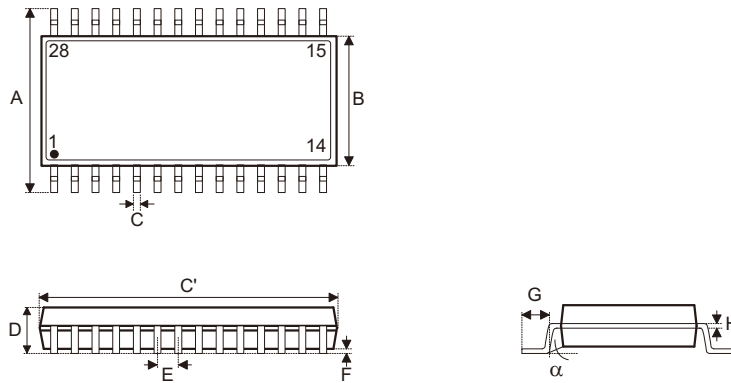
**28-pin SSOP (209mil) Outline Dimensions**


• MO-150

| Symbol   | Dimensions in inch |       |       |
|----------|--------------------|-------|-------|
|          | Min.               | Nom.  | Max.  |
| A        | 0.291              | —     | 0.323 |
| B        | 0.197              | —     | 0.220 |
| C        | 0.009              | —     | 0.013 |
| C'       | 0.390              | —     | 0.413 |
| D        | —                  | —     | 0.079 |
| E        | —                  | 0.026 | —     |
| F        | 0.002              | —     | —     |
| G        | 0.022              | —     | 0.037 |
| H        | 0.004              | —     | 0.008 |
| $\alpha$ | 0°                 | —     | 8°    |

| Symbol   | Dimensions in mm |      |       |
|----------|------------------|------|-------|
|          | Min.             | Nom. | Max.  |
| A        | 7.40             | —    | 8.20  |
| B        | 5.00             | —    | 5.60  |
| C        | 0.22             | —    | 0.33  |
| C'       | 9.90             | —    | 10.50 |
| D        | —                | —    | 2.00  |
| E        | —                | 0.65 | —     |
| F        | 0.05             | —    | —     |
| G        | 0.55             | —    | 0.95  |
| H        | 0.09             | —    | 0.21  |
| $\alpha$ | 0°               | —    | 8°    |

28-pin SOP (300mil) Outline Dimensions



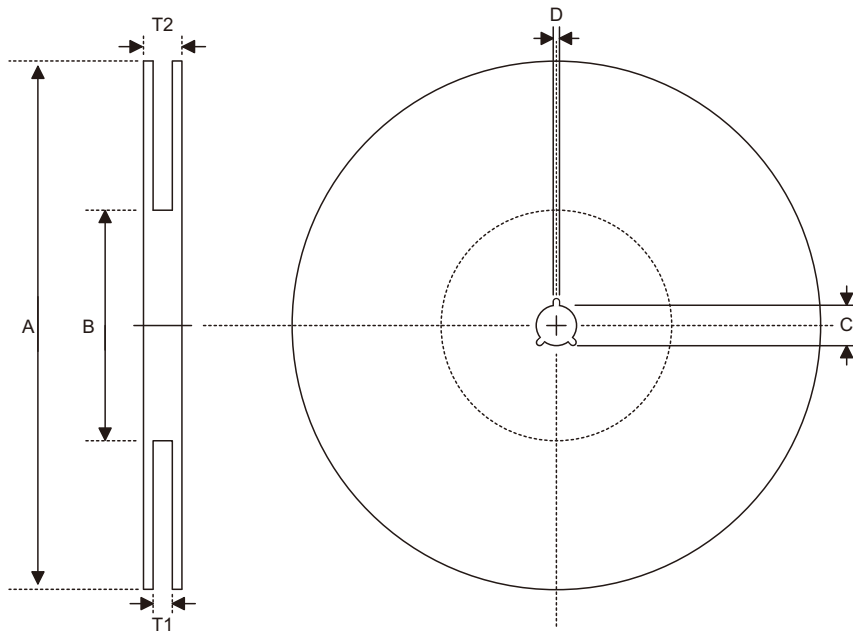
• MS-013

| Symbol   | Dimensions in inch |       |       |
|----------|--------------------|-------|-------|
|          | Min.               | Nom.  | Max.  |
| A        | 0.393              | —     | 0.419 |
| B        | 0.256              | —     | 0.300 |
| C        | 0.012              | —     | 0.020 |
| C'       | 0.697              | —     | 0.713 |
| D        | —                  | —     | 0.104 |
| E        | —                  | 0.050 | —     |
| F        | 0.004              | —     | 0.012 |
| G        | 0.016              | —     | 0.050 |
| H        | 0.008              | —     | 0.013 |
| $\alpha$ | 0°                 | —     | 8°    |

| Symbol   | Dimensions in mm |      |       |
|----------|------------------|------|-------|
|          | Min.             | Nom. | Max.  |
| A        | 9.98             | —    | 10.64 |
| B        | 6.50             | —    | 7.62  |
| C        | 0.30             | —    | 0.51  |
| C'       | 17.70            | —    | 18.11 |
| D        | —                | —    | 2.64  |
| E        | —                | 1.27 | —     |
| F        | 0.10             | —    | 0.30  |
| G        | 0.41             | —    | 1.27  |
| H        | 0.20             | —    | 0.33  |
| $\alpha$ | 0°               | —    | 8°    |

**Product Tape and Reel Specifications**

**Reel Dimensions**

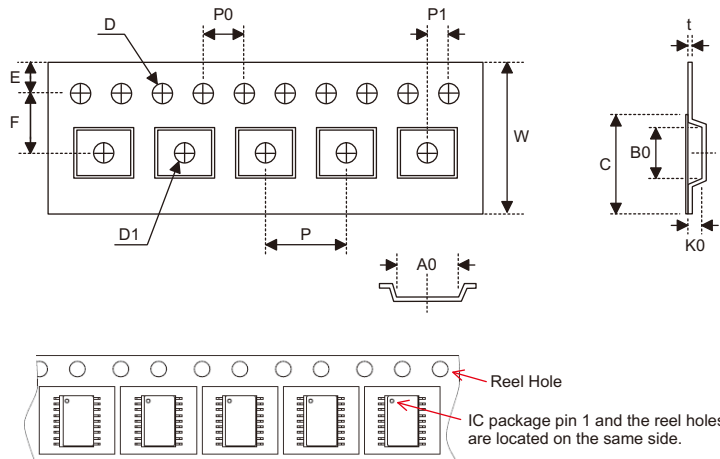


SOP 28W (300mil)

| Symbol | Description           | Dimensions in mm          |
|--------|-----------------------|---------------------------|
| A      | Reel Outer Diameter   | 330.0±1.0                 |
| B      | Reel Inner Diameter   | 100.0±1.5                 |
| C      | Spindle Hole Diameter | 13.0 <sup>+0.5/-0.2</sup> |
| D      | Key Slit Width        | 2.0±0.5                   |
| T1     | Space Between Flange  | 24.8 <sup>+0.3/-0.2</sup> |
| T2     | Reel Thickness        | 30.2±0.2                  |

SSOP 28N (209mil)

| Symbol | Description           | Dimensions in mm          |
|--------|-----------------------|---------------------------|
| A      | Reel Outer Diameter   | 330.0±1.0                 |
| B      | Reel Inner Diameter   | 100.0±1.5                 |
| C      | Spindle Hole Diameter | 13.0 <sup>+0.5/-0.2</sup> |
| D      | Key Slit Width        | 2.0±0.5                   |
| T1     | Space Between Flange  | 28.4 <sup>+0.3/-0.2</sup> |
| T2     | Reel Thickness        | 31.1 (max.)               |

**Carrier Tape Dimensions**

**SOP 28W (300mil)**

| Symbol | Description                              | Dimensions in mm            |
|--------|--|-----------------------------|
| W      | Carrier Tape Width                       | 24.0±0.3                    |
| P      | Cavity Pitch                             | 12.0±0.1                    |
| E      | Perforation Position                     | 1.75±0.10                   |
| F      | Cavity to Perforation (Width Direction)  | 11.5±0.1                    |
| D      | Perforation Diameter                     | 1.5 <sup>+0.1/-0.0</sup>    |
| D1     | Cavity Hole Diameter                     | 1.50 <sup>+0.25/-0.00</sup> |
| P0     | Perforation Pitch                        | 4.0±0.1                     |
| P1     | Cavity to Perforation (Length Direction) | 2.0±0.1                     |
| A0     | Cavity Length                            | 10.85±0.10                  |
| B0     | Cavity Width                             | 18.34±0.10                  |
| K0     | Cavity Depth                             | 2.97±0.10                   |
| t      | Carrier Tape Thickness                   | 0.35±0.01                   |
| C      | Cover Tape Width                         | 21.3±0.1                    |

**SSOP 28N (209mil)**

| Symbol | Description                              | Dimensions in mm            |
|--------|--|-----------------------------|
| W      | Carrier Tape Width                       | 24.0±0.3                    |
| P      | Cavity Pitch                             | 12.0±0.1                    |
| E      | Perforation Position                     | 1.75±0.10                   |
| F      | Cavity to Perforation (Width Direction)  | 11.5±0.1                    |
| D      | Perforation Diameter                     | 1.5 <sup>+0.1/-0.0</sup>    |
| D1     | Cavity Hole Diameter                     | 1.50 <sup>+0.25/-0.00</sup> |
| P0     | Perforation Pitch                        | 4.0±0.2                     |
| P1     | Cavity to Perforation (Length Direction) | 2.0±0.1                     |
| A0     | Cavity Length                            | 8.4±0.1                     |
| B0     | Cavity Width                             | 10.65±0.10                  |
| K0     | Cavity Depth                             | 2.4±0.1                     |
| t      | Carrier Tape Thickness                   | 0.30±0.05                   |
| C      | Cover Tape Width                         | 21.3±0.1                    |

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