Features

- Glueless slave SPI interface to Holtek's MCU
- USB (Universal Serial Bus) 2.0 Full-speed module
  - 6 endpoints (endpoint 0 included)
  - FIFO: 8, 8, 8, 64, 8, 64 for EP0~EP5 respectively
- Operating voltage: V_{DD} = 3.3V~5.5V
- Suspend Mode with low suspend current
- Remote Wake-up function
- USB Multiple Interrupt Generation Sources:
  - Access of the corresponding USB FIFO from the USB host
  - USB suspend signal from the USB host
  - USB resume signal from the USB host
  - USB Reset signal from the USB host
- CMOS external clock input, CLKI, with frequency 6MHz/12MHz for the USB PLL clock
- 16-pin NSOP package

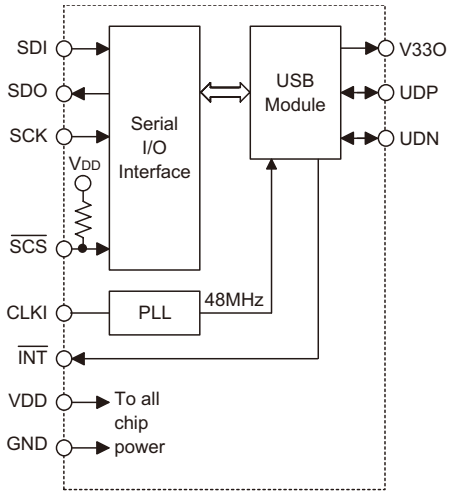
General Description

This device is a companion chip for microcontrollers to provide USB connectivity with the USB host. Six USB endpoints are supported with 8/8/8/64/8/64-byte FIFO for endpoint 0~5 respectively. An external interrupt output to the host MCU is used for inetrrupt-driven operation.

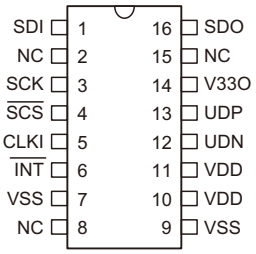
However, the host MCU may also poll the status register to obtain the latest status if the interrupt is not used.

The possible applications include low-cost data links for computers/peripherals, portable and battery operated devices/instruments, factory automation and process control.

Block Diagram



Pin Assignment



HT45B0K
16 NSOP-A

Pin Description

Pin Name	I/O	Descriptions
SDI	I	Serial I/O data input SDI is high impedance when $\overline{SCS}$ = HIGH
SDO	O	Serial I/O data output. SDO is high impedance when $\overline{SCS}$ = HIGH
SCK	I	Serial I/O clock input SCK is high impedance when $\overline{SCS}$ = HIGH
$\overline{SCS}$	I	Serial I/O Chip select input, low active Connected to internal pull-high resistor.
CLKI	I	External clock input
$\overline{INT}$	O	Interrupt output - CMOS output structure Connected to the external interrupt input of MCU A USB related interrupt will generate a low pulse signal on this line
V33O	—	3.3V regulator output
UDP	I/O	USBD+ line USB function is controlled by software control register.
UDN	I/O	USBD- line USB function is controlled by software control register.
VDD	—	Positive power supply
VSS	—	Negative power supply, ground
NC	—	No connection

Absolute Maximum Ratings

Supply Voltage.....V_{SS}−0.3V to V_{SS}+6.0V
Input Voltage.....V_{SS}−0.3V to V_{DD}+0.3V
Storage Temperature.....−50°C to +150°C
Operating Temperature.....−40°C to +85°C
I_{OH} Total.....−10mA
I_{OL} Total.....15mA
Total Power Dissipation.....10mW

Note : These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	f_{CLKI}=6MHz or 12MHz	3.3	—	5.5	V
I_{DD}	Operating Current (SPI Enabled, USB Transceiver and 3.3V Regulator On)	3.3V	f_{CLKI}=6MHz, SCK= f_{CLKI}/4	—	4.0	6.0	mA
		5.0V		—	6.5	10	mA
		3.3V	f_{CLKI}=12MHz, SCK= f_{CLKI}/4	—	4.0	7.0	mA
		5.0V		—	7.0	10	mA
I_{SUS}	Suspend Current (SPI Enabled, USB Suspend and 3.3V Regulator On)	—	Output no load, SUSP2=1 (bit 4 in UCC)	—	400	500	μA
I_{STB}	Standby Current (SPI Disabled, USB Disabled and 3.3V Regulator Off)	—	Output no load	—	0.1	1	μA
V_{IL1}	Input Low Voltage for I/O pins	—	—	0	—	$0.3\times V_{DD}$	V
V_{IH1}	Input High Voltage for I/O pins	—	—	$0.7\times V_{DD}$	—	V_{DD}	V
V_{IL2}	Input Low Voltage for CLKI	—	—	0	—	$0.3\times V_{DD}$	V
V_{IH2}	Input High Voltage for CLKI	—	—	$0.7\times V_{DD}$	—	V_{DD}	V
I_{OL}	I/O pins Sink Current	3.3V	V_O=$0.1\times V_{DD}$	4.0	12	—	mA
		5.0V		10	25	—	mA
I_{OH}	I/O pins Source Current	3.3V	V_O=$0.9\times V_{DD}$	-4.0	-5.0	—	mA
		5.0V		-5.0	-10	—	mA
R_{PH}	Pull-high Resistance for $\overline{SCS}$ only	3.3V	—	15	45	75	kΩ
		5V		10	30	50	kΩ

A.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
R_{POR}	V_{DD} Slew Rate for POR	—	—	0.0034	—	—	V/ms
f_{CLKI}	System Clock (External Clock Input)	3.3V~5.0V	—	—	6	—	MHz
				—	12	—	MHz
t_{CP}	SCK Period (t_{CH} + $_{CL}$)	3.3V	—	62.5	—	—	ns
		5.0V	—	50.0	—	—	ns
t_{CH}	SCK High Time	3.3V	—	28	—	—	ns
		5.0V	—	22	—	—	ns
t_{CL}	SCK Low Time	3.3V	—	28	—	—	ns
		5.0V	—	22	—	—	ns
t_{CSW}	$\overline{SCS}$ High Pulse Width	3.3V	—	500	—	—	ns
		5.0V	—	400	—	—	ns
t_{CSS}	$\overline{SCS}$ to SCK Setup Time	—	—	100	—	—	ns
t_{CSH}	$\overline{SCS}$ to SCK Hold Time	—	—	0	—	—	ns
t_{SDS}	SDI to SCK Setup Time	—	—	100	—	—	ns
t_{SDH}	SDI to SCK Hold Time	—	—	0	—	—	ns
t_R	SPI Output Rise Time	—	—	—	10	—	ns
t_F	SPI Output Fall Time	—	—	—	10	—	ns
t_W	SPI Data Output Delay Time	—	—	$\overline{0}$	—	—	ns
$t_{\overline{INT}}$	$\overline{INT}$ Pin Low Pulse Signal Output Time	—	—	1	—	—	t_{CLKI}

Functional Description

SPI Interface

The MCU communicates with the USB Module via an internal SPI interface. The SPI interface on this device is comprised of four signals: $\overline{SCS}$ (SPI Chip Select), SCK (SPI Clock), SDI (Serial Data Input) and SDO (Serial Data Output). The SPI master, which is the MCU, asserts $\overline{SCS}$ by pulling it low to start the data transaction cycle. When the first 8 bits of data are transmitted, $\overline{SCS}$ should not return to a high level. Instead, $\overline{SCS}$ must remain at a low level until the whole data transaction is completed. If $\overline{SCS}$ is de-asserted, that is returned to a high level, before the 16-bit data transaction is completed, all data bits will be discarded by the USB Module SPI slave.

SPI Command Protocol

To initiate a data transaction, the MCU master SPI needs to pull $\overline{SCS}$ to a low level first and then also pull SCK low. The input data bit on SDI should be stable before the next SCK rising edge, as the device will latch the SDI status on the next SCK rising edge. Regarding the SDO line, the output data bit will be updated on the SCK falling edge. The master needs to obtain the line status before the next SCK falling edge.

The registers corresponding to the USB module in this device are categorized into two types known as general registers and FIFO registers. The write/read operation access protocols for the two types of registers are different. Each transaction consists of a command/address phase and a data phase. For general registers, there are a total of 16 bits of data subdivided into 8-bits of command/address and 8-bits of data, transmitted and/or received by the SPI interface for each transaction. For the FIFO registers, there is an 8-bit command/address and an N-bytes of data transmitted to or received from the USB module using the SPI interface, where N is the number of accessed FIFO registers. After a complete transaction has been implemented, the master needs to set $\overline{SCS}$ to a high level in preparation for the next data transaction. When $\overline{SCS}$ is high, the SPI interface is disabled and SDO will be set to a high impedance state. If necessary, the master can de-assert the $\overline{SCS}$ pin to abort the transaction at any time which will cause any data transactions to be abandoned.

Both read and write operations are conducted along the SPI common interface with the following respective formats.

Registers are divided into two groups: general registers and FIFO registers.

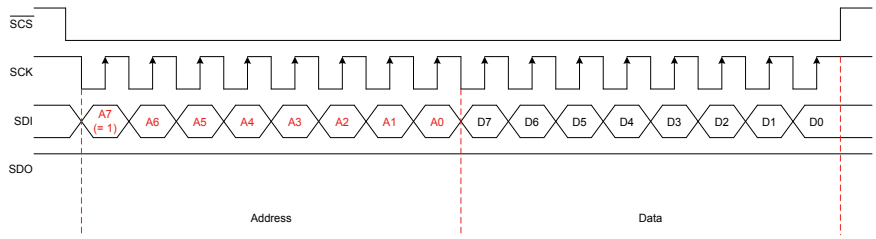
- General Registers: address = USR, USC, UCC, AWR, STALL, SIES, MISC, SETIO, UIC, PIPE, SWRST=00h ~ 0Ch (09h is unused)
- FIFO Registers: address = FIFO0~FIFO5=10h ~ 15h

General Register Operation Format

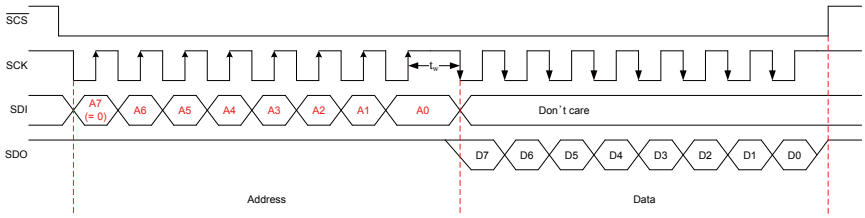
The SPI master asserts the $\overline{SCS}$ line (pulled low) to start the data transaction cycle. When the first 8 data bits are transmitted, the $\overline{SCS}$ signal should not be immediately returned to a high level but instead, must remain at a low level until the complete 16-bit data transaction is completed.

If the $\overline{SCS}$ line is de-asserted (returns high) before the 16-bit data transaction is completed, all data bits will be discarded by the SPI slave.

- General Register Write: 1-byte command/address + 1-byte data



- General Register Read: 1-byte command/address + 1-byte data



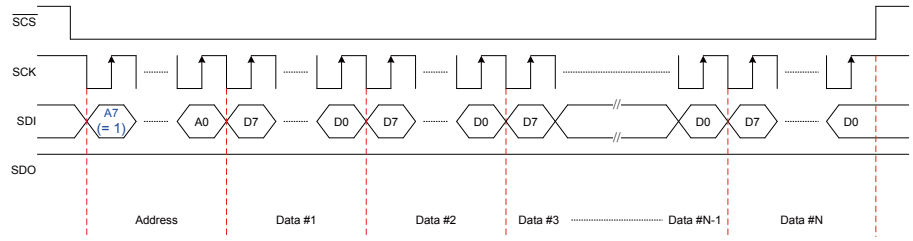
FIFO Register Operation Format

More than 1 byte data can be transmitted or received within one transaction.

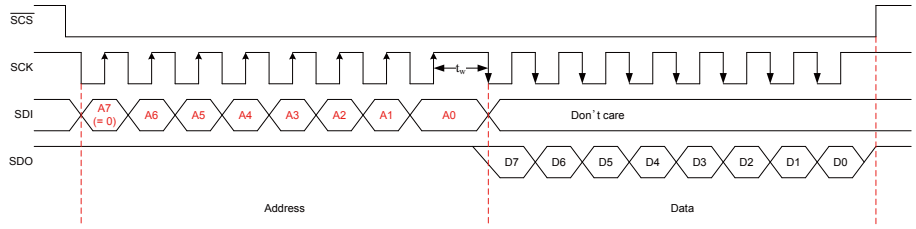
The SPI master asserts the $\overline{SCS}$ line (pulled low) to start the data transaction cycle. The first byte specifies the address of the FIFO registers. The other bytes are data to/from the FIFO.

Once the $\overline{SCS}$ line is de-asserted (pulled high), incomplete data, that is data less than 8 bits, should be discarded.

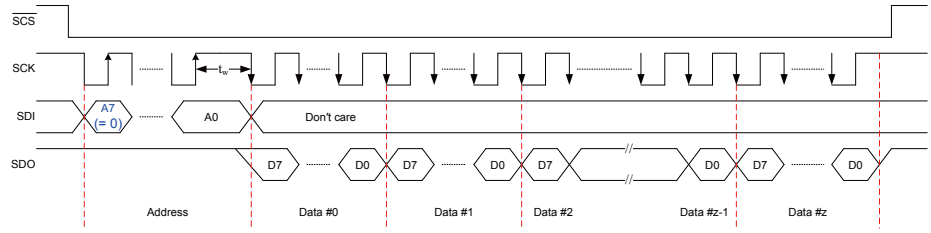
- FIFO Register Write: 1-byte command/address + N-byte data



- FIFO Register Read by single mode (S/C=1): 1-byte command/address + 1-byte data



- FIFO Register Read by continuous mode (S/C=0): 1-byte command/address + N-byte data



USB Module

To communicate with an external USB host, the internal USB module has the external pins known as UDP and UDN along with the 3.3V regulator output V33O. All data transmissions and receptions between MCU and USB module including USB commands are conducted along the interconnected SPI interface. The USB module has 6 endpoints and 160 bytes FIFO for the endpoints respectively. A Serial Interface Engine (SIE) decodes the incoming USB data stream and transfers it to the correct endpoint buffer memory (FIFO). The USB function control is implemented using a series of registers accessed by the MCU using its SPI Master serial interface. A series of status registers provide the user with the USB data transfer situation as well as any error conditions. The USB contains its own independent interrupt which can be used to indicate when the USB FIFOs are accessed by the host device or a change of the USB operating conditions including the USB suspend mode, resume event or USB reset occurs.

USB Accessing Commands

There are both read and write commands for accessing the USB Module. For reading and writing to registers, both command and address information is contained within a single byte. A series of registers which are addressed by 5 address bits A4~A0 are available to control the USB module for Read/Write Registers commands. The format for reading and writing commands is shown in the following table.

Command Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read operation	0	S/C	x	A4	A3	A2	A1	A0
Write operation	1	x	x	A4	A3	A2	A1	A0

Note: 1. “x” here stands for “don’t care”.

2. S/C=0: Read by continuous mode (Default)
   S/C=1: Read by single mode

USB Status and Control Registers

There are several registers associated with the USB function. Some of the registers control the overall function of the USB module as well as the interrupts, while some of the registers contain the status bits which indicate the USB data transfer situations and error condition. Also there are FIFOs for the USB endpoints to store the data received from or to be transmitted to the USB host. The USB module has 6 endpoints (EP0~EP5) with different FIFO size for each one. The FIFO size is 8 bytes for EP0~EP2 and EP4 which support “Interrupt transfer”, while the FIFO size for EP3 and EP5 is 64 bytes which can support “Bulk transfer”.

USB Register Summary

Address	Name	POR state	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	USC	--00 0000	—	—	PLL	V33C	RESUME	URST	RMWK	SUSP
01H	USR	--00 0000	—	—	EP5IF	EP4IF	EP3IF	EP2IF	EP1IF	EP0IF
02H	UCC	-0-0 0000	—	SYSCLK	—	SUSP2	USBCKEN	EPS2	EPS1	EPS0
03H	AWR	0000 0000	UAD6	UAD5	UAD4	UAD3	UAD2	UAD1	UAD0	WKEN
04H	STALL	--11 1110	—	—	STL5	STL4	STL3	STL2	STL1	STL0
05H	SIES	0100 0000	NMI	—	—	—	—	—	ERR	ASET
06H	MISC	0x1- -000	LEN0	READY	SETCMD	—	—	CLEAR	TX	REQUEST
07H	SETIO	--11 1110	—	—	SETIO5	SETIO4	SETIO3	SETIO2	SETIO1	DATATG
08H	UIC	--00 0000	—	—	EU5I	EU4I	EU3I	EU2I	EU1I	EU0I
09H	Unused	---- ----	Reserved							
0AH	PIPE	0-00 000-	SUSPC	—	EP5E	EP4E	EP3E	EP2E	EP1E	—
0BH	SWRST	---- ---0	—	—	—	—	—	—	—	RESET
0CH~0FH	Unused	---- ----	Reserved							
10H	FIFO0	xxxx xxxx	Data for endpoint 0							
11H	FIFO1	xxxx xxxx	Data for endpoint 1							
12H	FIFO2	xxxx xxxx	Data for endpoint 2							
13H	FIFO3	xxxx xxxx	Data for endpoint 3							
14H	FIFO4	xxxx xxxx	Data for endpoint 4							
15H	FIFO5	xxxx xxxx	Data for endpoint 5							
16H~1FH	Unused	---- ----	Reserved							

USC Register

The USC register contains the status bits for USB suspend, resume and reset indications. It also contains the bits used to control the Remote Wake-up, V33O output and PLL functions. Further explanation on each bit is given below:

USC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	PLL	V33C	RESUME	URST	RMWK	SUSP
R/W	—	—	R/W	R/W	R	R	R/W	R
POR	—	—	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as "0".

Bit 5 PLL: PLL enable control
0: turn on the PLL
1: turn off the PLL

Bit 4 V33C: V33O output enable control
0: turn off the V33O output
1: turn on the V33O output

Bit 3 RESUME: USB resume indication flag
0: USB device does not receive the resume signal or has left the suspend mode.
1: USB device receives the resume signal and is going to leave the suspend mode.
When the USB device receives the resume signal, this bit is set to 1 by SIE. This bit will appear for about 20ms, waiting for the MCU to detect it. When the RESUME is set by SIE, an interrupt will be generated to wake up the MCU. In order to detect the suspend state, MCU should set the USBCKEN bit to 1 and clear the PLL and SUSPC bits to 0 to enable the SIE and PHY functions. The RESUME bit will be cleared when the SUSP bit

is set to 0. When the MCU detects the suspend mode SUSP, the resume signal RESUME which causes MCU to wake up should be remembered and taken into consideration.

Bit 2 URST: USB reset indication flag
0: No USB reset event occurred.
1: USB reset event has occurred.
The USB bit is set and cleared by USB SIE. When the URST bit is set to 1, it indicates that a USB reset event has occurred and a USB interrupt will be initiated.

Bit 1 RMWK: USB remote wake-up command
0: disable USB remote wake-up command
1: initiate USB remote wake-up command
The RMWK is set to 1 by MCU to force the USB host leaving the suspend mode. Set RMWK bit to 1 to initiate the remote walk-up command. When the RMWK bit is set to 1, a 2μs delay for clearing this bit to 0 is necessary to ensure that the RMWK command is accepted by the SIE.

Bit 0 SUSP: USB suspend indication flag
0: USB leaves the suspend mode.
1: USB enters the suspend mode.
This bit is read only and set to 1 by SIE to indicate that the USB bus enters the suspend mode.
The USB interrupt is also generated when the SUSP bit is asserted.

USR Register

The USR (USB endpoint interrupt status register) register is consisted of the endpoint request flags (EP0IF~EP5IF) used to indicate which endpoint is accessed. When an endpoint is accessed, the related endpoint request flag will be set to 1 by SIE and a USB interrupt will be generated if the control bits related to the USB interrupt are enabled and the stack in the host MCU is not full. When the active endpoint request flag is serviced, the endpoint request flag has to be cleared to 0 by application program.

USR Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	EP5IF	EP4IF	EP3IF	EP2IF	EP1IF	EP0IF
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as “0”.

Bit 5~0 EP5IF~EP0IF: Endpoint Interrupt request flags
0: the corresponding Endpoint is not accessed.
1: the corresponding Endpoint has been accessed.

UCC Register

The UCC register is the system clock control register implemented to select the clock used by the MCU. This register consists of USB clock control bit USBCKEN, second suspend mode control bit SUSP2 and system clock selection bit SYSCLK. This register is also used to select which endpoint FIFO is accessed by Endpoint FIFO Selection bits EPS2~EPS0. Further explanation on each of the bits is given below:

UCC Register

Bit	7	6	5	4	3	2	1	0
Name	—	SYSCLK	—	SUSP2	USBCKEN	EPS2	EPS1	EPS0
R/W	—	R/W	—	R/W	R/W	R/W	R/W	R/W
POR	—	0	—	0	0	0	0	0

Bit 7 Unimplemented, read as "0".

Bit 6 SYSCLK: System clock input selection
0: 12MHz clock is used
1: 6MHz clock is used
This bit is used to specify the system clock oscillator frequency used by the MCU. If a 6MHz crystal oscillator or resonator is used, this bit should be set to 1. If a 12MHz crystal oscillator or resonator is used, this bit should be set to 0.

Bit 5 Unimplemented, read as "0".

Bit 4 SUSP2: Suspend mode 2 control
0: optimized setting in suspend mode
1: test setting in suspend mode. The band-gap circuit is turned off.
It is strongly recommended that this bit should be set to 0 when the USB interface is in suspend mode. Otherwise, the unpredictable results will occur.

Bit 3 USBCKEN: USB clock enable control
0: USB clock is disabled
1: USB clock is enabled
When the USB device receives the suspend signal sent from the USB host, the USB clock enable control bit USBCKEN should be set to 0 to reduce the power consumption.

Bit 2~0 EPS2~EPS0: Endpoint FIFO selection
000: Endpoint 0 FIFO is selected
001: Endpoint 1 FIFO is selected
010: Endpoint 2 FIFO is selected
011: Endpoint 3 FIFO is selected
100: Endpoint 4 FIFO is selected
101: Endpoint 5 FIFO is selected
11x: reserved for further expansion and can not be used.
The EPS2~EPS0 bits are used to select which endpoint is to be accessed. If the selected endpoint does not exist, the related functions are not available.

AWR Register

The AWR register contains the USB device address and the Remote wake-up function control bit. The initial value of the USB device address is 00H. The address value extracted from the USB command is to be immediately loaded into this register or not depending upon the device address update control bit ASET in the SIES register.

AWR Register

Bit	7	6	5	4	3	2	1	0
Name	UAD6	UAD5	UAD4	UAD3	UAD2	UAD1	UAD0	WKEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~1 UAD6~UAD0: USB device address

Bit 0 WKEN: USB device Remote Wake-up function enable control
0: disable USB remote wake-up function
1: enable USB remote wake-up function

STALL Register

The STALL register shows whether the corresponding endpoint works properly or not. As soon as the endpoint works improperly, the related bit in the STALL register has to be set to 1 by application program. The contents of the STALL register will be cleared by USB reset signal.

STALL Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	STL5	STL4	STL3	STL2	STL1	STL0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	1	1	1	1	1	1

Bit 7~6 Unimplemented, read as “0”.

Bit 5~0 STL5~STL0: USB endpoint stall indication
0: the corresponding USB endpoint is not stalled.
1: the corresponding USB endpoint is stalled.
The STL bit is set by users when the related USB endpoint is stalled. These bits are cleared by USB reset signal. For endpoint 0 the stall bit STL0 can also be cleared by Setup Token event.

SIES Register

The SIES register is used to indicate the present signal state which the SIE receives and also control whether the SIE changes the device address automatically or not.

SIES Register

Bit	7	6	5	4	3	2	1	0
Name	NMI	—	—	—	—	—	ERR	ASET
R/W	R/W	—	—	—	—	—	R/W	R/W
POR	0	—	—	—	—	—	0	0

Bit 7 NMI: Endpoint 0 NAK token interrupt mask control
0: Endpoint 0 NAK token interrupt is not masked.
1: Endpoint 0 NAK token interrupt is masked.
If this bit is set to 1, the interrupt will not occur when the device sends a NAK token to the USB host from Endpoint 0. Otherwise, when this bit is set to 0 and the device Endpoint 0 sends a NAK token to the USB host, the Endpoint 0 NAK token interrupt will be generated if the corresponding endpoint interrupt control is enabled.

Bit 6 Unimplemented

Bit 5 Reserved.
This bit can not be changed and should be kept as 0.

Bit 4~3 Unimplemented

Bit 2 Reserved
This bit can not be changed and should be kept as 0.

Bit 1 ERR: Error indication flag during endpoint 0 FIFO is accessed
0: No error occurs during endpoint 0 FIFO is accessed.
1: Error has occurred during endpoint 0 FIFO is accessed.
The ERR bit is used to indicate that there are some errors occurred during endpoint 0 FIFO is accessed. This bit is set by SIE and should be cleared by firmware.

Bit 0 ASET: Device Address update control
0: device address is updated immediately when the AWR register is written.
1: device address is updated after the device IN token data has been read (SETUP stage finished).
The ASET bit is used to configure the SIE to automatically update the device address with the value stored in the AWR register. When this bit is set to 1 by firmware, the SIE will update the device address with the value stored in the AWR register after the USB host has successfully read the data from the device by IN token. Otherwise, when this bit is cleared to 0, the SIE will update the device address immediately after an address is written to the AWR register.

MISC Register

The MISC register contains the commands to control the desired endpoint FIFO action along with the status to show the condition of the desired endpoint FIFO. The MISC register will be cleared by a USB reset signal.

MISC Register

Bit	7	6	5	4	3	2	1	0
Name	LEN0	READY	SETCMD	—	—	CLEAR	TX	REQUEST
R/W	R/W	R	R/W	—	—	R/W	R/W	R/W
POR	0	x	1	—	—	0	0	0

"x" means unknown.

Bit 7 LEN0: zero-length packet indication flag for Endpoint 0
0: no operation.
1: a zero-length packet is sent from the USB host.
If this bit is set to 1, it indicates that a 0-sized packet is sent from a USB host. This bit should be cleared by the application program or by the next valid SETUP token.

Bit 6 READY: Endpoint FIFO Ready indication flag
0: the desired endpoint FIFO is not ready.
1: the desired endpoint FIFO is ready.
This bit is used to indicate whether the desired endpoint FIFO is ready to operate or not.

Bit 5 SETCMD: SETUP command indication flag
0: the data in the endpoint 0 FIFO is not SETUP token.
1: the data in the endpoint 0 FIFO is SETUP token.
This bit is used to indicate whether the data in the Endpoint 0 FIFO is SETUP token or not. It is set by hardware and cleared by firmware.

Bit 4~3 Unimplemented, read as "0".

Bit 2 CLEAR: clear requested FIFO
0: no operation.
1: clear the requested endpoint FIFO.
This bit is used by MCU to clear the requested FIFO, even if the FIFO is not ready. If user wants to clear the current requested Endpoint FIFO, the CLEAR bit should be set to 1 to generate a positive pulse with 2μs pulse width and then clear this bit to zero.

Bit 1 TX: Direction of data transfer between the MCU and the endpoint FIFO
0: the data transfer from the endpoint FIFO to the MCU
(MCU read data from the endpoint FIFO).
1: the data transfer from the MCU to the endpoint FIFO
(MCU write data to the endpoint FIFO).
This bit defines the direction of data transfer between the MCU and the endpoint FIFO. When the TX bit is set to high, this means that the MCU desires to write data to the endpoint FIFO. After the MCU write operation has been complete, this bit has to be cleared to zero before terminating FIFO request to indicate the end of data transfer. For a MCU read operation, this bit has to be cleared to zero to show that the MCU desires to read data from the endpoint FIFO and has to be set to high before terminating FIFO request to indicate the end of data transfer after the completion of MCU read operation.

Bit 0 REQUEST: FIFO request control
0: no operation.
1: Request the desired FIFO.
This bit is used to request the operation of the desired FIFO. After selecting the desired endpoint, the FIFO can be requested by setting this bit to high. After completion, this bit has to be cleared to zero.

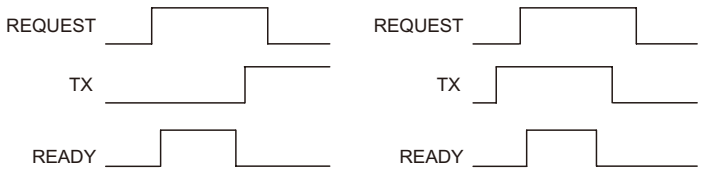
The MCU can communicate with the endpoint FIFO by setting the corresponding registers, whose addresses are listed in the following table. After reading the current data, the next data will show after 2μs, used to check the endpoint FIFO status and responds to the MISC register, if a read/write action is still being implemented.

Some timing constrains are listed here. By setting the MISC register, the MCU can perform reading, writing and clearing actions. There are some examples shown in the following for the endpoint FIFO reading, writing and clearing.

Read or Write FIFOn Table (n=0~5)

Actions	MISC Setting Flow and Status
Check whether FIFOn can be read or not	00H → 01H → delay 2μs, check 41H (ready) or 01H (not ready) → 00H.
Check whether FIFOn can be written or not	02H → 03H → delay 2μs, check 43H (ready) or 03H (not ready) → 02H.
Read FIFOn sequence	00H → 01H → delay 2μs, check 41H → read* from FIFOn register and check not ready (01H) → 03H → 02H.
Write FIFOn sequence	02H → 03H → delay 2μs, check 43H → write* to FIFOn register and check not ready (03H) → 01H → 00H.
Read 0-sized packet sequence from FIFO0	00H → 01H → delay 2μs, check 81H → clear LEN0 (01H) → 03H → 02H.
Write 0-sized packet sequence to FIFOn	02H → 03H → delay 2μs → 01H → 00H.

Note *: There are 2μs existing between 2 reading actions or between 2 writing actions.



Read FIFO Timing **Write FIFO Timing**

SETIO Register

The SETIO register is used to configure the endpoint FIFO as IN pipe or OUT pipe.

SETIO Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	SETIO5	SETIO4	SETIO3	SETIO2	SETIO1	DATATG
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	1	1	1	1	1	0

Bit 7~6 Unimplemented, read as "0".

Bit 5~1 SETIO5~SETIO1: Endpoint 5 FIFO ~ Endpoint FIFO1 pipe direction control.
0: the corresponding endpoint FIFO is configured as OUT pipe.
1: the corresponding endpoint FIFO is configured as IN pipe.
If the related SETIO bit is set to 1, the corresponding endpoint FIFO is configured as IN pipe for IN token operation. Otherwise, the corresponding endpoint FIFO is configured as OUT pipe for OUT token operation. The purpose of this function is to avoid the USB host from abnormally sending only an IN token or OUT token and disable the related endpoint.

Bit 0 DATATG: DATA0 toggle bit
0: no operation.
1: DATA0 will be sent first.
As the USB specification defined, when the USB host sends a "Set Configuration" SETUP token, the Data pipe should send the DATA0 (Data toggle) first. Therefore, when the USB device receives a "Set Configuration" SETUP token, user needs to set DATATG bit to 1 and then clear it to zero after a 2μs delay to generate a positive pulse with 2μs pulse width to make sure that the next data will send a DATA0 first.

UIC register

The UIC register is used to control the interrupt request for each endpoint. Interrupts can be enabled or disabled independently if the corresponding endpoint FIFO pipes are enabled.

UIC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	EU5I	EU4I	EU3I	EU2I	EU1I	EU0I
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as "0".

Bit 5~0 EU5I~EU0I: USB Endpoint 5 ~ Endpoint 0 interrupt control as being accessed.
0: disable the corresponding endpoint interrupt as it is accessed.
1: enable the corresponding endpoint interrupt as it is accessed.
If the related Endpoint FIFO pipe is enabled and the corresponding Endpoint interrupt is enabled, the USB interrupt for endpoint access will occur. Then a low pulse signal will be generated on $\overline{INT}$ line to get the attentions from the host MCU.

PIPE Register

The PIPE register is used to control that the FIFO pipe for each endpoint is enabled or disable. The endpoint access interrupt can be controlled independently by configuring the UIC register if the corresponding Endpoint FIFO pipe is enabled.

PIPE Register

Bit	7	6	5	4	3	2	1	0
Name	SUSPC	—	EP5E	EP4E	EP3E	EP2E	EP1E	—
R/W	R/W	—	R/W	R/W	R/W	R/W	R/W	—
POR	0	—	0	0	0	0	0	—

Bit 7 SUSPC: USB PHY control in suspend mode
0: the USB PHY is enabled.
1: the USB PHY is disabled.
If the USB enters the suspend mode, user can set SUSPC bit to 1 to disable the USB PHY for low power consumption. When the USB receives the resume signal from the USB host, the SUSPC bit should be set to 0 to make sure that the USB PHY can work normally.

Bit 6 Unimplemented, read as "0".

Bit 5~1 EP5E~EP1E: USB Endpoint 5 ~ Endpoint 0 FIFO pipe enable control.
0: the corresponding Endpoint FIFO Pipe is disabled.
1: the corresponding Endpoint FIFO Pipe is enabled.
If the corresponding Endpoint FIFO pipe is disabled, the read/write operations to the related Endpoint FIFO Pipe are not available. If the corresponding Endpoint FIFO Pipe and the interrupt are both enabled, the related USB Endpoint interrupt will be generated as the interrupt trigger events occur. Otherwise, if the Endpoint FIFO Pipe or the Endpoint interrupt is disabled, the corresponding Endpoint interrupt will not be generated.

Bit 0 Unimplemented, read as "0".

SWRST register

The SWRST register controls the software reset operation of the device. The only one available bit named RESET in the SWRST register is the device software reset control bit. When this bit is equal to "0", the device operates normally. If this bit is equal to "1", the whole device will be reset act just like power-on reset. When this situation occurs, all of the device registers and the circuitry relevant to SPI interface and USB Module will be reset. The registers in this device including the status registers and control registers will keep the POR states shown in the above USB registers summary table after the reset condition occurs.

SWRST Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	RESET
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1 Unimplemented, read as "0".

Bit 0 RESET: device software reset
0: no action
1: device reset occurs

FIFO0~FIFO5 Registers

The FIFO0~FIFO5 Registers are used for data transactions between the USB device and the USB host. The MCU reads data from or writes data to the FIFOs via the SPI interface to complete data interchange. For "Interrupt transfer" it is supported by FIFO0~FIFO2 and FIFO4, while it is supported by FIFO3 and FIFO5 for "Bulk transfer".

FIFO0~FIFO5 Registers

Label	Type	POR	MISC Setting Flow and Status
FIFO0	R/W	xxxx xxxx	Data pipe for endpoint 0, depth = 8 bytes
FIFO1	R/W	xxxx xxxx	Data pipe for endpoint 1, depth = 8 bytes
FIFO2	R/W	xxxx xxxx	Data pipe for endpoint 2, depth = 8 bytes
FIFO3	R/W	xxxx xxxx	Data pipe for endpoint 3, depth = 64 bytes
FIFO4	R/W	xxxx xxxx	Data pipe for endpoint 4, depth = 8 bytes
FIFO5	R/W	xxxx xxxx	Data pipe for endpoint 5, depth = 64 bytes

"x" means unknown.

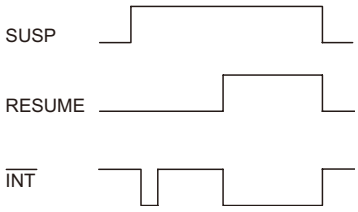
USB Module Suspend Mode and Wake-up

USB Suspend Mode

If there is no signal on the USB bus for over 3ms, the devices will go into a suspend mode. The Suspend indication bit SUSP, bit 0 of the USC register, will be set to 1 and a USB interrupt will be generated to indicate that the device should jump to the suspend state to meet the 500μA USB suspend current specification. In order to meet the 500μA suspend current, the firmware should disable the USB clock by clearing the USB clock enable control bit USBCKEN in the UCC register to 0. Also the USB PLL and PHY circuitry control bits known as PLL and SUSPC should be set to 1 to disable the USB PLL and PHY function. The suspend current is about 400μA.

USB Host Wake-up

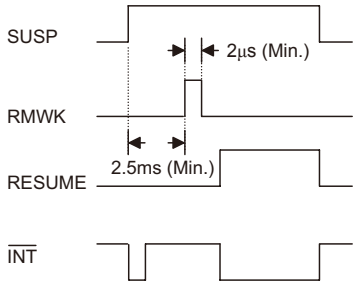
When the resume signal is asserted by the USB host, the USB device will be woken up with a USB interrupt generated on the $\overline{INT}$ line and the Resume indication bit RESUME in the USC register will be set. In order to make the device function properly, the application program must set the USBCKEN bit in the UCC register to 1 and clear the PLL and SUSPC bits in the USC register and PIPE register respectively to 0. When the resume signal is de-asserted by the USB host, the USB device actually leaves the suspend mode and the USB host will start to communicate with the USB device. The SUSP bit will be cleared as well as the RESUME bit when the USB device really leaves the suspend mode. So when the MCU is detecting the Suspend bit, the Resume bit should be stored and taken into consideration. The following diagram shows the relationship between the SUSP and RESUME bits and $\overline{INT}$ signal.



Suspend and Host Wake-up

USB Remote Wake-up

As the device has a remote wake-up function, it can wake up the USB Host by sending a wake-up pulse by setting the RMWK bit in the USC register to 1 for 2μs and then setting the RMWK bit to 0. Once the USB Host receives a wake-up signal from the device, it will send a Resume signal to the device. The timing is as follows:

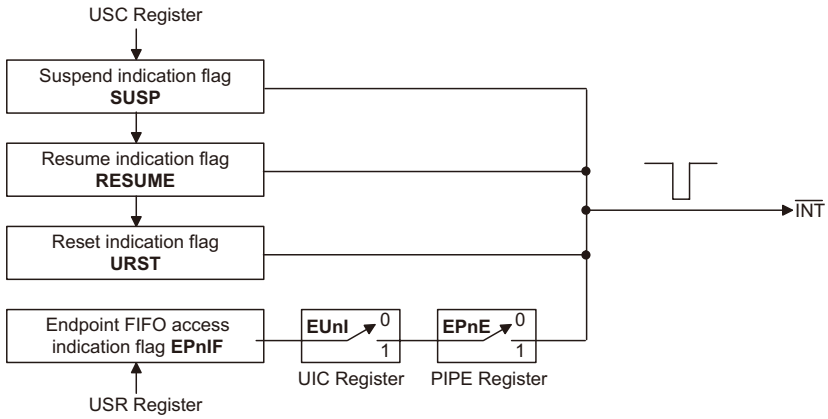


Suspend and Remote Wake-up

USB Interrupt Structure

Several individual USB conditions can generate a USB interrupt. These conditions are the USB suspended, USB resume, USB reset and USB endpoint FIFO access events. When the USB interrupt caused by any of these conditions occurs, a low pulse will be generated on the $\overline{INT}$ line to get the attention of the microcontroller or microprocessor.

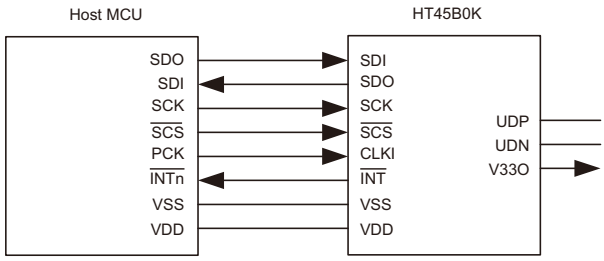
For the USB Endpoint FIFO access event, there are the corresponding indication flags to indicate which endpoint FIFO is accessed. As the Endpoint FIFO access flag is set, it will generate a USB interrupt on $\overline{INT}$ line if the associated Endpoint FIFO pipe and interrupt control are both enabled. The Endpoint FIFO access flags should be cleared by the application program. As the USB suspended, USB resume or USB reset condition occurs, the corresponding indication flag, known as SUSP, RESUME and URST bits, will be set and a USB interrupt will directly generated without any associated interrupt control being enabled. The SUSP, RESUME and URST bits are read only and set or cleared by the USB SIE.



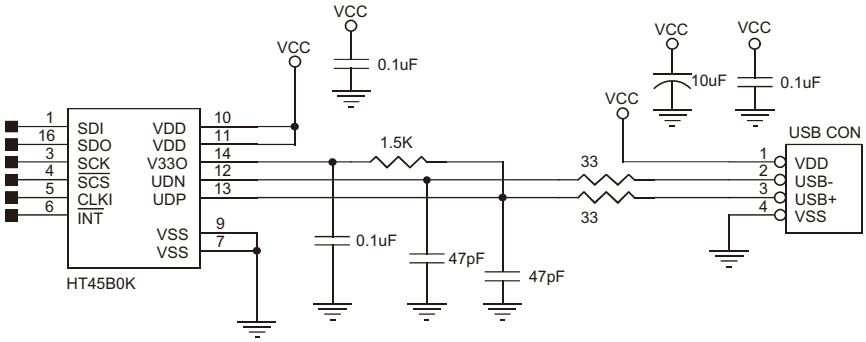
USB Interrupt Structure

Application Circuit

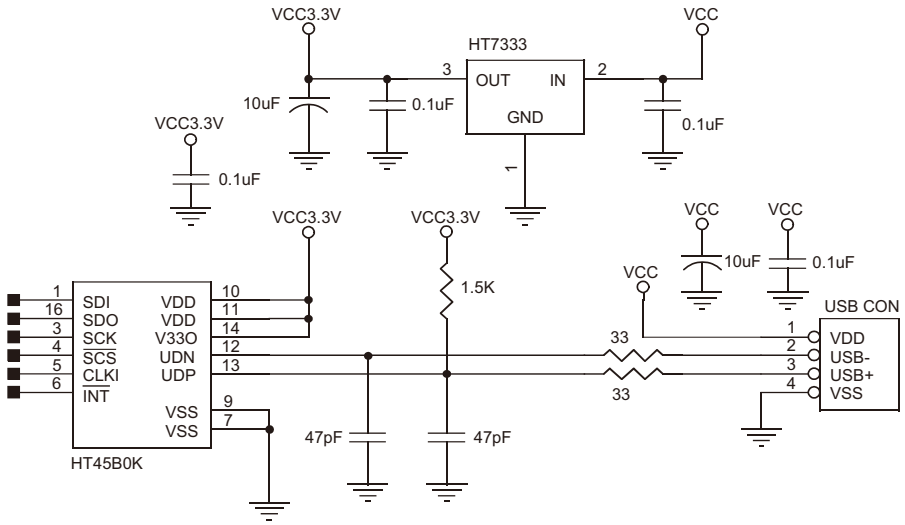
MCU Connection



USB Connection for 5V application

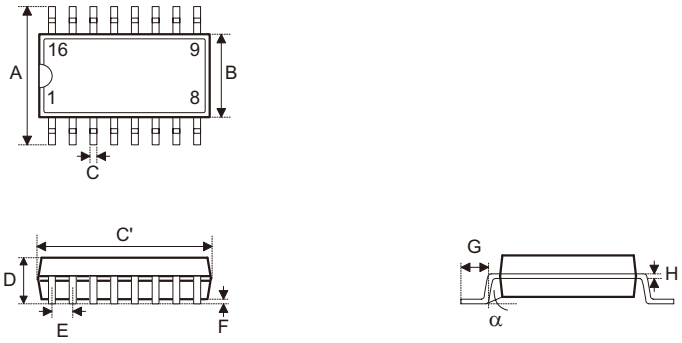


USB Connection for 3.3V application



Package Information

16-pin NSOP (150mil) Outline Dimensions

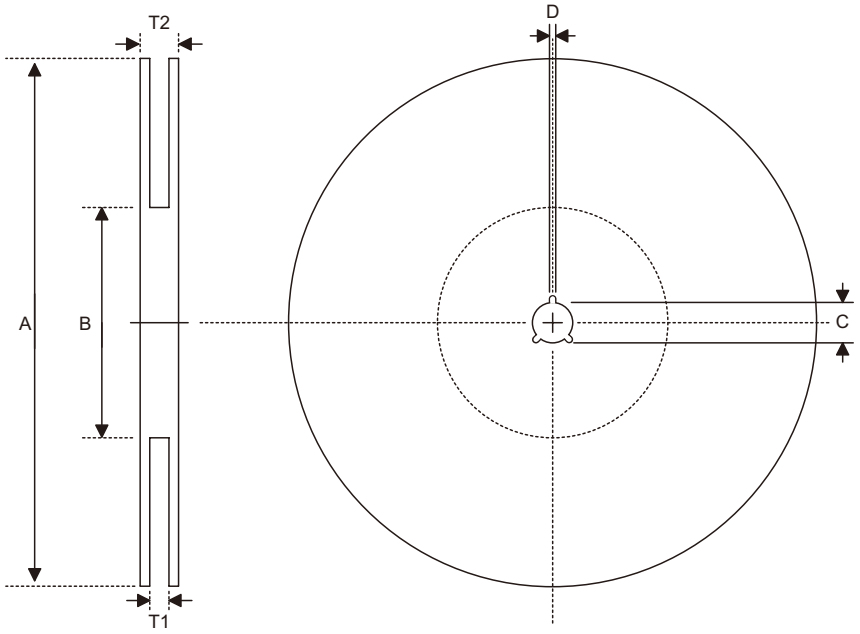


● MS-012

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.012	—	0.020
C'	0.386	—	0.394
D	—	—	0.069
E	—	0.050	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.30	—	0.51
C'	9.80	—	10.01
D	—	—	1.75
E	—	1.27	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.18	—	0.25
α	0°	—	8°

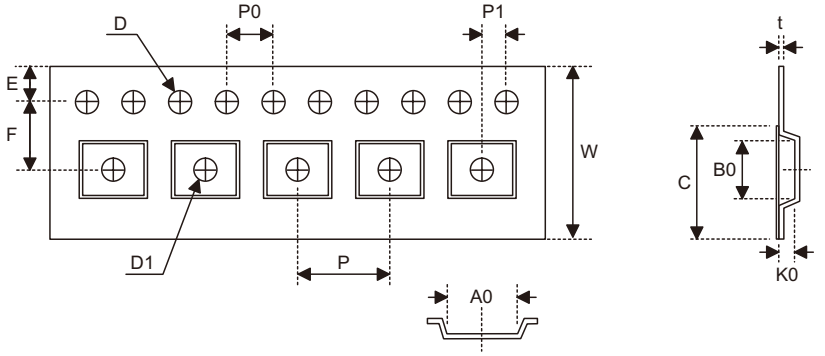
Reel Dimensions

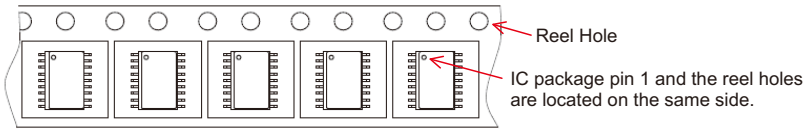


SOP 16N (150mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 +0.5/-0.2
D	Key slit Width	2.0±0.5
T1	Space Between Flange	16.8 +0.3/-0.2
T2	Reel Thickness	22.2±0.2

Carrier Tape Dimensions





Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0±0.3
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.55 +0.10/-0.00
D1	Cavity Hole Diameter	1.50 +0.25/-0.00
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.5±0.1
B0	Cavity Width	10.3±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	13.3±0.1

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