Dot Character VFD Controller & Driver

Features

- Logic voltage: 2.7V~5.5V
- High voltage: 80V (max.)
- Provides a driving segment for cursor display (48 units)
- Alphanumeric and symbolic display through built-in ROM
- 80×8-bit display RAM
- On chip ROM (5×8 dot), in total 240 characters, plus 8 user-defined characters
- Customized ROM acceptable
- Display contents:
  - 16 columns by 2 (1) rows + 32 (16) cursors
  - 20 columns by 2 (1) rows + 40 (20) cursors
  - 24 columns by 2 (1) rows + 48 (24) cursors
- Supports display output (80-segment & 24-grid)
- Supports M68 parallel data input/output (switchable 4-bit and 8-bit) i80 parallel data input/output (switchable 4-bit and 8-bit) or serial data input/output
- Built-in oscillation circuit
- 144-pin LQFP package

Applications

- Consumer products panel function control
- Industrial measuring instrument panel function control
- Other similar application panel function control

General Description

The HT16528 is a Vacuum Fluorescent Display, VFD controller/driver with dot matrix VFD display. It consists of 80 segment output lines and 24 grid output lines. It can display up to 16C×2L, 20C×2L, 24C×2L.

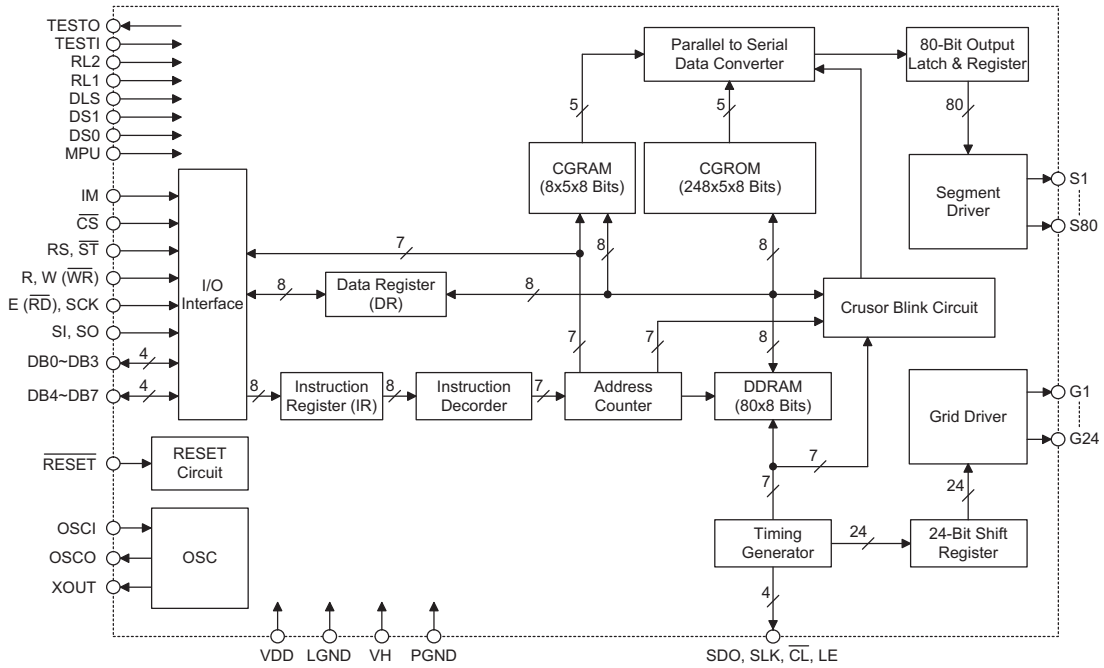
The HT16528 has a character generator ROM which stores up to 240×5×8 dot characters.

The HT16528 has serial/parallel interface. This VFD controller/driver is ideal as an MCU peripheral device.

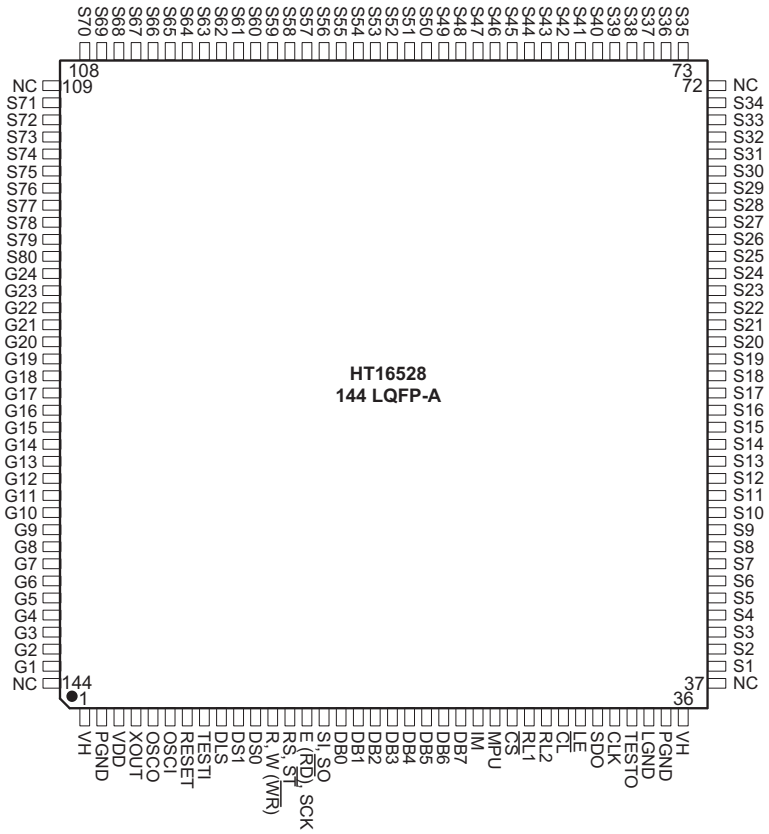
Ordering Information

Part Number	Package Information
HT16528-001	144-pin plastic LQFP (Fine pitch) (20mm×20mm), standard ROM (ROM code: 001)
HT16528-002	144-pin plastic LQFP (Fine pitch) (20mm×20mm), standard ROM (ROM code: 002)
HT16528-003	144-pin plastic LQFP (Fine pitch) (20mm×20mm), standard ROM (ROM code: 003)

Block Diagram



Pin Assignment



Pin Description

Pin Name	I/O	Description
Logic System (Microprocessor Interface)		
RS, $\overline{ST}$	I	When parallel mode is selected, this pin is utilized to select the register, either Instruction Register or Data Register. 0: IR (Instruction Register) 1: DR (Data Register) When serial mode is selected, this pin performs strobe input. Data can be set as input when this signal goes 0. During the next rising edge of this signal, command processing is performed.
E ($\overline{RD}$), SCK	I	When M68 parallel mode is selected (E), this pin is write enable. Writes data at the falling edge. When i80 parallel mode is selected (RD), this pin is read enable. When this pin is ″Low″, data is output to the data Bus. When Serial mode is selected, this pin is shift clock input, data will be written at the rising edge.
$\overline{CS}$	I	When this pin is ″Low″, the device is active.
OSCI OSCO	I O	Connected to an external resistor to generate an oscillation frequency.
XOUT	O	Oscillator signal output pin
R, W ($\overline{WR}$)	I	When M68 parallel mode is selected (R, W), this pin is data mode select pin (0: write, 1: read). When i80 parallel mode is selected ($\overline{WR}$), this pin is a write enable pin. Data will be written at rising edge signal. When serial mode is selected, connect this pin to ″Hi″ or ″Low″. Read or Write is chosen by instruction.
SI, SO	I/O	When serial mode is selected, this pin is used as I/O pin. When parallel mode is selected, this pin needs to be connected to ″Hi″ or ″Low″.
DB0~DB7	I/O	When parallel mode is selected, these pins are used as I/O pins. Data are stored sequentially, the first bit which is sent to the HT16528 is MSB. If 4 bits mode is selected, only DB4~DB7 are used.
$\overline{RESET}$	I	Initialize all the internal register and commands. All segments and digits are fixed PGND.
DS0, DS1	I	Set the duty ratio. Duty ratio will determine the number of grid. The relationship between duty ratio and these pins is shown in Table 1-1.
IM	I	Select interface mode (parallel mode or serial mode) 0: Serial mode 1: Parallel mode In parallel mode, instruction will determine the length of word.
MPU	I	Select interface mode (i80 type CPU mode or M68 type CPU mode) 0: i80 type CPU mode 1: M68 type CPU mode
DLS	I	Select number of display line when power ON reset or resetting. 0: Select 1 line (N=0), ″N″ is display line select flag in Function set command. 1: Select 2 line (N=1)
RL1, RL2	I	Set segment outputs pin assignment. The selection table is listed as Table 1-2 & Table 1-7
TESTI	I	0 or open: Normal operation mode 1: Test mode
TESTO	O	For IC testing only, leave this pin open.
Logic System (To External Extension Driver)		
SDO	O	Serial data output for extension digit driver.
SLK	O	Shift clock pulse for extension digit driver. Active during rising edge

Pin Name	I/O	Description
$\overline{CL}$	O	Clear signal for extension digit driver, active low. The digit data stored in the latch register of the extension driver are output when this signal is ″Hi″, if this signal is ″Low″, extension driver outputs are ″Low″.
LE	O	Latch enable signal for extension digit driver.
Output Pins		
G1~G24	O	High-voltage output, grid output pins.
S1~S80	O	High-voltage output, segment output pins.
Power System		
VDD	—	Pins for logic circuit
LGND	—	LGND is ground pin for logic circuit
VH	—	Power supply pins for VFD driver circuit
PGND	—	PGND is ground pin for VFD driver circuit

Table 1-1. Duty Ratio Setting

DS0	DS1	Duty Ratio
0	0	1/16 (# of grid = 16)
0	1	1/24 (# of grid = 24)
1	0	1/20 (# of grid = 20)
1	1	1/40 (# of grid = 40)*

Note: * When setting to 1/40 duty mode, use the external extension grid driver.

Table 1-2. Segment Setting: 2 Line Display (N=1)

RL1	RL2	Table No.
0	0	Table 1-3
0	1	Table 1-4
1	0	Table 1-5
1	1	Table 1-6

Table 1-3. The Number Of Segment Pins 1

No.	Name	No.	Name	No.	Name	No.	Name
1	VH	37	NC	73	S35	109	NC
2	PGND	38	S1	74	S36	110	S71
3	VDD	39	S2	75	S37	111	S72
4	XOUT	40	S3	76	S38	112	S73
5	OSCO	41	S4	77	S39	113	S74
6	OSCI	42	S5	78	S40	114	S75
7	$\overline{\text{RESET}}$	43	S6	79	S41	115	S76
8	TESTI	44	S7	80	S42	116	S77
9	DLS	45	S8	81	S43	117	S78
10	DS1	46	S9	82	S44	118	S79
11	DS0	47	S10	83	S45	119	S80
12	R, W ($\overline{\text{WR}}$)	48	S11	84	S46	120	G24
13	RS, $\overline{\text{ST}}$	49	S12	85	S47	121	G23
14	E ($\overline{\text{RD}}$), SCK	50	S13	86	S48	122	G22
15	SI, SO	51	S14	87	S49	123	G21
16	DB0	52	S15	88	S50	124	G20
17	DB1	53	S16	89	S51	125	G19
18	DB2	54	S17	90	S52	126	G18
19	DB3	55	S18	91	S53	127	G17
20	DB4	56	S19	92	S54	128	G16
21	DB5	57	S20	93	S55	129	G15
22	DB6	58	S21	94	S56	130	G14
23	DB7	59	S22	95	S57	131	G13
24	IM	60	S23	96	S58	132	G12
25	MPU	61	S24	97	S59	133	G11
26	$\overline{\text{CS}}$	62	S25	98	S60	134	G10
27	RL1	63	S26	99	S61	135	G9
28	RL2	64	S27	100	S62	136	G8
29	$\overline{\text{CL}}$	65	S28	101	S63	137	G7
30	LE	66	S29	102	S64	138	G6
31	SDO	67	S30	103	S65	139	G5
32	SLK	68	S31	104	S66	140	G4
33	TESTO	69	S32	105	S67	141	G3
34	LGND	70	S33	106	S68	142	G2
35	PGND	71	S34	107	S69	143	G1
36	VH	72	NC	108	S70	144	NC

Table 1-4. The Number Of Segment Pins 2

No.	Name	No.	Name	No.	Name	No.	Name
1	VH	37	NC	73	S6	109	NC
2	PGND	38	S40	74	S5	110	S71
3	VDD	39	S39	75	S4	111	S72
4	XOUT	40	S38	76	S3	112	S73
5	OSC	41	S37	77	S2	113	S74
6	OSCI	42	S36	78	S1	114	S75
7	$\overline{\text{RESET}}$	43	S35	79	S41	115	S76
8	TESTI	44	S34	80	S42	116	S77
9	DLS	45	S33	81	S43	117	S78
10	DS1	46	S32	82	S44	118	S79
11	DS0	47	S31	83	S45	119	S80
12	R, W ($\overline{\text{WR}}$)	48	S30	84	S46	120	G24
13	RS, $\overline{\text{ST}}$	49	S29	85	S47	121	G23
14	E ($\overline{\text{RD}}$), SCK	50	S28	86	S48	122	G22
15	SI, SO	51	S27	87	S49	123	G21
16	DB0	52	S26	88	S50	124	G20
17	DB1	53	S25	89	S51	125	G19
18	DB2	54	S24	90	S52	126	G18
19	DB3	55	S23	91	S53	127	G17
20	DB4	56	S22	92	S54	128	G16
21	DB5	57	S21	93	S55	129	G15
22	DB6	58	S20	94	S56	130	G14
23	DB7	59	S19	95	S57	131	G13
24	IM	60	S18	96	S58	132	G12
25	MPU	61	S17	97	S59	133	G11
26	$\overline{\text{CS}}$	62	S16	98	S60	134	G10
27	RL1	63	S15	99	S61	135	G9
28	RL2	64	S14	100	S62	136	G8
29	$\overline{\text{CL}}$	65	S13	101	S63	137	G7
30	LE	66	S12	102	S64	138	G6
31	SDO	67	S11	103	S65	139	G5
32	SLK	68	S10	104	S66	140	G4
33	TESTO	69	S9	105	S67	141	G3
34	LGND	70	S8	106	S68	142	G2
35	PGND	71	S7	107	S69	143	G1
36	VH	72	NC	108	S70	144	NC

Table 1-5. The Number Of Segment Pins 3

No.	Name	No.	Name	No.	Name	No.	Name
1	VH	37	NC	73	S75	109	NC
2	PGND	38	S41	74	S76	110	S10
3	VDD	39	S42	75	S77	111	S9
4	XOUT	40	S43	76	S78	112	S8
5	OSCO	41	S44	77	S79	113	S7
6	OSCI	42	S45	78	S80	114	S6
7	$\overline{\text{RESET}}$	43	S46	79	S40	115	S5
8	TESTI	44	S47	80	S39	116	S4
9	DLS	45	S48	81	S38	117	S3
10	DS1	46	S49	82	S37	118	S2
11	DS0	47	S50	83	S36	119	S1
12	R, W ($\overline{\text{WR}}$)	48	S51	84	S35	120	G24
13	RS, $\overline{\text{ST}}$	49	S52	85	S34	121	G23
14	E ($\overline{\text{RD}}$), SCK	50	S53	86	S33	122	G22
15	SI, SO	51	S54	87	S32	123	G21
16	DB0	52	S55	88	S31	124	G20
17	DB1	53	S56	89	S30	125	G19
18	DB2	54	S57	90	S29	126	G18
19	DB3	55	S58	91	S28	127	G17
20	DB4	56	S59	92	S27	128	G16
21	DB5	57	S60	93	S26	129	G15
22	DB6	58	S61	94	S25	130	G14
23	DB7	59	S62	95	S24	131	G13
24	IM	60	S63	96	S23	132	G12
25	MPU	61	S64	97	S22	133	G11
26	$\overline{\text{CS}}$	62	S65	98	S21	134	G10
27	RL1	63	S66	99	S20	135	G9
28	RL2	64	S67	100	S19	136	G8
29	$\overline{\text{CL}}$	65	S68	101	S18	137	G7
30	LE	66	S69	102	S17	138	G6
31	SDO	67	S70	103	S16	139	G5
32	SLK	68	S71	104	S15	140	G4
33	TESTO	69	S72	105	S14	141	G3
34	LGND	70	S73	106	S13	142	G2
35	PGND	71	S74	107	S12	143	G1
36	VH	72	NC	108	S11	144	NC

Table 1-6. The Number Of Segment Pins 4

No.	Name	No.	Name	No.	Name	No.	Name
1	VH	37	NC	73	S46	109	NC
2	PGND	38	S80	74	S45	110	S10
3	VDD	39	S79	75	S44	111	S9
4	XOUT	40	S78	76	S43	112	S8
5	OSCO	41	S77	77	S42	113	S7
6	OSCI	42	S76	78	S41	114	S6
7	$\overline{\text{RESET}}$	43	S75	79	S40	115	S5
8	TESTI	44	S74	80	S39	116	S4
9	DLS	45	S73	81	S38	117	S3
10	DS1	46	S72	82	S37	118	S2
11	DS0	47	S71	83	S36	119	S1
12	R, W ($\overline{\text{WR}}$)	48	S70	84	S35	120	G24
13	RS, $\overline{\text{ST}}$	49	S69	85	S34	121	G23
14	E ($\overline{\text{RD}}$), SCK	50	S68	86	S33	122	G22
15	SI, SO	51	S67	87	S32	123	G21
16	DB0	52	S66	88	S31	124	G20
17	DB1	53	S65	89	S30	125	G19
18	DB2	54	S64	90	S29	126	G18
19	DB3	55	S63	91	S28	127	G17
20	DB4	56	S62	92	S27	128	G16
21	DB5	57	S61	93	S26	129	G15
22	DB6	58	S60	94	S25	130	G14
23	DB7	59	S59	95	S24	131	G13
24	IM	60	S58	96	S23	132	G12
25	MPU	61	S57	97	S22	133	G11
26	$\overline{\text{CS}}$	62	S56	98	S21	134	G10
27	RL1	63	S55	99	S20	135	G9
28	RL2	64	S54	100	S19	136	G8
29	$\overline{\text{CL}}$	65	S53	101	S18	137	G7
30	LE	66	S52	102	S17	138	G6
31	SDO	67	S51	103	S16	139	G5
32	SLK	68	S50	104	S15	140	G4
33	TESTO	69	S49	105	S14	141	G3
34	LGND	70	S48	106	S13	142	G2
35	PGND	71	S47	107	S12	143	G1
36	VH	72	NC	108	S11	144	NC

Table 1-7. Segment Setting: 1 Line Display (N=0)

RL1	RL2	Table No.
Don't care	0	Table 1-8
Don't care	1	Table 1-9

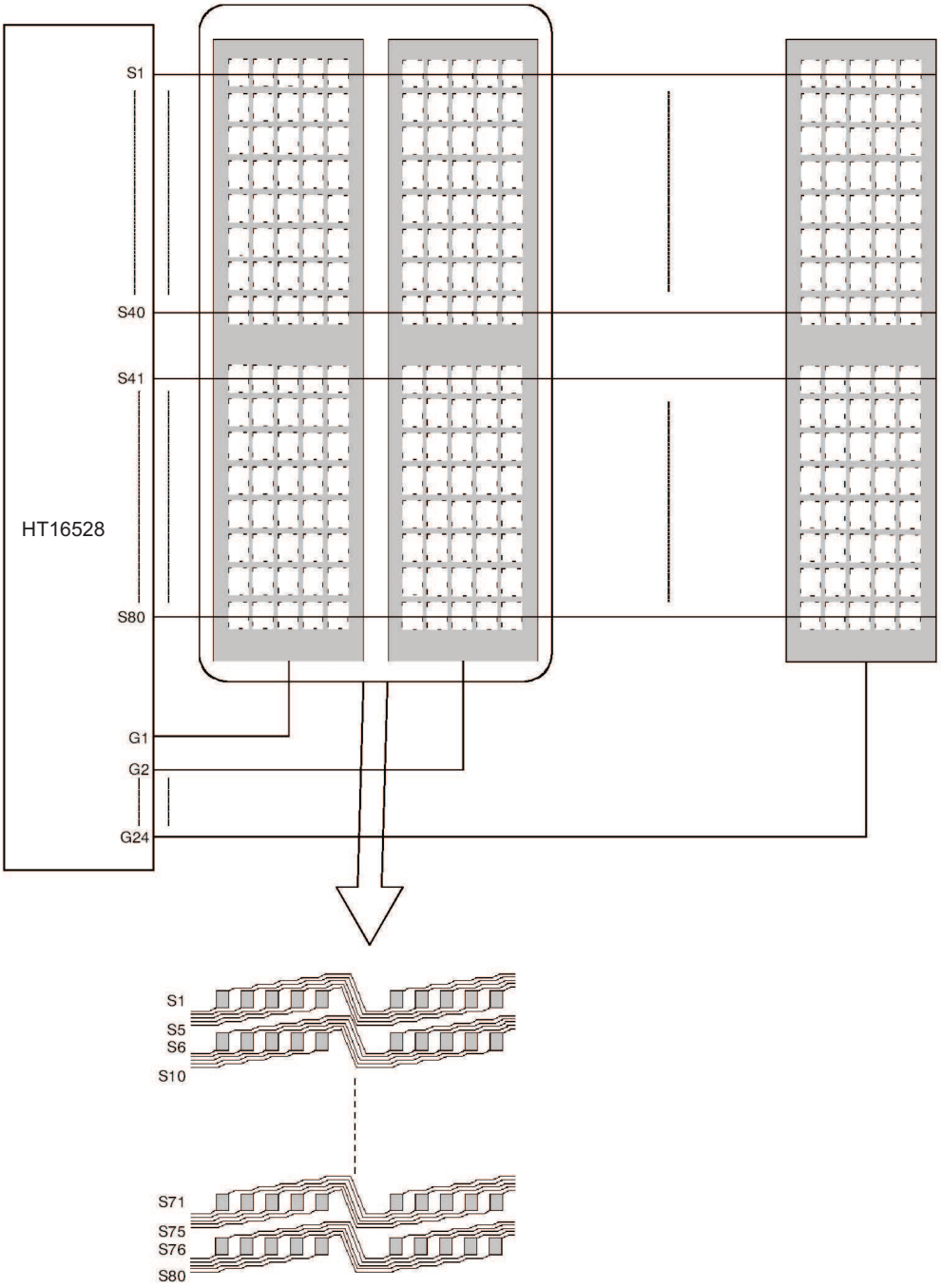
Table 1-8. The Number Of Segment Pins 5

No.	Name	No.	Name	No.	Name	No.	Name
1	VH	37	NC	73	S35	109	NC
2	PGND	38	S1	74	S36	110	Don't use
3	VDD	39	S2	75	S37	111	↓
4	XOUT	40	S3	76	S38	112	↓
5	OSCO	41	S4	77	S39	113	↓
6	OSCI	42	S5	78	S40	114	↓
7	$\overline{\text{RESET}}$	43	S6	79	Don't use	115	↓
8	TESTI	44	S7	80	↓	116	↓
9	DLS	45	S8	81	↓	117	↓
10	DS1	46	S9	82	↓	118	↓
11	DS0	47	S10	83	↓	119	↓
12	R, W ($\overline{\text{WR}}$)	48	S11	84	↓	120	G24
13	RS, $\overline{\text{ST}}$	49	S12	85	↓	121	G23
14	E ($\overline{\text{RD}}$), SCK	50	S13	86	↓	122	G22
15	SI, SO	51	S14	87	↓	123	G21
16	DB0	52	S15	88	↓	124	G20
17	DB1	53	S16	89	↓	125	G19
18	DB2	54	S17	90	↓	126	G18
19	DB3	55	S18	91	↓	127	G17
20	DB4	56	S19	92	↓	128	G16
21	DB5	57	S20	93	↓	129	G15
22	DB6	58	S21	94	↓	130	G14
23	DB7	59	S22	95	↓	131	G13
24	IM	60	S23	96	↓	132	G12
25	MPU	61	S24	97	↓	133	G11
26	$\overline{\text{CS}}$	62	S25	98	↓	134	G10
27	RL1	63	S26	99	↓	135	G9
28	RL2	64	S27	100	↓	136	G8
29	$\overline{\text{CL}}$	65	S28	101	↓	137	G7
30	LE	66	S29	102	↓	138	G6
31	SDO	67	S30	103	↓	139	G5
32	SLK	68	S31	104	↓	140	G4
33	TESTO	69	S32	105	↓	141	G3
34	LGND	70	S33	106	↓	142	G2
35	PGND	71	S34	107	↓	143	G1
36	VH	72	NC	108	↓	144	NC

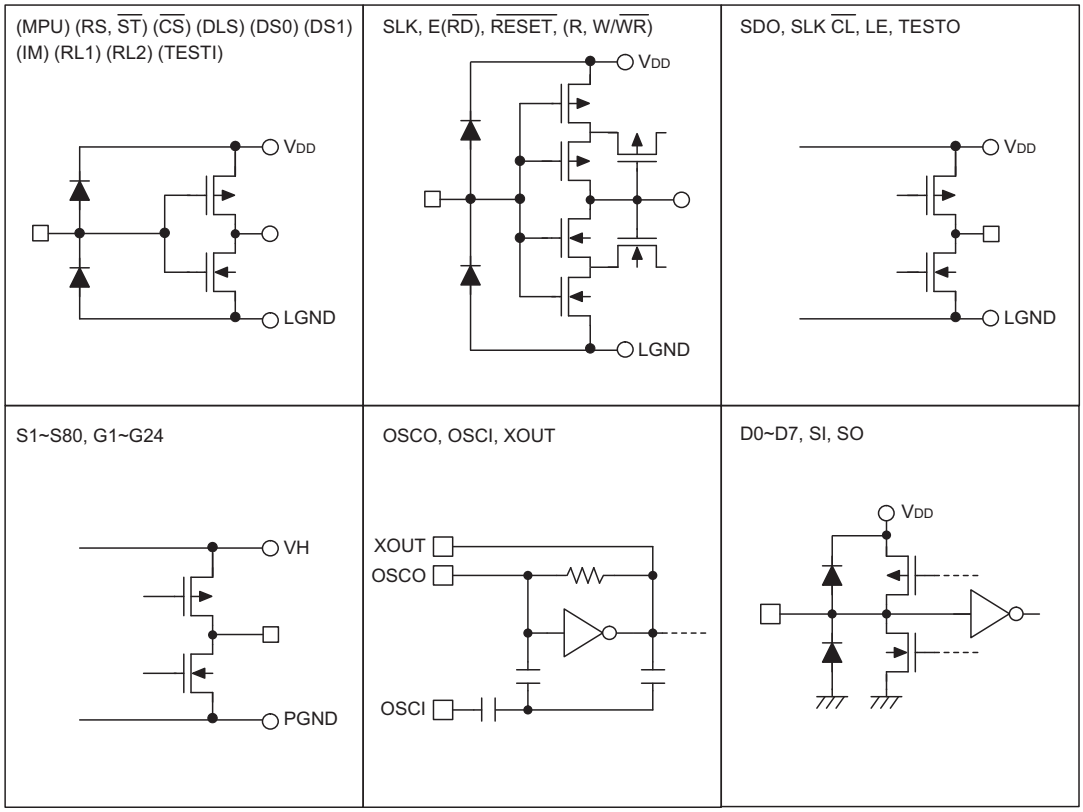
Table 1-9. The Number Of Segment Pins 6

No.	Name	No.	Name	No.	Name	No.	Name
1	VH	37	NC	73	S6	109	NC
2	PGND	38	S40	74	S5	110	Don't use
3	VDD	39	S39	75	S4	111	↓
4	XOUT	40	S38	76	S3	112	↓
5	OSCO	41	S37	77	S2	113	↓
6	OSCI	42	S36	78	S1	114	↓
7	$\overline{\text{RESET}}$	43	S35	79	Don't use	115	↓
8	TESTI	44	S34	80	↓	116	↓
9	DLS	45	S33	81	↓	117	↓
10	DS1	46	S32	82	↓	118	↓
11	DS0	47	S31	83	↓	119	↓
12	R, W ($\overline{\text{WR}}$)	48	S30	84	↓	120	G24
13	RS, $\overline{\text{ST}}$	49	S29	85	↓	121	G23
14	E ($\overline{\text{RD}}$), SCK	50	S28	86	↓	122	G22
15	SI, SO	51	S27	87	↓	123	G21
16	DB0	52	S26	88	↓	124	G20
17	DB1	53	S25	89	↓	125	G19
18	DB2	54	S24	90	↓	126	G18
19	DB3	55	S23	91	↓	127	G17
20	DB4	56	S22	92	↓	128	G16
21	DB5	57	S21	93	↓	129	G15
22	DB6	58	S20	94	↓	130	G14
23	DB7	59	S19	95	↓	131	G13
24	IM	60	S18	96	↓	132	G12
25	MPU	61	S17	97	↓	133	G11
26	$\overline{\text{CS}}$	62	S16	98	↓	134	G10
27	RL1	63	S15	99	↓	135	G9
28	RL2	64	S14	100	↓	136	G8
29	$\overline{\text{CL}}$	65	S13	101	↓	137	G7
30	LE	66	S12	102	↓	138	G6
31	SDO	67	S11	103	↓	139	G5
32	SLK	68	S10	104	↓	140	G4
33	TESTO	69	S9	105	↓	141	G3
34	LGND	70	S8	106	↓	142	G2
35	PGND	71	S7	107	↓	143	G1
36	VH	72	NC	108	↓	144	NC

HT16528 Connect to VFD as Below Figure



Approximate Internal Connections



Absolute Maximum Ratings

Logic Supply Voltage .....V_{SS}–0.3V to V_{SS}+6.0V

Input Voltage.....V_{SS}–0.3V to V_{DD}+0.3V

Driver Output Voltage.....V_{SS}–0.3V to V_H

Driver Output Current (Total) .....500 (Est.) mA

Operating Temperature.....–40°C to 85°C

Driver Supply Voltage .....V_{SS}–0.3V to V_{SS}+88V

Output Voltage.....V_{SS}–0.3V to V_{DD}+0.3V

Driver Output Current .....±50mA

Storage Temperature .....–55°C to 125°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Unless otherwise specified, V_H=50V, V_{SS}=V_{LGND}=V_{PGND}=0V, Ta=–40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Logic Supply Voltage	—	—	2.7	5.0	5.5	V
V_H	VFD Supply Voltage	—	—	20	—	80	V
I_{DD}	Operating Current	2.7V~5.5V	No load, CPU Non-access	—	—	1000	μA
I_H	Operating Current	2.7V~5.5V	No load	—	—	500	μA
I_{LOH}	Hi-level Leakage Current	2.7V~5.5V	Logic except DB0~DB7, SI, SO, $V_{IN/OUT}$=V_{DD}	—	—	1	μA
I_{LOL}	Hi-level Leakage Current	2.7V~5.5V	Logic $V_{IN/OUT}$=V_{SS}	—	—	–1	μA
I_{IH}	Hi-level Input Current	2.7V~5.5V	TEST, V_{IN}=V_{DD}	5	—	500	μA
I_P	Pull-up MOS Current	2.7V~5.5V	DB0~DB7, SI, SO	5	125	280	μA
V_{IH1}	"H" Input Voltage 1	—	Except E, SCK, $\overline{\text{RESET}}$, R, W ($\overline{\text{WR}}$)	0.7V_{DD}	—	V_{DD}	V
V_{IL1}	"L" Input Voltage 1	—	Except E,SCK, $\overline{\text{RESET}}$, R, W ($\overline{\text{WR}}$)	0	—	0.3V_{DD}	V
V_{IH2}	"H" Input Voltage 2	—	E, SCK, $\overline{\text{RESET}}$, R, W ($\overline{\text{WR}}$)	0.8V_{DD}	—	V_{DD}	V
V_{IL2}	"L" Input Voltage 2	—	E, SCK, $\overline{\text{RESET}}$, R ,W ($\overline{\text{WR}}$)	0	—	0.2V_{DD}	V
V_{OH1}	Hi-level Output Voltage	2.7V~5.5V	DB0~DB7, SI,SO, SDO, SLK, LE, $\overline{\text{CL}}$, I_{OL1}= –0.1mA	V_{DD}–0.5	—	V_{DD}	V
V_{OL1}	Low-level Output Voltage	2.7V~5.5V	DB0~DB7, SI,SO, SDO, SLK, LE, $\overline{\text{CL}}$, I_{OL1}= 0.1mA	0	—	V_{SS}+0.5	V
V_{OH21}	Hi-level Output Voltage	2.7V~5.5V	S1~S80, I_{OH2}= –0.5mA	48	—	—	V
V_{OH22}			S1~S80, I_{OH2}= –1mA	46	—	—	V
V_{OH2G}			G1~G24, I_{OH2}= –15mA	45	—	—	V
V_{OL2}	Low-level Output Voltage	2.7V~5.5V	S1~S80, G1~G24, I_{OL2}= 1mA	—	—	5	V

A.C. Characteristics

Unless otherwise specified, V_H=50V, V_{SS}=V_{LGND}=V_{PGND}=0V, Ta=–40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{OSC}	Oscillation Frequency	2.7V~5.5V	R_{OSC}=56kΩ	392	560	728	kHz
f_C	Oscillation Frequency	2.7V~5.5V	OSCI external clock	350	560	750	kHz
t_{R1}	Rise Time	2.7V~5.5V	C_L= 50pF, S1~S80	—	—	2.5	μs
t_{R2}		2.7V~5.5V	C_L=50pF, G1~G24	—	—	0.25	μs
t_F	Fall Time	2.7V~5.5V	C_L= 50pF, S1~S80, G1~G24	—	—	2	μs

Switching Timing

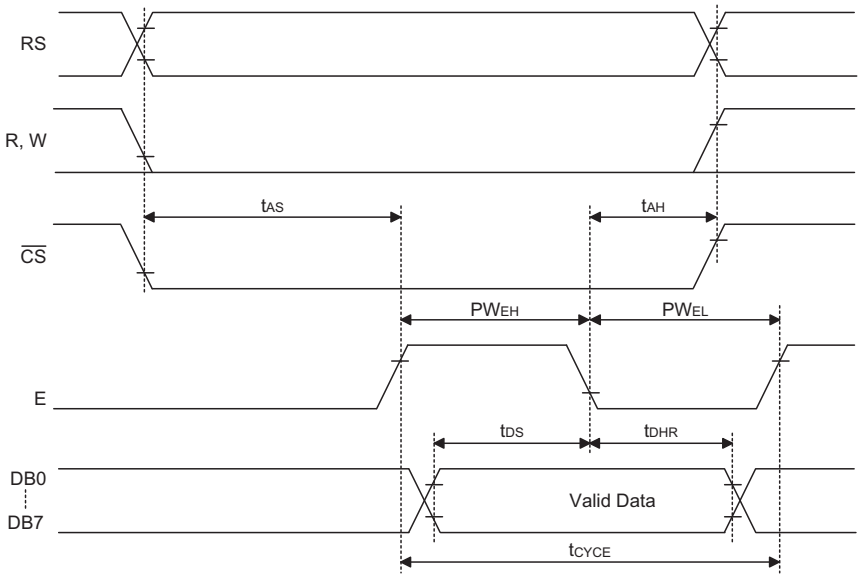
Timing Conditions 1 for M68-Type for Parallel Mode, Write Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{CYCLE}	Enable Cycle Time	4.5V~5.5V	E↑ → E↑	500	—	—	ns
		2.7V~4.5V		1000	—	—	ns
PW_{EH}	Enable Pulse Width High	4.5V~5.5V	E	230	—	—	ns
		2.7V~4.5V		450	—	—	ns
PW_{EL}	Enable Pulse Width Low	4.5V~5.5V	E	230	—	—	ns
		2.7V~4.5V		450	—	—	ns
t_{AS}	((RS), (R, W), ($\overline{CS}$)) — (E) Setup Time	4.5V~5.5V	RS, R, W, CS → E↑	20	—	—	ns
		2.7V~4.5V		60	—	—	ns
t_{AH}	((RS), (R, W)) — (E) Hold Time	4.5V~5.5V	E↓ → RS, R, W	10	—	—	ns
		2.7V~4.5V		20	—	—	ns
t_{CH}	($\overline{CS}$) — (E) Hold Time	4.5V~5.5V	E↓ → CS	20	—	—	ns
		2.7V~4.5V		40	—	—	ns
t_{DS}	Write Data Setup Time	4.5V~5.5V	Data → E↑	80	—	—	ns
		2.7V~4.5V		195	—	—	ns
t_{DH}	Write Data Hold Time	4.5V~5.5V	E↓ → Data	10	—	—	ns
		2.7V~4.5V		10	—	—	ns
t_{WRE}	Reset Pulse Width	4.5V~5.5V	—	500	—	—	ns
		2.7V~4.5V		500	—	—	ns

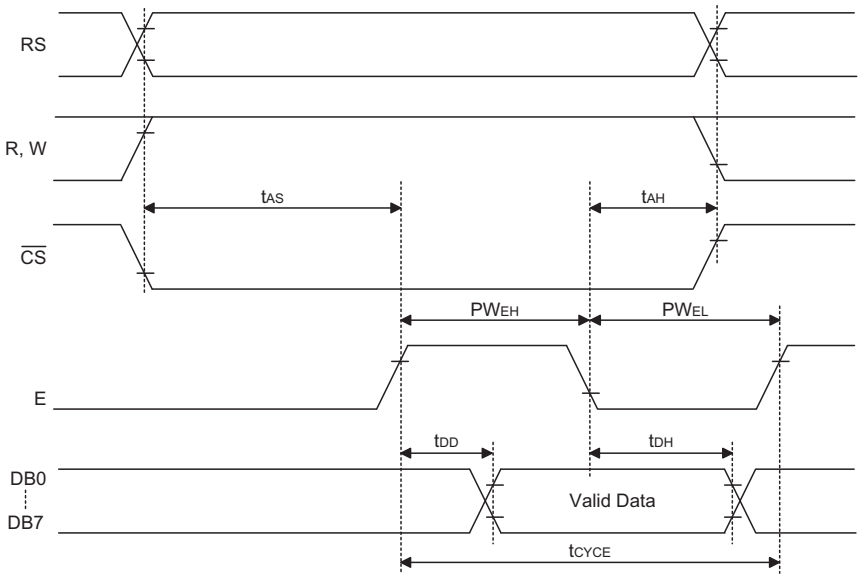
M68-Type for Parallel Mode, Read Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{CYCLE}	Enable Cycle Time	4.5V~5.5V	E↑ → E↑	500	—	—	ns
		2.7V~4.5V		1000	—	—	ns
PW_{EH}	Enable Pulse Width High	4.5V~5.5V	E	230	—	—	ns
		2.7V~4.5V		450	—	—	ns
PW_{EL}	Enable Pulse Width Low	4.5V~5.5V	E	230	—	—	ns
		2.7V~4.5V		450	—	—	ns
t_{AS}	((RS), (R, W), ($\overline{CS}$)) — (E) Setup Time	4.5V~5.5V	RS, R, W, CS → E↑	20	—	—	ns
		2.7V~4.5V		60	—	—	ns
t_{AH}	((RS), (R, W)) — (E) Hold Time	4.5V~5.5V	E↓ → RS, R, W	10	—	—	ns
		2.7V~4.5V		30	—	—	ns
t_{CH}	($\overline{CS}$) — (E) Hold Time	4.5V~5.5V	E↓ → CS	20	—	—	ns
		2.7V~4.5V		40	—	—	ns
t_{DD}	Read Data Setup Time	4.5V~5.5V	Data → E↑	—	—	160	ns
		2.7V~4.5V		—	—	360	ns
t_{DHr}	Read Data Hold Time	4.5V~5.5V	E↓ → Data	5	—	—	ns
		2.7V~4.5V		5	—	—	ns

Parallel Mode (M68 Input)



Parallel Mode (M68 Output)



Note: The input signal rising time and falling time (t_f, t_r) is specified at 15ns or less.

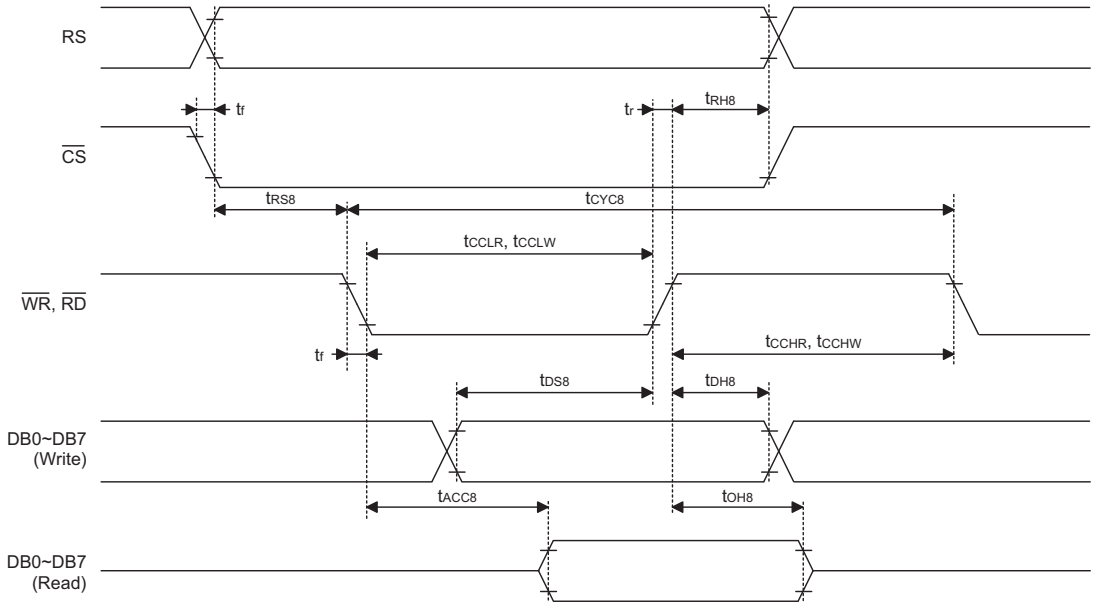
All timing is specified using 20% and 80% of V_{DD} as the reference.

PW_{EH} is specified as the overlap between $\overline{CS}$ being L and E.

Timing Conditions 2 for i80-Type, Parallel Mode Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{RH8}	RS Hold Time	4.5V~5.5V	RS	10	—	—	ns
		2.7V~4.5V		20	—	—	ns
t_{CH8}	$\overline{CS}$ Hold Time	4.5V~5.5V	$\overline{CS}$	20	—	—	ns
		2.7V~4.5V		40	—	—	ns
t_{RS8}	RS, $\overline{CS}$ Setup Time	4.5V~5.5V	RS, $\overline{CS}$	10	—	—	ns
		2.7V~4.5V		30	—	—	ns
t_{CYC8}	System Cycle Time	4.5V~5.5V	—	200	—	—	ns
		2.7V~4.5V		600	—	—	ns
t_{CCLW}	Control "L" Pulse Width ($\overline{WR}$)	4.5V~5.5V	$\overline{WR}$	30	—	—	ns
		2.7V~4.5V		50	—	—	ns
t_{CCLR}	Control "L" Pulse Width ($\overline{RD}$)	4.5V~5.5V	$\overline{RD}$	70	—	—	ns
		2.7V~4.5V		200	—	—	ns
t_{CCHW}	Control "H" Pulse Width ($\overline{WR}$)	4.5V~5.5V	$\overline{WR}$	100	—	—	ns
		2.7V~4.5V		200	—	—	ns
t_{CCHR}	Control "H" Pulse Width ($\overline{RD}$)	4.5V~5.5V	$\overline{RD}$	100	—	—	ns
		2.7V~4.5V		200	—	—	ns
t_{DS8}	Data Setup Time	4.5V~5.5V	DB0~DB7	30	—	—	ns
		2.7V~4.5V		60	—	—	ns
t_{DH8}	Data Hold Time	4.5V~5.5V	DB0~DB7	10	—	—	ns
		2.7V~4.5V		20	—	—	ns
t_{ACC8}	RD Access Time	4.5V~5.5V	DB0~DB7, C_L=100pF	—	—	70	ns
		2.7V~4.5V		—	—	140	ns
t_{OH8}	Output Disable Time	4.5V~5.5V	DB0~DB7, C_L=100pF	5	—	—	ns
		2.7V~4.5V		5	—	—	ns
t_{WRE}	Reset Pulse Width	4.5V~5.5V	—	500	—	—	ns
		2.7V~4.5V		500	—	—	ns

Parallel Mode (i80)



Note: The input signal rising time and falling time (t_f, t_r) is specified at 15ns or less.

All timing is specified using 20% and 80% of V_{DD} as the reference.

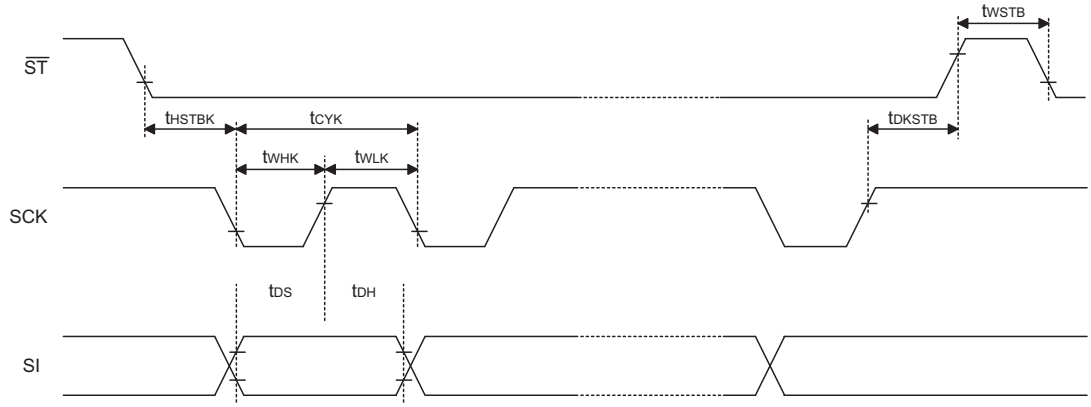
t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS}$ as L and $\overline{WR}$ and $\overline{RD}$ at the L level.

Timing Conditions 3 for Serial Mode Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{CYK}	Shift Clock Cycle	4.5V~5.5V	SCK	500	—	—	ns
		2.7V~4.5V		1000	—	—	ns
t_{WHK}	High-level Shift Clock Pulse Width	4.5V~5.5V	SCK	200	—	—	ns
		2.7V~4.5V		300	—	—	ns
t_{WLK}	Low-level Shift Clock Pulse Width	4.5V~5.5V	SCK	200	—	—	ns
		2.7V~4.5V		300	—	—	ns
t_{HSTBK}	Shift Clock Hold Time	4.5V~5.5V	STD↓ → SCK↓	100	—	—	ns
		2.7V~4.5V		150	—	—	ns
t_{DS}	Data Setup Time	4.5V~5.5V	Data → SCK↑	100	—	—	ns
		2.7V~4.5V		150	—	—	ns
t_{DK}	Data Hold Time	4.5V~5.5V	SCK↑ → Data	100	—	—	ns
		2.7V~4.5V		150	—	—	ns
t_{DKSTB}	$\overline{ST}$ Hold Time	4.5V~5.5V	SCK↑ → $\overline{ST}$↑	500	—	—	ns
		2.7V~4.5V		750	—	—	ns
t_{WSTB}	$\overline{ST}$ Pulse Width	4.5V~5.5V	—	500	—	—	ns
		2.7V~4.5V		750	—	—	ns
t_{WAIT}	Wait Time	4.5V~5.5V	8th CLK↑ → 1st CLK↓	1	—	—	μs
		2.7V~4.5V		1	—	—	μs
t_{ODO}	Output Data Delay Time	4.5V~5.5V	ST↓ → Data	—	—	150	ns
		2.7V~4.5V		—	—	300	ns

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{ODH}	Output Data Hold Time	4.5V~5.5V	SCK↑ → Data	5	—	—	ns
		2.7V~4.5V		5	—	—	ns
t_{WRE}	Reset Pulse Width	4.5V~5.5V	—	500	—	—	ns
		2.7V~4.5V		500	—	—	ns

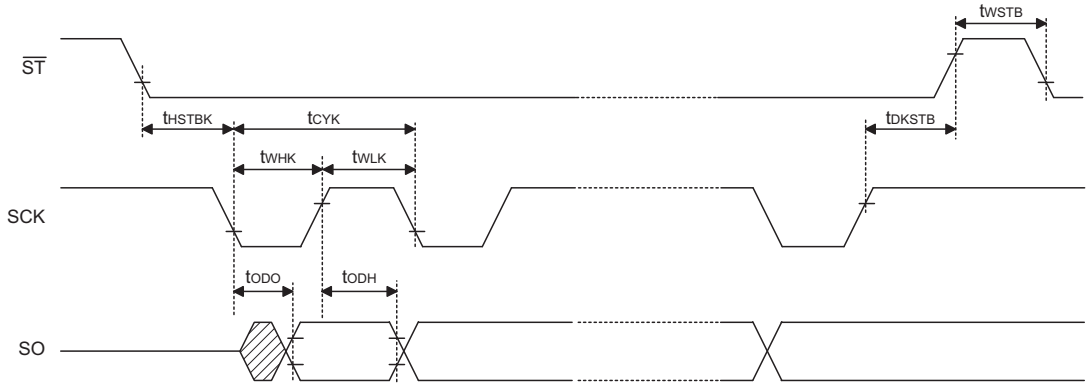
Serial Mode (Input)



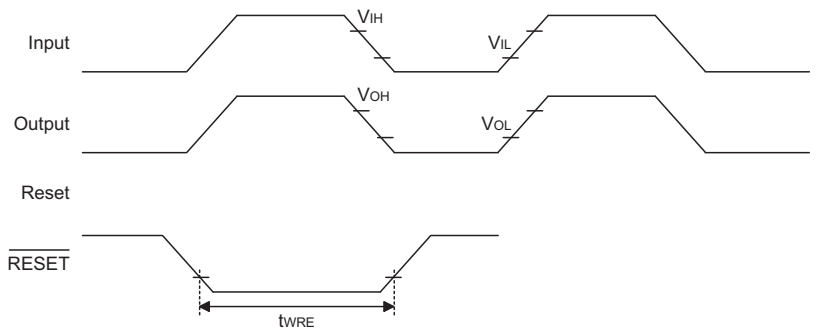
Note: The input rise time and fall time (t_R, t_F) is specified at 15ns or less.

All timing is specified using 20% and 80% of V_{DD} as the reference.

Serial Mode (Output)

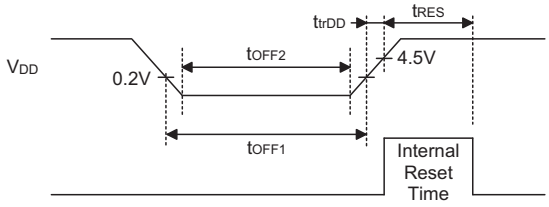


AC Measurement Point



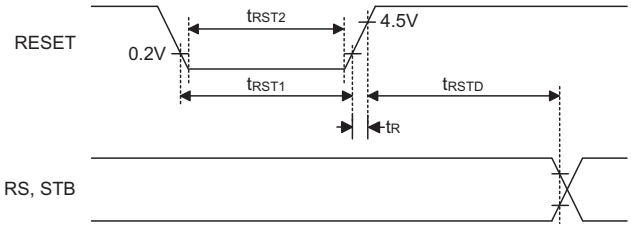
Timing Condition for interface: M68, i80 and Serial Power On Reset Ta=25°C

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit
t_{RES}	Resetting Time	2.7V~5.5V	100	—	—	μs
t_{trDD}	VDD Rising Time	2.7V~5.5V	1	—	—	μs
t_{OFF1}	VDD OFF Width	2.7V~5.5V	1	—	—	ms
t_{OFF2}	VDD OFF Width	2.7V~5.5V	500	—	—	ns



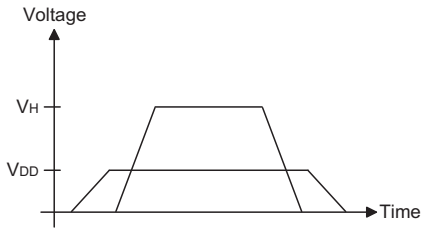
RESET Timing

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit
t_{RSTD}	Delay Time After Reset	2.7V~5.5V	100	—	—	μs
t_R	Reset Rising Time	2.7V~5.5V	1	—	—	μs
t_{RST1}	RST/Pulse Width Low	2.7V~5.5V	1	—	—	ms
t_{RST2}	RST/Pulse Width Low	2.7V~5.5V	500	—	—	ns



Power Supply Connection Sequence

- Connect the PGND and LGND externally to have an equal potential voltage
- To avoid faulty connection, turn on the driver power supply (V_H) after turning on the logic power supply (V_{DD}). Then turn off the logic power supply (V_{DD}) after turning off the driver power supply (V_H).
- If the power connection sequence recommended by Holtek is not followed, there's a possibility that the internal logic transistors may be damaged.



Functional Description

CPU Interface

HT16528 have 4 or 8-bit parallel interface or serial interface. These modes are selected by IM pin.

- IM=″0″: Serial mode
- IM=″1″: Parallel mode

CPU Interface Table							
IM	$\overline{CS}$	RS, $\overline{ST}$	E ($\overline{RD}$), SCK	R, W ($\overline{WR}$)	MPU	SI, SO	DB0~DB7
0	$\overline{CS}$	$\overline{ST}$	SCK	Note	Note	SI, SO	Note
1	$\overline{CS}$	RS	E ($\overline{RD}$)	R, W ($\overline{WR}$)	MPU	Note	DB0~DB7

Note: Keep this pin Hi or Lo.

Registers (IR, DR)

The HT16528 has two 8-bit registers, namely, an instruction register (IR) and a data register (DR). The IR register stores instruction code such as display clear and cursor shift. It also contains address information for display data RAM (DDRAM) and character generator RAM (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written into or read from the DDRAM or CGRAM. Data written into the DR from the MPU is automatically written into the DDRAM or CGRAM by internal operation. The DR is also used for data storage when reading data from the DDRAM or CGRAM. When the address information is written into the IR, data is read and then stored into the DR from the DDRAM or CGRAM by internal operation. Data transfer between the MPU is completed when the MPU reads the DR. After the read, data in DDRAM or CGRAM at the next address is sent to the DR for the next read from the MPU. These two registers can be selected by the register selector (RS) signal, (Refer to CPU Interface table).

Registers (IR, DR) Table				
Common	M68	i80		Register Selection
RS	R, W	$\overline{RD}$	$\overline{WR}$	
0	0	1	0	Write IR data during internal operation (display clear, etc.)
0	1	0	1	Read data to be busy flag (DB7) and address counter (DB6~DB0)
1	0	1	0	Write DR data (DR→DDRAM, CGRAM)
1	1	0	1	Read DR data (DDRAM, CGRAM→DR)

Busy Flag (Read BF Flag)

Busy flag data (DB7) is always output as ″0″.

Address Counter (AC)

The Address counter (AC) assigns address to both DDRAM and CGRAM. When an instruction address is written into the IR, the address information is sent from the IR to the AC.

Selection of either DDRAM or CGRAM is also determined concurrently by the instruction. After writing into (or read from) the DDRAM or CGRAM, the AC is automatically incremented by 1 (or decremented by 1). The cursor position are then output to DB0~DB6 when RS=0 and R, W=1 (Refer to Registers (IR, DR) Table).

Display Data RAM (DDRAM)

The Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. The area in the DDRAM that is not used for display can be used as general data RAM. Refer to DDRAM address table for the relationships between DDRAM address and positions on the VFD.

The DDRAM address (ADD) is set in the address counter (AC) as hexadecimal.

DDRAM Address Table						
High Order Bits			Low Order Bits			
AC6	AC5	AC4	AC3	AC2	AC1	AC0
Hexadecimal			Hexadecimal			

Example: DDRAM address ″3FH″

0	1	1	1	1	1	1
3			F			

- 1-line display (N=0)

Display Position

(Digit)	1	2	3	4	5	6		79	80
DDRAM Address (Hexadecimal)	00	01	02	03	04	05		4E	4F

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only one HT16528, 24 characters are displayed. When display shift operation is performed, the DDRAMaddress shifts as shown in the following table.

Example: 1-line by 24-character Display Table

Display Position

(Digit)	1	2	3	4	5	6		23	24
DDRAM Address (Hexadecimal)	00	01	02	03	04	05		16	17
For Shift Left	01	02	03	04	05	06		17	18
For Shift Right	4F	00	01	02	03	04		15	16

- 2-line display (N=1)

Display Position

(Digit)	1	2	3	4	5	6		39	40
DDRAM Address	00	01	02	03	04	05		26	27
(Hexadecimal)	40	41	42	43	44	45		66	67

When the number of display character is less than 40×2 lines, the 2 lines are displayed from the head. The first line end address and the second line start address are not consecutive.
For example, if using only one HT16528, 24 characters × 2 lines are displayed. When display shift operation is performed, the DDRAM address shifts as shown in the following table.

Example: 2-line by 24-character Display Table

Display Position

(Digit)	1	2	3	4	5	6		23	24
DDRAM Address	00	01	02	03	04	05		16	17
(Hexadecimal)	40	41	42	43	44	45		56	57
For Shift Left	01	02	03	04	05	06		17	18
	41	42	43	44	45	46		57	58
For Shift Right	27	00	01	02	03	04		15	16
	67	40	41	42	43	44		55	56

- 40 Characters×2 line display

The DDRAM stores the character code of each character being displayed on the VFD. Valid DDRAMaddresses are 00H to 27H and 40H to 67H. The DDRAMnot used for display characters can be used as general purpose RAM. The tables below show the relationship between the DDRAMaddress and the character position on the VFD display shift as shown in the following table.

Example: 2-line by 40-character Display Table

Display Position

(Digit)	1	2	3	4		23	24	25		39	40
DDRAM Address	00	01	02	03		16	17	18		26	27
(Hexadecimal)	40	41	42	43		56	57	58		66	67
For Shift Left	01	02	03	04		17	18	19		27	00
	41	42	43	44		57	58	59		67	40
For Shift Right	27	00	01	02		15	16	17		25	26
	67	40	41	42		55	56	57		65	66
	HT16528 Display							Extension Driver Display			

- Character Generator ROM (CGROM)
  - CGROM for generating character patterns of 5×8 dots from 8-bit character codes, generates 240 type of character patterns.
  - The character codes are shown on the following page.
  - Character codes 00H to 0FH are allocated to the CGRAM

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0 (CGRAM)															
0001	RAM1 (CGRAM)															
0010	RAM2 (CGRAM)															
0011	RAM3 (CGRAM)															
0100	RAM4 (CGRAM)															
0101	RAM5 (CGRAM)															
0110	RAM6 (CGRAM)															
0111	RAM7 (CGRAM)															
1000	RAM8 (CGRAM)															
1001	RAM9 (CGRAM)															
1010	RAMA (CGRAM)															
1011	RAMB (CGRAM)															
1100	RAMC (CGRAM)															
1101	RAMD (CGRAM)															
1110	RAME (CGRAM)															
1111	RAMF (CGRAM)															

Character Code Table 1 (ROM Code: 001)

LSB \ MSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0 (CGRAM)															
0001	RAM1 (CGRAM)															
0010	RAM2 (CGRAM)															
0011	RAM3 (CGRAM)															
0100	RAM4 (CGRAM)															
0101	RAM5 (CGRAM)															
0110	RAM6 (CGRAM)															
0111	RAM7 (CGRAM)															
1000	RAM8 (CGRAM)															
1001	RAM9 (CGRAM)															
1010	RAMA (CGRAM)															
1011	RAMB (CGRAM)															
1100	RAMC (CGRAM)															
1101	RAMD (CGRAM)															
1110	RAME (CGRAM)															
1111	RAMF (CGRAM)															

Character Code Table 2 (ROM Code: 002)

LSB \ MSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0 (CGRAM)															
0001	RAM1 (CGRAM)															
0010	RAM2 (CGRAM)															
0011	RAM3 (CGRAM)															
0100	RAM4 (CGRAM)															
0101	RAM5 (CGRAM)															
0110	RAM6 (CGRAM)															
0111	RAM7 (CGRAM)															
1000	RAM8 (CGRAM)															
1001	RAM9 (CGRAM)															
1010	RAMA (CGRAM)															
1011	RAMB (CGRAM)															
1100	RAMC (CGRAM)															
1101	RAMD (CGRAM)															
1110	RAME (CGRAM)															
1111	RAMF (CGRAM)															

Character Code Table 3 (ROM code: 003)

Character Generator RAM (CGRAM)

The CGRAM stores the pixel information (1=pixel on, 0=pixel off) for the eight user-define 5×8 characters. Valid CGRAM addresses are 00H to 3FH. CGRAM not used to defined characters can be used as general purpose RAM. Character codes 00H~07H (or 08H~0FH) are assigned to the user-defined characters (see section 5.0 character font tables). The table below shows the relationship between the character codes, CGRAM addresses, and CGRAM data for each user-defined character.

Relationship between CGRAM address and character code (DDRAM) and 5×7 (with cursor) dot character patterns (CGRAM)

Character Code (RAM Data)								CGRAM Address						CGRAM Data								
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
High Order Bit							Low Order Bit	High Order Bit			Low Order Bit			High Order Bit							Low Order Bit	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	X	X	X	**1**	0	0	0	**1**	Character Pattern (1)
0	0	0	0	X	0	0	0	0	0	0	0	0	1	X	X	X	**1**	0	0	0	**1**	
0	0	0	0	X	0	0	0	0	0	0	0	1	0	X	X	X	**1**	0	0	0	**1**	
0	0	0	0	X	0	0	0	0	0	0	0	1	1	X	X	X	**1**	**1**	**1**	**1**	**1**	
0	0	0	0	X	0	0	0	0	0	0	1	0	0	X	X	X	**1**	0	0	0	**1**	
0	0	0	0	X	0	0	0	0	0	0	1	0	1	X	X	X	**1**	0	0	0	**1**	
0	0	0	0	X	0	0	0	0	0	0	1	1	0	X	X	X	**1**	0	0	0	**1**	
0	0	0	0	X	0	0	0	0	0	0	1	1	1	X	X	X	0	0	0	0	0	Cursor Position
0	0	0	0	X	0	0	1	0	0	1	0	0	0	X	X	X	**1**	**1**	**1**	**1**	**1**	Character Pattern (2)
0	0	0	0	X	0	0	1	0	0	1	0	0	1	X	X	X	0	0	**1**	0	0	
0	0	0	0	X	0	0	1	0	0	1	0	1	0	X	X	X	0	0	**1**	0	0	
0	0	0	0	X	0	0	1	0	0	1	0	1	1	X	X	X	0	0	**1**	0	0	
0	0	0	0	X	0	0	1	0	0	1	1	0	0	X	X	X	0	0	**1**	0	0	
0	0	0	0	X	0	0	1	0	0	1	1	0	1	X	X	X	0	0	**1**	0	0	
0	0	0	0	X	0	0	1	0	0	1	1	1	0	X	X	X	0	0	**1**	0	0	
0	0	0	0	X	0	0	1	0	0	1	1	1	1	X	X	X	0	0	0	0	0	Cursor Position
↓								↓			↓			↓								
0	0	0	0	X	1	1	1	1	1	1	0	0	0	X	X	X	**1**	0	0	0	**1**	Character Pattern (8)
0	0	0	0	X	1	1	1	1	1	1	0	0	1	X	X	X	**1**	0	0	**1**	0	
0	0	0	0	X	1	1	1	1	1	1	0	1	0	X	X	X	**1**	0	**1**	0	0	
0	0	0	0	X	1	1	1	1	1	1	0	1	1	X	X	X	**1**	**1**	0	0	0	
0	0	0	0	X	1	1	1	1	1	1	1	0	0	X	X	X	**1**	0	**1**	0	0	
0	0	0	0	X	1	1	1	1	1	1	1	0	1	X	X	X	**1**	0	0	**1**	0	
0	0	0	0	X	1	1	1	1	1	1	1	1	0	X	X	X	**1**	0	0	0	**1**	
0	0	0	0	X	1	1	1	1	1	1	1	1	1	X	X	X	**1**	**1**	**1**	**1**	**1**	Cursor Position

Note: ″X″ means don′t care

Character code bits 0~2 correspond to CGRAM address bits 3~5 (3 bits: 8 types)

CGRAM address bits 0~2 designate character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.

Character pattern row position corresponds to CGRAM data bits 0~4 (bit 4 being at the left).

CGRAM character patterns are selected when character code bits 4~7 are all 0. However, since character code bit 3 has no effect, the ″H″ display example above can be selected by either character code 00H or 08H.

1 for CGRAM data corresponds to display selection and 0 to non selection.

Timing Generation Circuit

Timing generation circuit generates timing signals for the operation of internal circuit such as DDRAM, CGRAM and CGROM. The RAM reads the timing for display and the internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

VFD Driver Circuit

VFD driver circuit consists of 24 grid signal drivers and 80 segment signal drivers. When the character font and number of digits are selected by hardware (DS0, DS1) at power on, the required grid signal drivers automatically output drive waveforms, while the other grid signal driver continue to output non-selection waveforms.

Sending serial data is latched when the display data character pattern corresponds to the last address of the display data RAM (DDRAM).

Since serial data is latched when the display data character pattern corresponds to the starting address enters the internal shift register, the HT16528 drives from the head display.

Cursor/Blink Control Circuit

Cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DDRAM) address set in the address counter (AC).

For example, when the address counter is 08H, the cursor position is displayed at DDRAM address 08H.

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

Cursor/Blink Control Table

Display position (Digit)	1	2	3	4	5	6	7	8	9	10	11	12
DDRAM address (Hexadecimal)	00	01	02	03	04	05	06	07	**08**	09	0A	0B

Cursor Position

1-line Display

Display position (Digit)	1	2	3	4	5	6	7	8	9	10	11	12
DDRAM address	00	01	02	03	04	05	06	07	**08**	09	0A	0B
(Hexadecimal)	40	41	42	43	44	45	46	47	48	49	4A	4B

Cursor Position

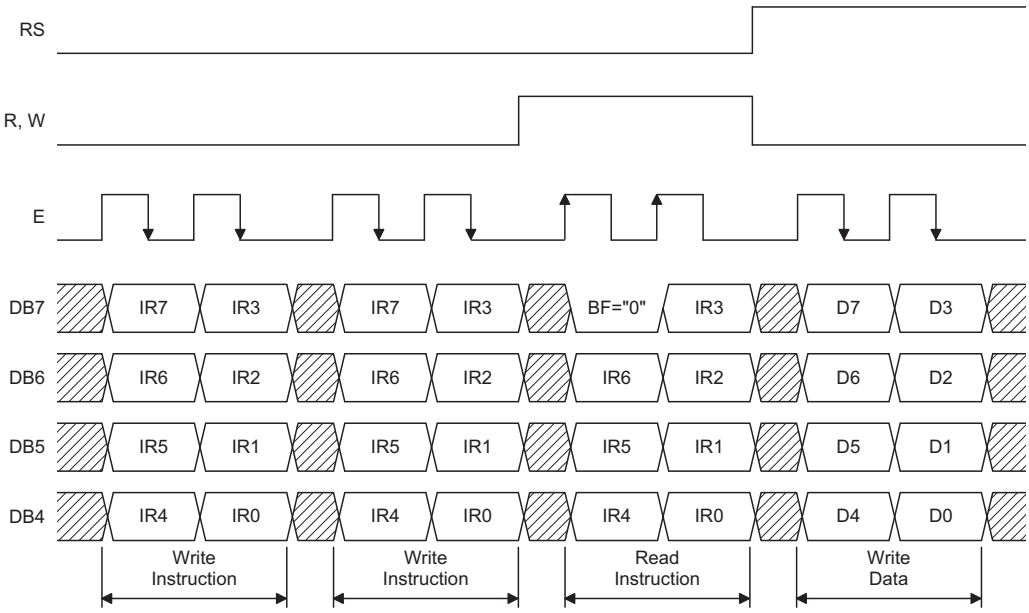
2-line Display

Note: The cursor or blinking appears when the address counter (AC) selects the character generator RAM (CGRAM). However, the cursor and blinking become meaningless when the cursor or blinking is displayed in the meaningless position when AC is a CGRAM address.

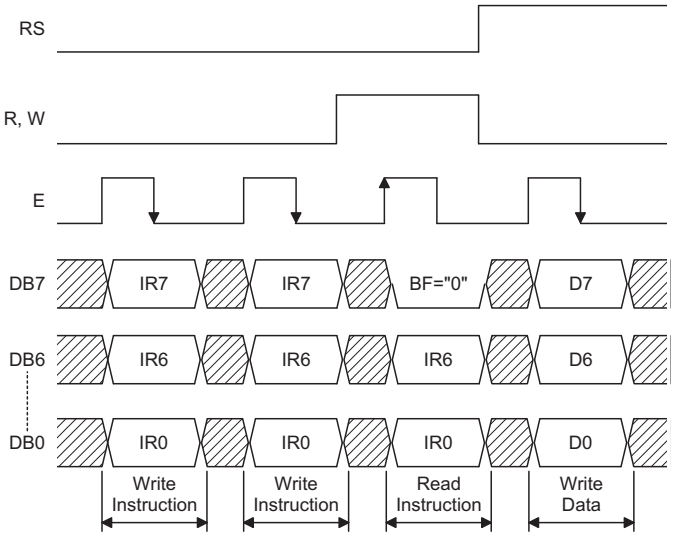
Interface With CPU Mode

- Parallel Data Transfer M68 (IM=1, MPU=1)
  This IC can interface (data transfer) with the CPU in 4 or 8 bits in M68 interface.
  However, the internal registers consist of 8 bits. Using the DB4 to DB7 twice must perform data transfer in 4 bits. When using 4-bit parallel data transfer, DB0 to DB3 pins remain Hi or Low. The transfer order is initially from the higher 4 bits (D4 to D7) then followed by the lower 4 bits (D0 to D3).
  BF checks are performed before transferring the higher 4 bits. BF checks are not required before transferring the lower 4 bits.

- 4-bit data transfer (M68)



- 8-bit data transfer (M68)



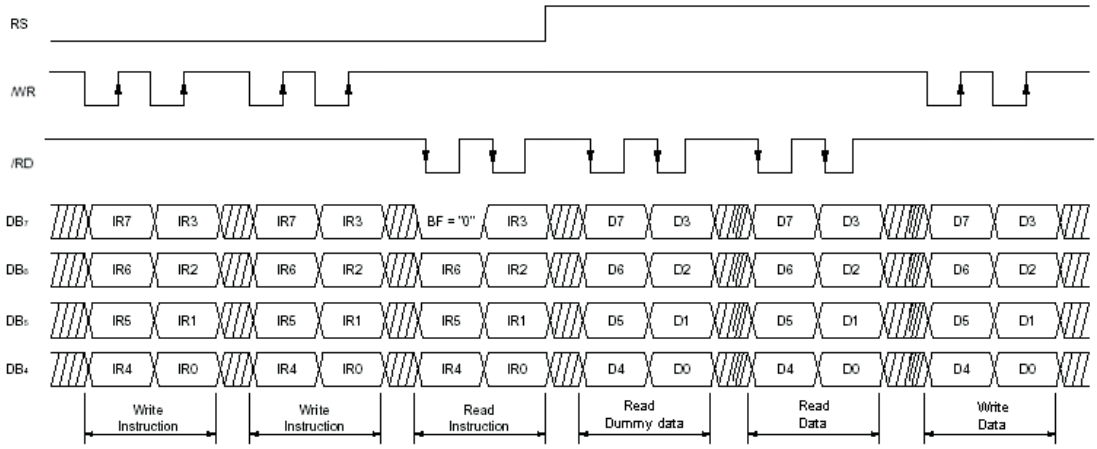
Parallel mode for i80 (IM=1, MPU=0)

When setting ″IM=1, MPU=0″, i80 is selected. In the HT16528, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to internal data bus.

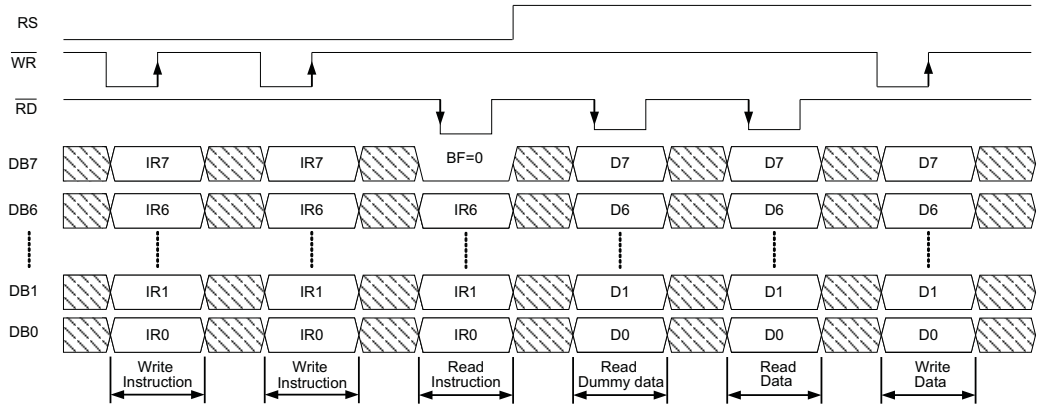
8-bit or 4-bit mode can be selected for i80 interface. However, the internal registers consist of 8 bits. DB4 to DB7 must be used twice for performing data transfer in 4-bit mode. When using 4-bit parallel data transfer, DB0 to DB3 pins remain Hi or Low. The transfer order is started from the higher 4 bits (D4 to D7) then followed by the lower 4 bits (D0 to D3).

There is a certain restriction in the read sequence of this display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read for the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is selected. This relationship is shown in the following figure.

- 4-bit data transfer (i80)



- 8-bit data transfer (i80)

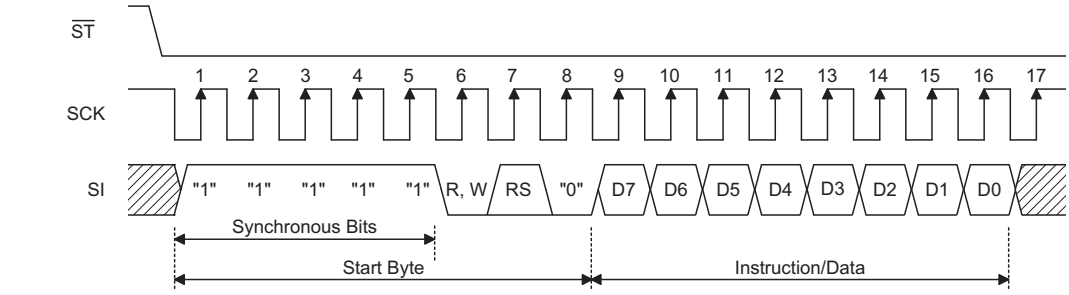


Serial Mode

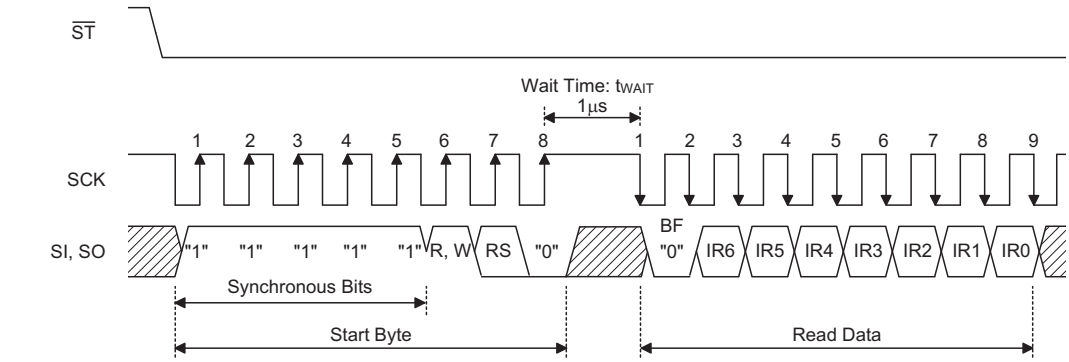
In the synchronous serial interface mode, instructions and data are sent between the host and the module using 8-bit bytes. Two bytes are required per read/write cycle and are transmitted MSB first. The start byte contains 5 high bits, the Read/Write (R/W) control bit, the Register Select (RS) control bit, and a low bit. The subsequent byte contains the instruction/data bits. The R/W bit determines whether the cycle is a read (high) or a write (low) cycle. The RS bit is used to identify the second byte as an instruction (low) or data (high).

This mode uses the strobe ($\overline{ST}$) control signal, Serial Clock (SCK) input, and Serial I/O (SI/SO) line to transfer information. In a write cycle, bits are clocked into the module on the rising edge of SCK. In a read cycle, bits in the start byte are clocked into the module on the rising edge of SCK. After a minimum wait time, each bit in the instruction/data byte can be read from the module after each falling edge of SCK. Each read/write cycle begins on the falling edge of $\overline{ST}$ and ends on the rising edge. To be a valid read/write cycle, the $\overline{ST}$ must go high at the end of the cycle.

Data Write



Data Read



Commands

Instruction	RS	R, W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Clear display	0	0	0	0	0	0	0	0	0	1	Clear all display, and sets the DDRAM address at 00H.
Cursor home	0	0	0	0	0	0	0	0	1	x	Sets the DDRAM address at 00H. Also returns the display shifted to the original position. The DDRAM contents remain unchanged.
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor direction and specifies the display shift. These operations are performed during writing/reading data.
Display On/Off	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF(D), cursor ON/OFF(C), cursor blink of character position (B).
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	x	x	Shifts display or cursor, while keeping the DDRAM contents.
Function	0	0	0	0	1	DL	N	x	BR1	BR0	Sets data length (in parallel data transfer) and Number of line
CGRAM address set	0	0	0	1	ACG						Sets the address of the CGRAM. After that, data of the DDRAM is transferred.
DDRAM address set	0	0	1	ADD							Sets the address of the DDRAM. After that, data of the DDRAM is transferred.
Read busy flag & address	0	1	BF=0	ACC							Reads the busy flag (BF) and the address counter. BF is output as ″0″ always.
Write data to CGRAM or DDRAM	1	0	Write data								Writes data into the CGRAM of the DDRAM.
Read data from CGRAM or DDRAM	1	1	Read DR data								Reads data from the CGRAM or DDRAM.

Note: I/D=1: Increment, I/D=0: Decrement
S=1: Display shift enable, S=0: Cursor shift enable
S/C=1: Display shift, S/C=0: Cursor shift
R/L=1: Right shift, R/L=0: Left shift
DL=1: 8bit, DL=0: 4bit
BR1, BR0= (00: 100%) , (01: 75%) , (10: 50%) , (11: 25%)
″X″: Don′t care
ACG: CGRAM address
ADD: DDRAM address
ACC: Address counter
DDRAM: Display Data RAM
CGRAM: Character Generator RAM

Clear Display

	RS	R, W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

The instruction:

- Fills all locations in the display data RAM (DDRAM) with 20H (Blank character).
- Clears the contents of the address counter (ACC) to 00H.
- Sets display for zero character shifts (returns to original position).
- Sets the address counter to point to the display data RAM (DDRAM).
- If cursor is displayed, move cursor to the left most character in the top line (upper line).
- Sets address counter (ACC) to increment on each access to DDRAM or CGRAM.

When resetting

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1

Cursor Home

	RS	R, W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

Note: "x" don't care

The instruction:

- Clears the contents of the address counter (ACC) to 00H.
- Sets the address counter to point to the display data RAM (DDRAM).
- Sets display for zero character shifts (returns to original position).
- If cursor is displayed, move cursor to the left most character in the top line (upper line).

Entry Mode

	RS	R, W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

This instruction selects whether the cursor position increments or decrements after each DDRAM or CGRAM access and determines the direction the information on the display shifts after each DDRAM write. The instruction also enables or disables display shifts after each DDRAM write (information on the display does not shift after a DDRAM read or CGRAM access). The DDRAM, CGRAM, and cursor position are not affected by this instruction.

I/D=0: The AC decrements after each DDRAM or CGRAM access.
If S=1, the information on the display shifts to the right by one character position after each DDRAM write.

I/D=1: The AC increments after each DDRAM or CGRAM access.
If S=1, the information on the display shifts to the left by one character position after each DDRAM write.

S=0: The display shift function is disabled.

S=1: The display shift function is enabled.

Cursor Move and Display Shift by the Entry Mode Set			
I/D	**S**	**After Writing DDRAM Data**	**After Reading DDRAM Data**
0	0	Cursor moves one character to the left.	Cursor moves one character to the right.
1	0	Cursor moves one character to the right.	Cursor moves one character to the right.
0	1	Display shifts one character to the right without cursor movements.	Cursor moves one character to the left.
1	1	Display shifts one character to the left without cursor movements.	Cursor moves one character to the right.

When resetting

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0

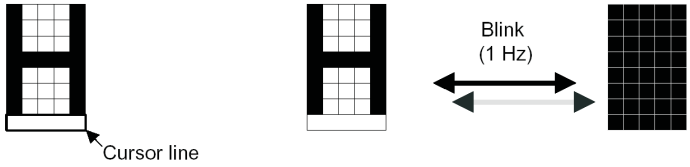
Display ON/OFF

	RS	R, W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

This instruction selects whether the display and cursor are on or off and selects whether or not the character at the current cursor position blinks. The DDRAM, CGRAM, and cursor position are not affected by this instruction.

- D=0: The display is off (display blank).
- D=1: The display is on (contents of the DDRAM is displayed).
- C=0: The cursor is off.
- C=1: The cursor is on (8th rows of pixels).
- B=0: The blinking character function is disabled.
- B=1: The blinking character function is enabled

Note: A character with all pixels on will alternate with the character displayed at the current cursor position at a 1Hz rate with a 50% duty cycle.



When resetting

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	0

Cursor or Display Shift

	RS	R, W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X

Note: ″x″ don't care

This instruction shifts the display and/or moves the cursor to the left or right, without reading or writing to the DDRAM.

″S/C″ bit selects movement of the cursor or movement of both cursor and display.

- S/C=1: Shift both cursor and display.
- S/C=0: Shift only the cursor.

  ″R/L″ bit selects whether moving the direction to the left or right of the display and/or cursor.
- R/L=1: Shift one character right.
- R/L=0: Shift one character left.

Cursor or Display Shift			
S/C	**R/L**	**Cursor Position**	**Information on the Display**
0	0	Decrements by one (left)	No change
0	1	Increments by one (right)	No change
1	0	Decrements by one (left)	Shifts on character position to the left
1	1	Increments by one (right)	Shifts on character position to the right

Function Set

	RS	R, W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	X	BR1	BR0

Note: ″x″ don't care

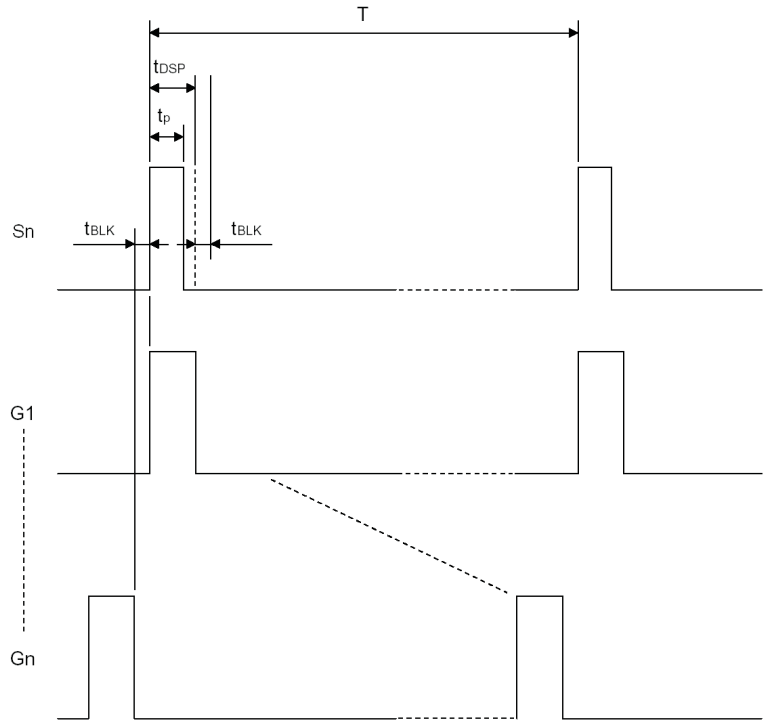
This instruction sets the width of the data bus for the parallel interface modes, the number of display lines, and the luminance level (brightness) of the VFD. DDRAM, CGRAM, and cursor position are not affected by this instruction.

- DL=0: Sets the data bus width for the parallel interface modes to 4-bit (DB7~DB4).
- DL=1: Sets the data bus width for the parallel interface modes to 8-bit (DB7~DB0).
- N=0: Sets the number of display lines to 1 (this setting is not recommended, using segment output S1~S40, S41~S80 fixed to Low level).
- N=1: Sets the number of display lines to 2 (using segment output S1~S80).

BR1, BR0 flag is brightness control for the VFD to modulate the pulse width of the segment output as follows.

t_{DSP}≅200μs, t_{BLK}≅10μs

BR1	BR0	Brightness	t_P
0	0	100%	t_{DSP}×1.00
0	1	75%	t_{DSP}×0.75
1	0	50%	t_{DSP}×0.50
1	1	25%	t_{DSP}×0.25



Note: "n" means number of grid, T=nx (t_{DSP}+t_{BLK})

When resetting

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0

CGRAM Address Set

	RS	R,W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	A	A	A	A	A	A

This instruction places the 6-bit CGRAM address specified by DB5~DB0 into the cursor position. Subsequent data writes (reads) will be to (from) the CGRAM. The DDRAM and CGRAM contents are not affected by this instruction.

When resetting: Don't care.

DDRAM Address Set

	RS	R,W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	A	A	A	A	A	A	A

This instruction places the 7-bit DDRAM address specified by DB6~DB0 into the cursor position. Subsequent data writes (reads) will be to (from) the DDRAM. The DDRAM and CGRAM contents are not affected by this instruction.

Valid DDRAM Address Ranges		
	Number of Character	**Address Range**
1st line	40	00H~27H
2nd line	40	40H~67H

When resetting: Don′t care.

Read Busy Flag and Address

	RS	R,W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	A	A	A	A	A	A	A

This instruction reads the Busy Flag (BF)* and the value of address counter in binary ″AAAAAAA″. This address counter is used by the CGRAM and DDRAM addresses, its value is determined by the previous instruction. The address counter contents are the same as for instructions ″CGRAM address set″ and ″DDRAM address set″.

Note: ″*″ means the Busy Flag (BF) always outputs a ″0″.

Write Data to the CGRAM or DDRAM

	RS	R,W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D	D	D	D	D	D	D	D
			←High order bit							Low order bit→

This instruction writes the 8-bit data byte on DB7~DB0 into the DDRAM or CGRAM location addressed by the cursor position. The most recent DDRAM or CGRAM Address Set instruction determines whether the write is to the DDRAM or CGRAM. This instruction also increments or decrements the cursor position and shifts the display according to the I/D and S bits set by the Entry Mode Set instruction.

Read Data from CGRAM or DDRAM

	RS	R,W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D	D	D	D	D	D	D	D
			←High order bit							Low order bit→

This instruction reads the 8-bit data byte from the DDRAM or CGRAM location addressed by the cursor position on DB7~DB0. The most recent DDRAM or CGRAM Address Set instruction determines whether the read is from the DDRAM or CGRAM. This instruction also increments or decrements the cursor position and shifts the display according to the I/D and S bits set by the Entry Mode Set instruction. Before sending this instruction, a DDRAM or CGRAM Address Set instruction should be executed to set the cursor position to the desired DDRAM or CGRAM address to be read.

After reading one data, the value of the address is automatically increased or decreased by 1 according to the selection by ″Entry mode″.

Note: The Address counter is automatically increased or decreased by 1 after a data write instruction to the CGRAM or DDRAM are executed. But at this moment the data to be pointed to by the address counter cannot be read if a data read instruction is executed. Therefore, to read data correctly, executing an address set instruction or cursor shift instruction (the only case of a DDRAM data read) just before reading, or reading the second data in case of reading data continuously by executing a read data instruction.

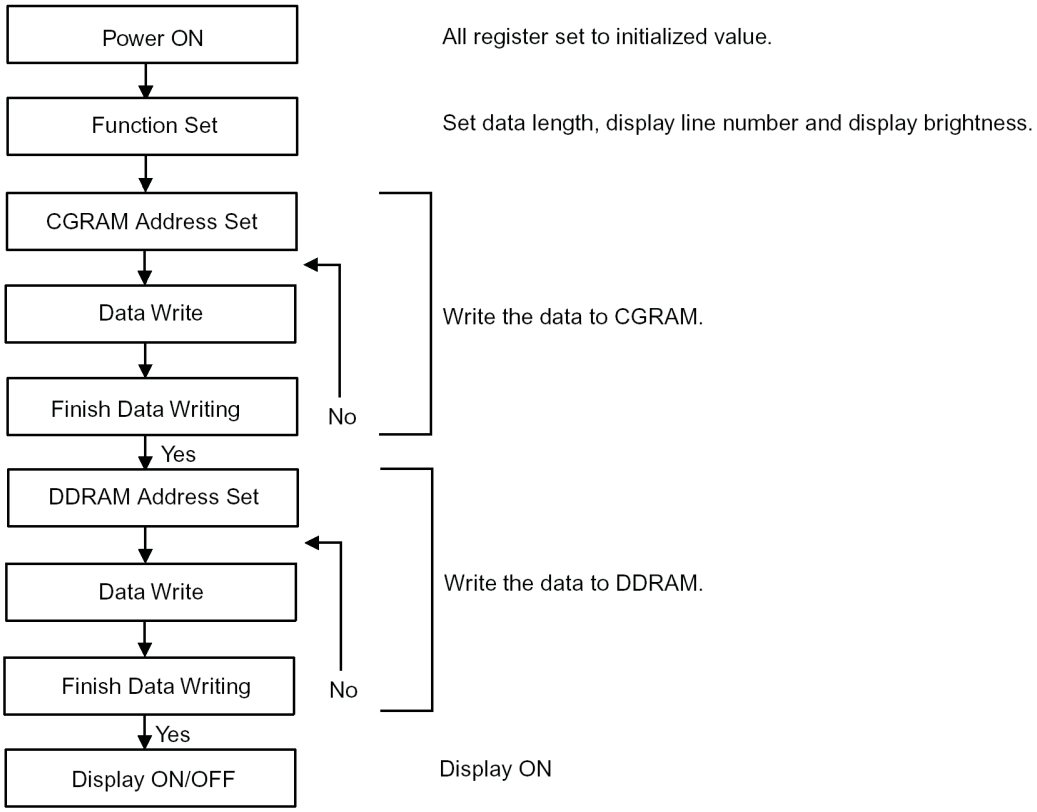
Power ON Reset

After a power-on reset, the module is initialize to the following conditions:

- All DDRAM locations are set to 20H (character code for a space).
- The cursor position is set to DDRAM address 00H
- The relationship between DDRAM addresses and character positions on the VFD is set to the non-shifted position.
- Entry Mode Set instruction bits:
  I/D=1: The cursor position increments after each DDRAM or CGRAM access.
  If S=1, the information on the display shifts to the left by one character position after each DDRAM write.
  S=0: The display shift function is disabled.
- Display On/Off Control instruction bits:
  D=0: The display is off (display blank).
  C=0: The cursor is off.
  B=0: The blinking character function is disabled.
- Function Set instruction bits:
  DL=1: Sets the data bus width for the parallel interface modes to 8 bits (DB7~DB0).
  N=1: Number of display lines is set to 2.
  BR1, BR0=0,0: Sets the luminance level to 100%.
- MPU interface, duty ratio selection are based on the following table.

Relationship between Status of HT16528 and Pin Selection at Power on Reset					
Pin Name				Function	Remark
TEST	IM	DS1	DS0		
1	x	x	x	Self test mode	This is effective on aging.
0 or open	0	x	x	Serial interface	SI, SO, SCK, $\overline{ST}$
0 or open	1	x	x	Parallel interface	RS, E, R, W, DB7~DB4 or DB7~DB0
0 or open	x	0	0	Duty= 1/16 (16C×1 or 2L display)	It's not necessary to use the extension driver. The number of line is selected by instruction.
0 or open	x	0	1	Duty= 1/20 (20C×1 or 2L display)	
0 or open	x	1	0	Duty= 1/24 (24C×1 or 2L display)	
0 or open	x	1	1	Duty= 1/40 (40C×1 or 2L display)	Extension driver should be used. The number of line is selected by instruction.

Example (8-bit Data Parallel, Data Increment Mode)

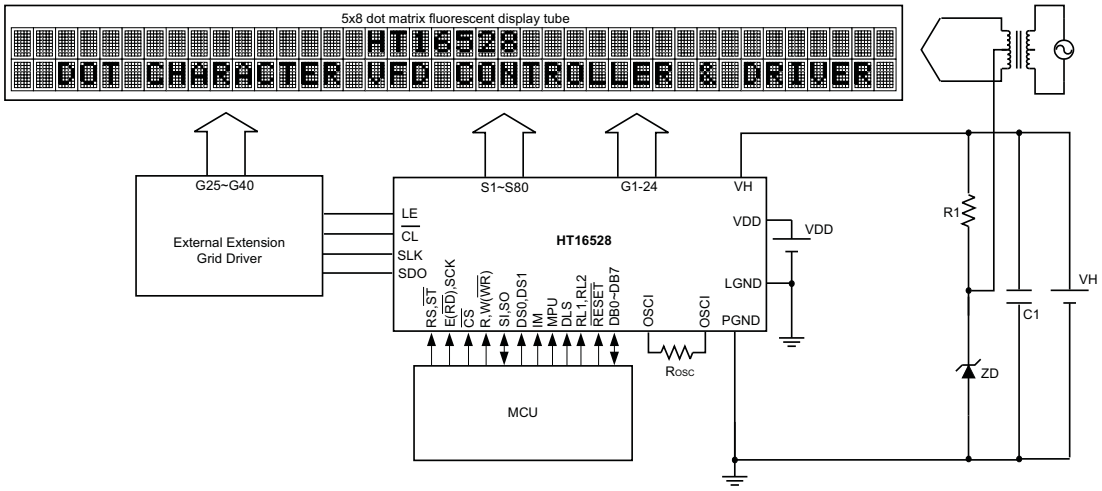


Initialization Sequence & Data Set

Initialization Programming Example & Data Set (M68 series MPU)

RS	R, W	D7	D6	D5	D4	D3	D2	D1	D0	Description
Power On										
0	0	0	0	1	1	1	x	0	1	Function Set Data length: 8 bits Display line number: 2 lines VFD Brightness: 75%
0	0	0	1	0	0	0	0	0	0	CGRAM address set to 00H
1	0	x	x	x	D	D	D	D	D	Write data to CGRAM 64 bytes (8 characters)
		x	x	x	D	D	D	D	D	
		|	|	|	|	|	|	|	|	
		x	x	x	D	D	D	D	D	
0	0	1	0	0	0	0	0	0	0	DDRAM address set to 00H
1	0	D	D	D	D	D	D	D	D	Write data to DDRAM 80 bytes (80 characters)
		D	D	D	D	D	D	D	D	
		|	|	|	|	|	|	|	|	
		D	D	D	D	D	D	D	D	
0	0	0	0	0	0	1	1	0	0	Display ON/OFF Display ON, cursor OFF, cursor blink OFF

Application Circuits

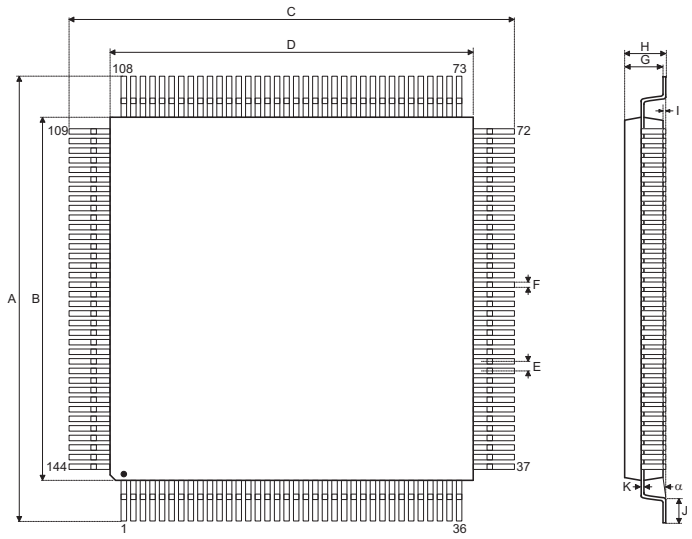


Note: The VH value depends on the fluorescent display tube used. Adjust the value of the constants R1 and ZD to the power supply voltage used.

R_{OSC}=56kΩ for oscillator resistor.

Package Information

144-pin LQFP (20mm×20mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.862	—	0.870
B	0.783	—	0.791
C	0.862	—	0.870
D	0.783	—	0.791
E	—	0.020	—
F	—	0.008	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	21.90	—	22.10
B	19.90	—	20.10
C	21.90	—	22.10
D	19.90	—	20.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°