Features

- Logic supply voltage: 5V/3.3V
- Maximum output terminal voltage: 17V
- 16-channel constant current output
- Channel output current range
  – 3~45mA @V_{DD}=5V
  – 3~30mA @V_{DD}=3.3V
- Excellent output current accuracy
  – Between channels: < ± 2.5%
  – Between devices: < ± 3%
- Adjustable $\overline{OE}$ line output pulse width
- Staggered output delay
- Up to 25MHz serial interface clock frequency
- Schmitt trigger input structure
- Package types: 24-pin SSOP

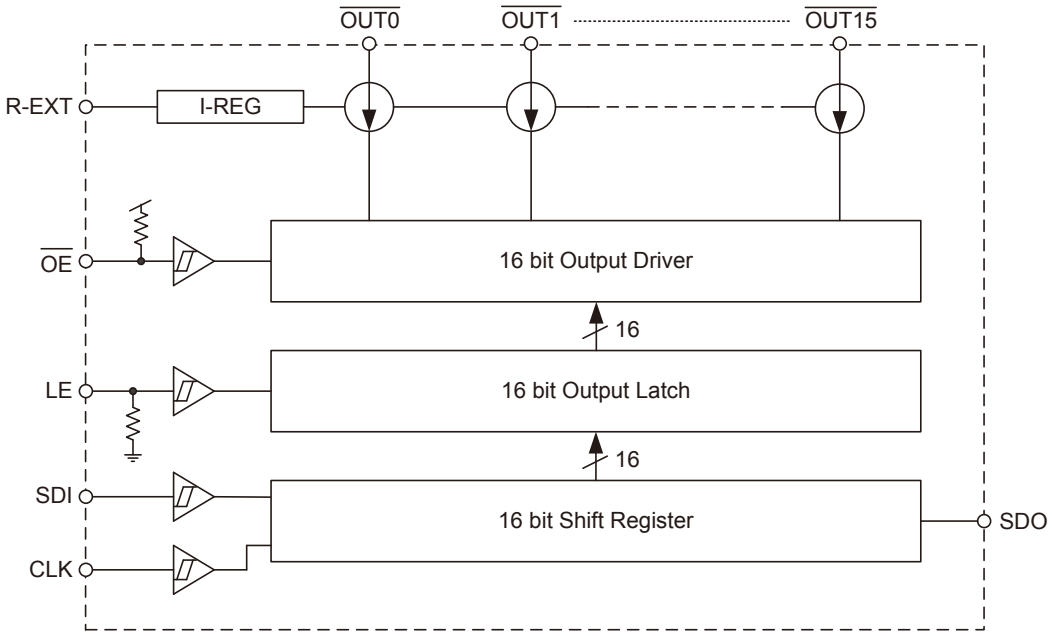
Applications

- LED displays
- Message boards
- Other consumer applications

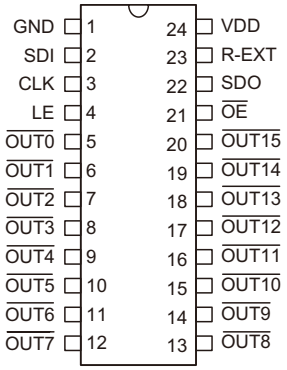
General Description

The HT16D724 is a high accuracy constant current driver which is specifically designed for LED display applications. The device provides 16-channel stable and constant current outputs for driving LEDs. Communication with the outside world is managed using a fully integrated serial interface function, which provides designers with a means of easy communication with external peripheral hardware. In this way, many devices can be cascaded together to drive larger LED displays.

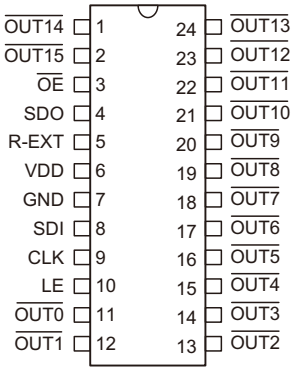
Block Diagram



Pin Assignment



HT16D724
24 SSOP-A

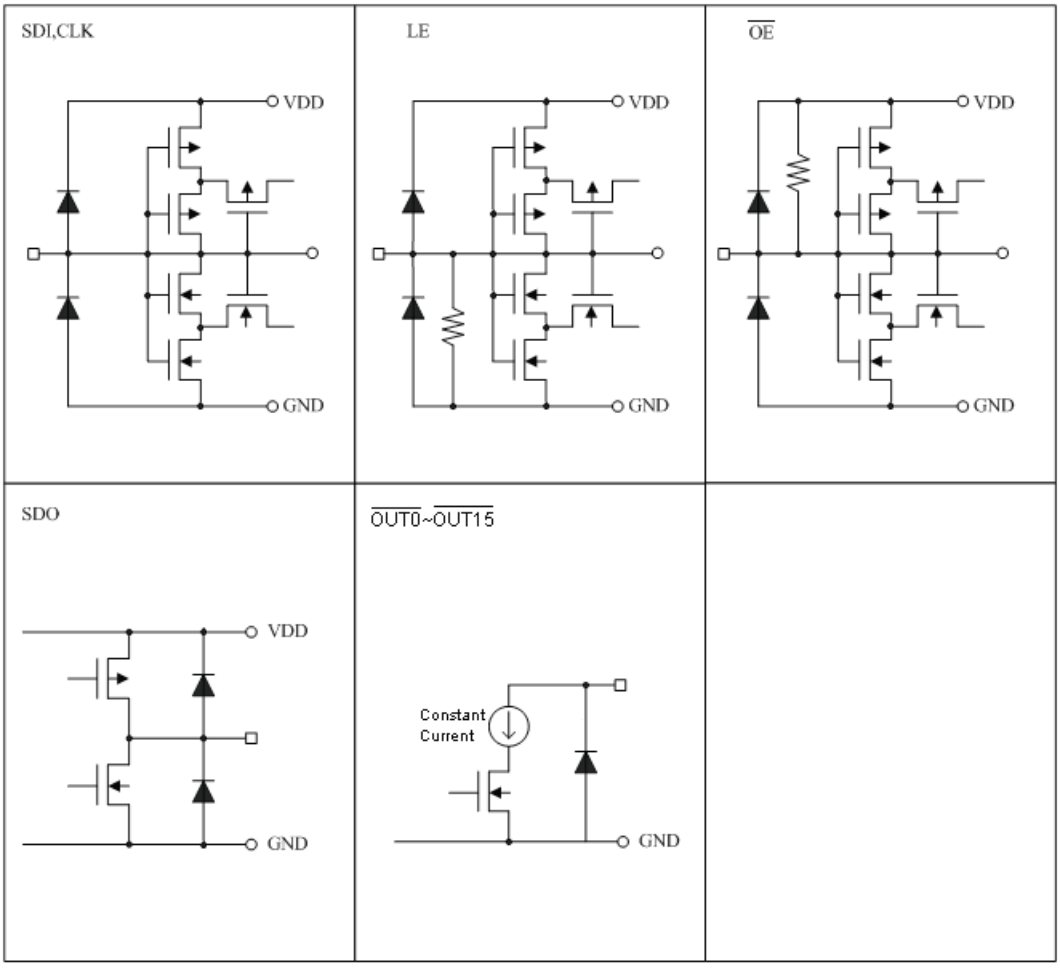


HT16D724-1
24 SSOP-B

Pin Description

Pin Name	I/O	Description
VDD	—	Positive power supply
GND	—	Negative power supply, ground.
SDI	I	Serial data input
CLK	I	Clock input Transfers data on its rising edge and carry command information when the LE line is asserted.
LE	I	Data latch control Data is latched into the internal latch register during an LE pin high level.
$\overline{OE}$	I	Output enable control 1: all outputs disabled 0: all outputs enabled
R-EXT	I	External resistor connection input Connected to an external resistor to setup the output ports current level.
$\overline{OUT0}$~$\overline{OUT15}$	O	Parallel data outputs
SDO	O	Serial data output Used for cascading of other LED driver devices.

Approximate Internal Connections



Absolute Maximum Ratings

Logic Supply Voltage (V_{DD})....V_{GND}-0.3V to V_{GND}+7.0V
Logic Input Voltage .....V_{GND}-0.3V to V_{DD}+0.3V
Output Voltage ..... V_{GND}-0.3V to 20V

Output Current 50mA
GND Terminal Current 800mA
Storage Temperature .....-55°C to 150°C
Operating Temperature .....-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

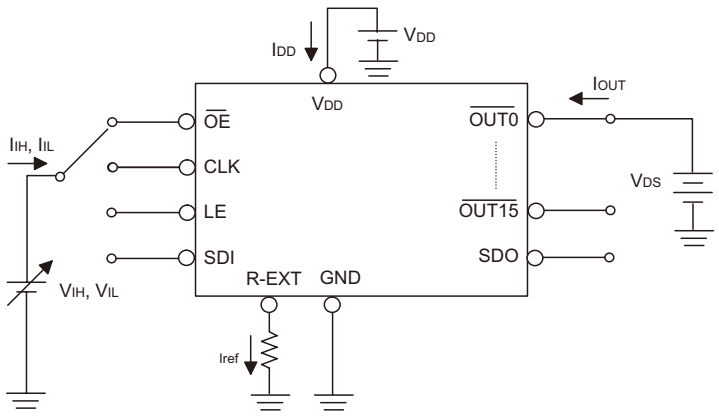
V_{DD}= 5.0V, Ta= 25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Logic Supply Voltage	—	4.5	5.0	5.5	V
I_{OUT}	Output Current	Current range	3	—	45	mA
V_{IH}	High Input Voltage (SDI, CLK, LE, $\overline{OE}$ pins)	Ta=-40°C~85°C	$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	Low Input Voltage (SDI, CLK, LE, $\overline{OE}$ pins)	Ta=-40°C~85°C	0	—	$0.3V_{DD}$	V
V_{OH}	SDO pin High-Level Output Voltage	I_{OH}=-1mA	4.6	—	—	V
V_{OL}	SDO pin Low-Level Output Voltage	I_{OL}=+1mA	—	—	0.4	V
I_{OZ}	Output Leakage Current	V_{DS}=17V and channel off	—	—	0.5	uA
I_{OUT1}	Output Current 1	V_{DS}=1V, R_{ext}=6000Ω,	—	3.1	—	mA
I_{OUT2}	Output Current 2	V_{DS}=1V, R_{ext}=720Ω,	—	25.8	—	mA
dI_{OUT1}	Current Skew	I_{OUT}=3.1mA, V_{DS}=1V, R_{ext}=6000Ω	—	±1.5	±2	%
dI_{OUT2}	Current Skew	I_{OUT}=25.8mA, V_{DS}=1V, R_{ext} =720Ω	—	±1.5	±2.5	%
$\%/dV_{DS}$	Output Current vs. Output Voltage Regulation	V_{DS} =1.0V~3.0V	—	±0.1	—	%/V
$\%/dV_{DD}$	Output Current vs. Supply Voltage Regulation	V_{DD} = 4.5V~5.5V	—	—	±1.0	%/V
R_{PU}	$\overline{OE}$ Pin Pull High Resistor	—	250	450	800	KΩ
R_{PD}	LE Pin Pull Low Resistor	—	250	450	800	KΩ
I_{DD}	Supply Current	R_{ext}=open, $\overline{OUT0}$~$\overline{OUT15}$=off	—	2	2.8	mA
		R_{ext}=1240Ω, $\overline{OUT0}$~$\overline{OUT15}$=off	—	4	4.8	mA
		R_{ext}=620Ω, $\overline{OUT0}$~$\overline{OUT15}$=off	—	6	6.8	mA
		R_{ext}=1240Ω, $\overline{OUT0}$~$\overline{OUT15}$=on	—	5.2	8.2	mA
		R_{ext}=620Ω, $\overline{OUT0}$~$\overline{OUT15}$=on	—	6.5	9.5	mA

V_{DD}= 3.3V, Ta= 25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Logic Supply Voltage	—	3	3.3	3.6	V
I_{OUT}	Output Current	Current range	3	—	30	mA
V_{IH}	High Input Voltage (SDI, CLK, LE, $\overline{OE}$ pins)	Ta=-40°C~85°C	$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	Low Input Voltage (SDI, CLK, LE, $\overline{OE}$ pins)	Ta=-40°C~85°C	0	—	$0.3V_{DD}$	V
V_{OH}	SDO pin High-Level Output Voltage	I_{OH}=-1mA	2.9	—	—	V
V_{OL}	SDO pin Low-Level Output Voltage	I_{OL}=+1mA	—	—	0.4	V
I_{OZ}	Output Leakage Current	V_{DS}=17V and channel off	—	—	0.5	uA
I_{OUT1}	Output Current 1	V_{DS}=1V, R_{ext}=6000Ω,	—	3.1	—	mA
I_{OUT2}	Output Current 2	V_{DS}=1V, R_{ext}=720Ω,	—	25.8	—	mA
dI_{OUT1}	Current Skew	I_{OUT}=3.1mA, V_{DS}=1V, R_{ext}=6000Ω	—	±1.5	±2	%
dI_{OUT2}	Current Skew	I_{OUT}=25.8mA, V_{DS}=1V, R_{ext} =720Ω	—	±1.5	±2.5	%
$\%/dV_{DS}$	Output Current vs. Output Voltage Regulation	V_{DS} =1.0V~3.0V	—	±0.1	—	%/V
$\%/dV_{DD}$	Output Current vs. Supply Voltage Regulation	V_{DD} = 3V~3.6V	—	—	±1.0	%/V
R_{PU}	$\overline{OE}$ Pin Pull High Resistor	—	250	450	800	KΩ
R_{PD}	LE Pin Pull Low Resistor	—	250	450	800	KΩ
I_{DD}	Supply Current	R_{ext}=open, $\overline{OUT0}$~$\overline{OUT15}$=off	—	1.7	2.3	mA
		R_{ext}=1851Ω, $\overline{OUT0}$~$\overline{OUT15}$=off	—	3.9	4.5	mA
		R_{ext}=748Ω, $\overline{OUT0}$~$\overline{OUT15}$=off	—	5.2	5.8	mA
		R_{ext}=1851Ω, $\overline{OUT0}$~$\overline{OUT15}$=on	—	3.9	4.5	mA
		R_{ext}=748Ω, $\overline{OUT0}$~$\overline{OUT15}$=on	—	5.2	5.8	mA

D.C. Characteristics Test Circuit



A.C. Characteristics

V_{DD}= 5.0V, Ta= 25°C

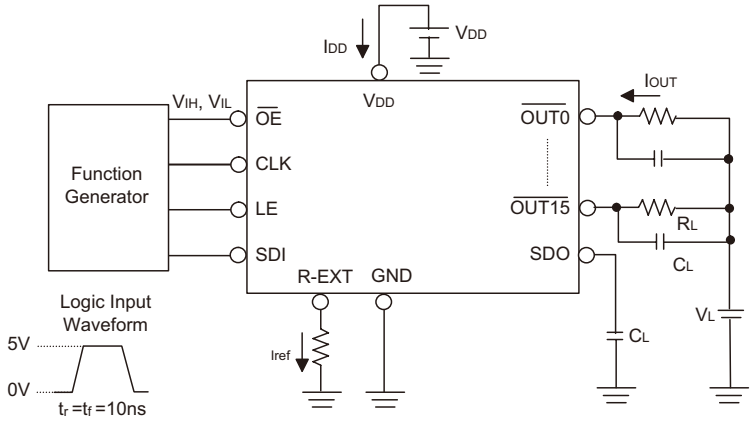
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay Time (“L” to “H”, CLK→SDO)	V_{DS}= 1.0V V_{IH}= V_{DD} V_{IL}= GND R_{ext}= 930Ω V_L= 4.5V R_L= 162Ω C_L= 10pF	—	20	40	ns
t_{PLH1}	Propagation Delay Time (“L” to “H”, CLK→OUT2n		—	45	65	ns
	Propagation Delay Time (“L” to “H”, CLK→OUT2n+1)		—	30	50	ns
t_{PLH2}	Propagation Delay Time (“L” to “H”, LE→OUT2n)		—	45	65	ns
	Propagation Delay Time (“L” to “H”, LE→OUT2n+1)		—	30	50	ns
t_{PLH3}	Propagation Delay Time (“L” to “H”, $\overline{OE}$→OUT2n)		—	45	65	ns
	Propagation Delay Time (“L” to “H”, $\overline{OE}$→OUT2n+1)		—	30	50	ns
t_{PHL}	Propagation Delay Time (“H” to “L”, CLK→SDO)		—	20	40	ns
t_{PHL1}	Propagation Delay Time (“H” to “L”, CLK→OUT2n)		—	60	85	ns
	Propagation Delay Time (“H” to “L”, CLK→OUT2n+1)		—	50	65	ns
t_{PHL2}	Propagation Delay Time (“H” to “L”, LE→OUT2n)		—	60	85	ns
	Propagation Delay Time (“H” to “L”, LE→OUT2n+1)		—	50	65	ns
t_{PHL3}	Propagation Delay Time (“H” to “L”, $\overline{OE}$→OUT2n)		—	70	95	ns
	Propagation Delay Time (“H” to “L”, $\overline{OE}$→OUT2n+1)		—	60	75	ns
$t_{W(CLK)}$	Pulse Width		20	—	—	ns
$t_{W(LE)}$	Pulse Width		20	—	—	ns
$t_{W(OE)}$	$\overline{OE}$ Pulse Width		70	100	—	ns
F_{CLK}	Data Clock Frequency		—	—	25	MHz
$t_{h(LE)}$	LE Hold Time		30	—	—	ns
$t_{su(LE)}$	LE Setup Time		5	—	—	ns
$t_{h(SDI)}$	SDI Hold Time		5	—	—	ns
$t_{su(SDI)}$	SDI Setup Time		3	—	—	ns
t_r	Maximum CLK Rise Time (See Note)		—	—	500	ns
t_f	Maximum CLK Fall Time (See Note)		—	—	500	ns
t_{or}	V_{OUT} Output Rise Time		—	40	—	ns
t_{of}	V_{OUT} Output Fall Time		—	55	—	ns

V_{DD}= 3.3V, Ta= 25°C

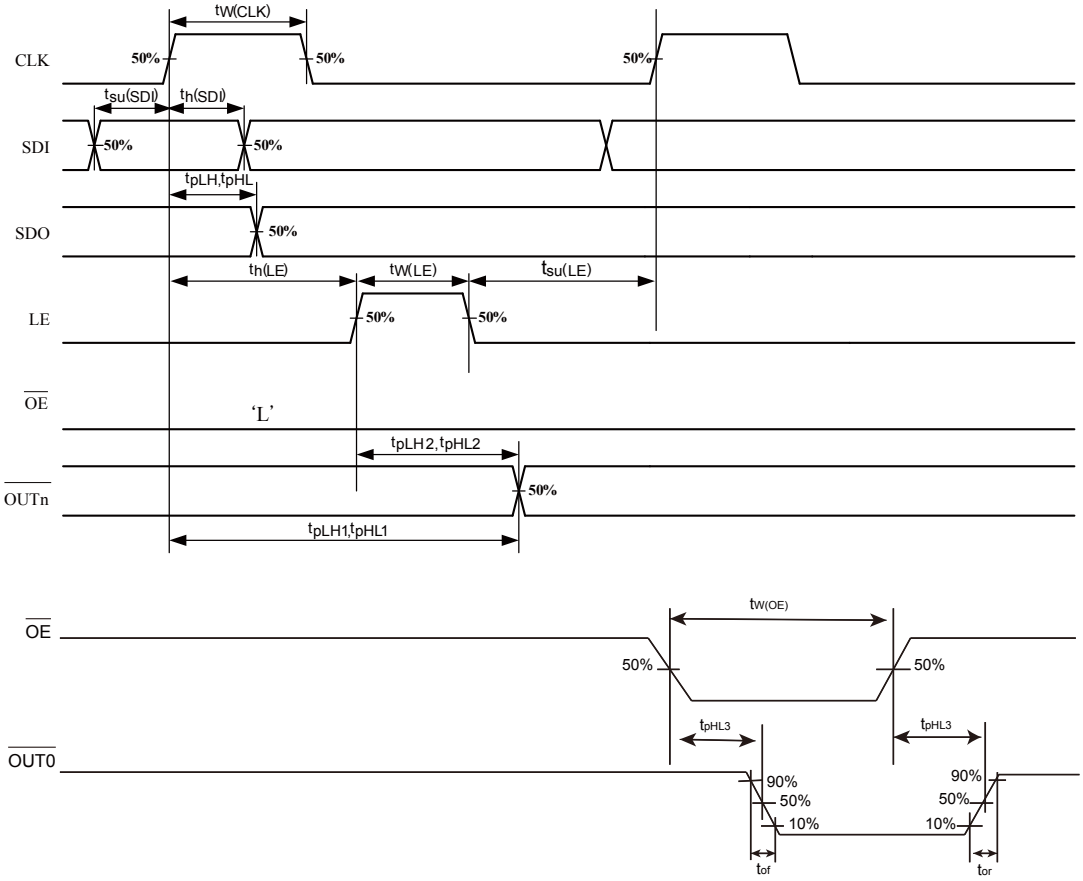
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay Time (“L” to “H”, CLK→SDO)	V_{DS}= 1.0V V_{IH}= V_{DD} V_{IL}= GND R_{ext}= 930Ω V_L= 3V R_L= 100Ω C_L= 10pF	—	20	40	ns
t_{PLH1}	Propagation Delay Time (“L” to “H”, CLK→$\overline{OUT2n}$		—	70	100	ns
	Propagation Delay Time (“L” to “H”, CLK→$\overline{OUT2n+1}$)		—	50	80	ns
t_{PLH2}	Propagation Delay Time (“L” to “H”, LE→$\overline{OUT2n}$)		—	70	100	ns
	Propagation Delay Time (“L” to “H”, LE→$\overline{OUT2n+1}$)		—	50	80	ns
t_{PLH3}	Propagation Delay Time (“L” to “H”, $\overline{OE}$→$\overline{OUT2n}$)		—	70	100	ns
	Propagation Delay Time (“L” to “H”, $\overline{OE}$→$\overline{OUT2n+1}$)		—	50	80	ns
t_{PHL}	Propagation Delay Time (“H” to “L”, CLK→SDO)		—	20	40	ns
t_{PHL1}	Propagation Delay Time (“H” to “L”, CLK→$\overline{OUT2n}$)		—	100	120	ns
	Propagation Delay Time (“H” to “L”, CLK→$\overline{OUT2n+1}$)		—	80	100	ns
t_{PHL2}	Propagation Delay Time (“H” to “L”, LE→$\overline{OUT2n}$)		—	100	120	ns
	Propagation Delay Time (“H” to “L”, LE→$\overline{OUT2n+1}$)		—	80	100	ns
t_{PHL3}	Propagation Delay Time (“H” to “L”, $\overline{OE}$→$\overline{OUT2n}$)		—	90	105	ns
	Propagation Delay Time (“H” to “L”, $\overline{OE}$→$\overline{OUT2n+1}$)		—	70	90	ns
$t_{W(CLK)}$	Pulse Width		20	—	—	ns
$t_{W(LE)}$	Pulse Width		20	—	—	ns
$t_{W(OE)}$	$\overline{OE}$ Pulse Width		100	130	—	ns
F_{CLK}	Data Clock Frequency		—	—	25	MHz
$t_{h(LE)}$	LE Hold Time		30	—	—	ns
$t_{su(LE)}$	LE Setup Time		5	—	—	ns
$t_{h(SDI)}$	SDI Hold Time		5	—	—	ns
$t_{su(SDI)}$	SDI Setup Time		3	—	—	ns
t_r	Maximum CLK Rise Time (See Note)		—	—	500	ns
t_f	Maximum CLK Fall Time (See Note)		—	—	500	ns
t_{or}	V_{OUT} Output Rise Time		—	40	—	ns
t_{of}	V_{OUT} Output Fall Time		—	60	—	ns

Note: The output channel exist 35ns delay time between odd numbers $\overline{OUT2n+1}$ and even numbers $\overline{OUT2n}$.

A.C. Characteristics Test Circuit



Timing Waveforms



Functional Description

Two operation methods are provided. The first is serial to serial operation which is used to transfer data in from an external microcontroller and transfer data out into another cascaded device. The other is serial to parallel operation which is used to transfer the device data to the external LED driver pins.

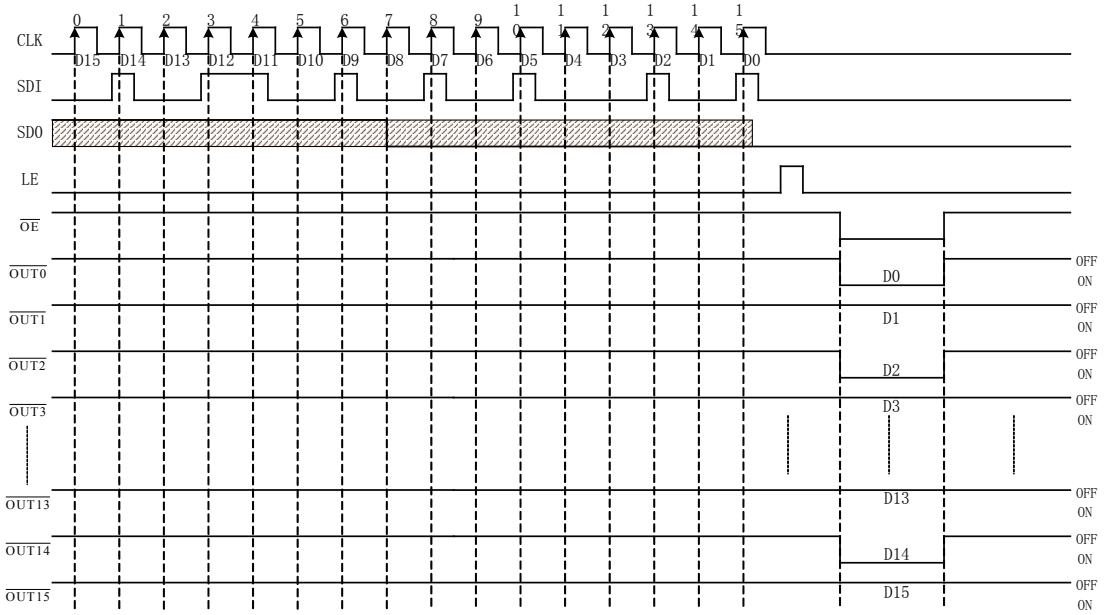
Serial-to-Serial Operation

The serial-to-serial function is implemented using the SDI and SDO pins. The SDI pin is used to receive serial input data for transfer into the LSB of the internal shift register while the SDO pin is used to transmit the MSB of the internal shift register to cascaded devices. Each bit of the data is shifted in from the SDI pin into the register on the rising edge of the CLK input signal where it will become the LSB of the internal shift register. At the same time, the SDO pin will shift out the MSB in the shift register to any connected cascaded devices.

Serial-to-Parallel Operation

If the LE pin is high and no clock is toggled on the CLK pin, then data will be latched from the shift register into an internal latch for transfer to the $\overline{OUT}$n pins. Data from the internal latch is transferred to the $\overline{OUT}$n pins using the $\overline{OE}$ pin. If the $\overline{OE}$ pin is low, then the data in the latch register will be transmitted to the output pins. The $\overline{OUT}$n pins can be disabled into a high state by setting the $\overline{OE}$ pin to a high level. The SDO pin will not be affected by the LE or $\overline{OE}$ pin status.

The following timing diagram illustrates both the serial-to-serial and serial-to-parallel operational waveform.



Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$....$\overline{OUT3}$.... $\overline{OUT15}$	SDO
↑	H	L	D_n	D_n.....D_{n-7}.....D_{n-15}	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	D_{n+2}.....D_{n-5}.....D_{n-13}	D_{n-13}
↓	X	L	D_{n+3}	D_{n+2}.....D_{n-5}.....D_{n-13}	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

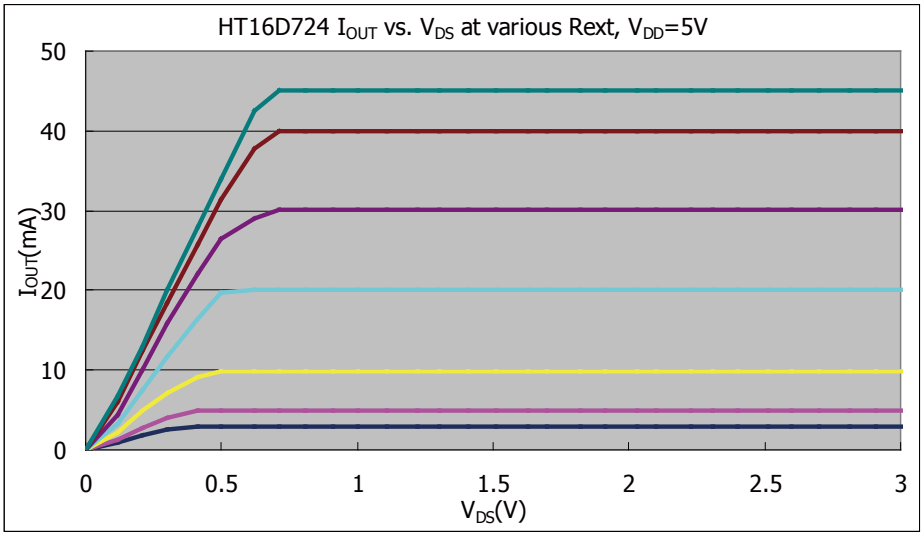
Constant Current Output

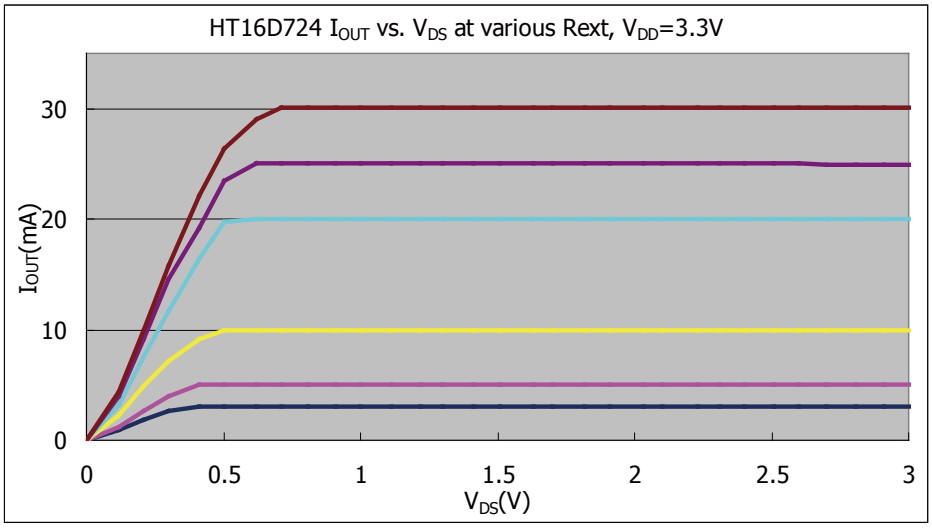
The output constant current for the output channels is set by a single external resistor, REXT, which is connected between the R-EXT pin and GND. The current level is set according to the value of this resistor. The current variation between channels is less than ±2.5% while the current variation between different devices is less than ±3%. The characteristic curve in the saturation region is flat and users can refer to the charts as shown below. The output current remains constant regardless of LED forward voltage (V_F) variations.

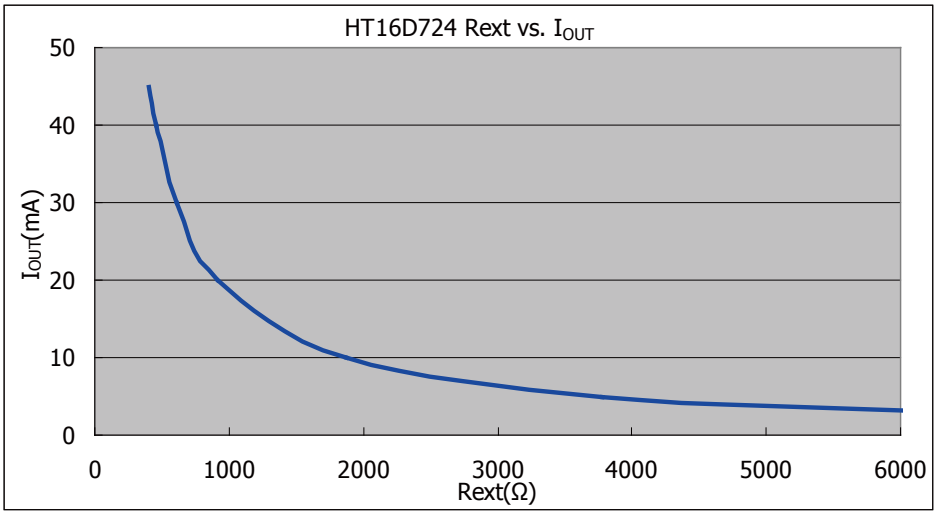
The constant current can be calculated using the following formula:

$$I_{OUT} = \frac{V_{R-EXT}}{R_{EXT}} \times M1 = \frac{18.9}{R_{EXT}}$$

The following I-V curve chart it provided for reference purposes.

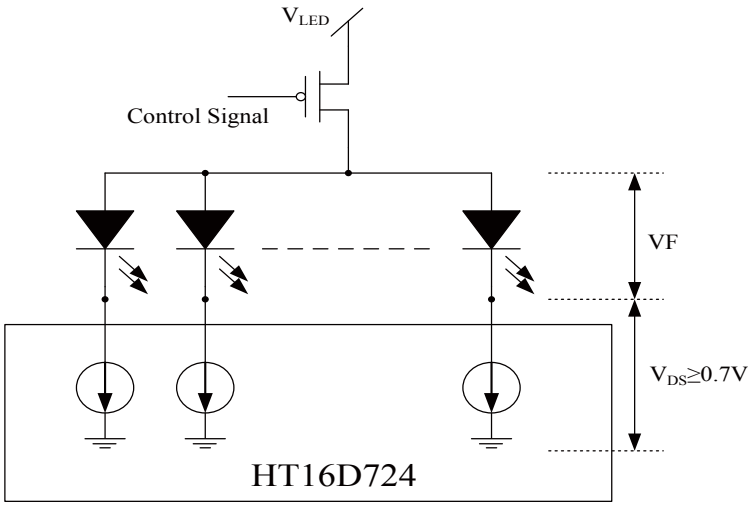




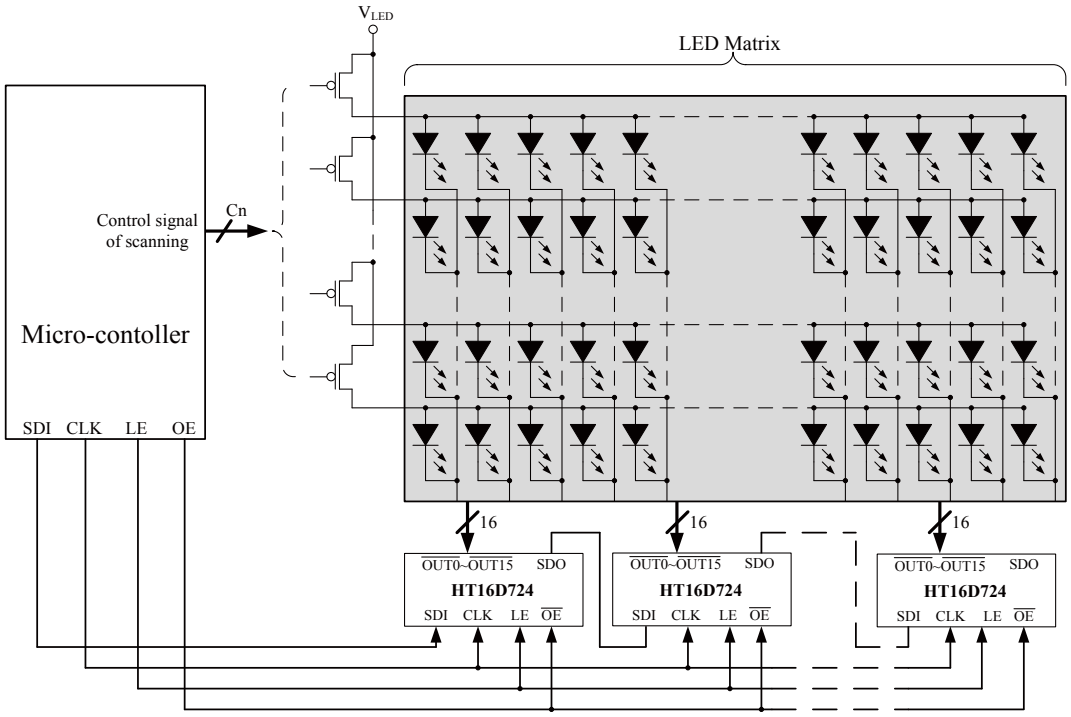


Load Supply Voltage (V_{LED})

HT16D724 can be operated very well when V_{DS} is set from 0.7V to 2V. It is recommended to use the lowest supply voltage (V_{LED}) to reduce the V_{DS} value in order to lower both the power consumption of HT16D724 and IC temperature.



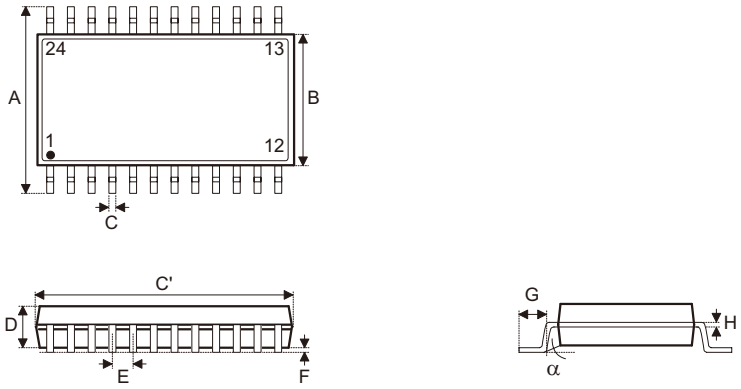
Application Circuit



Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website (http://www.holtek.com.tw/english/literature/package.pdf) for the latest version of the package information.

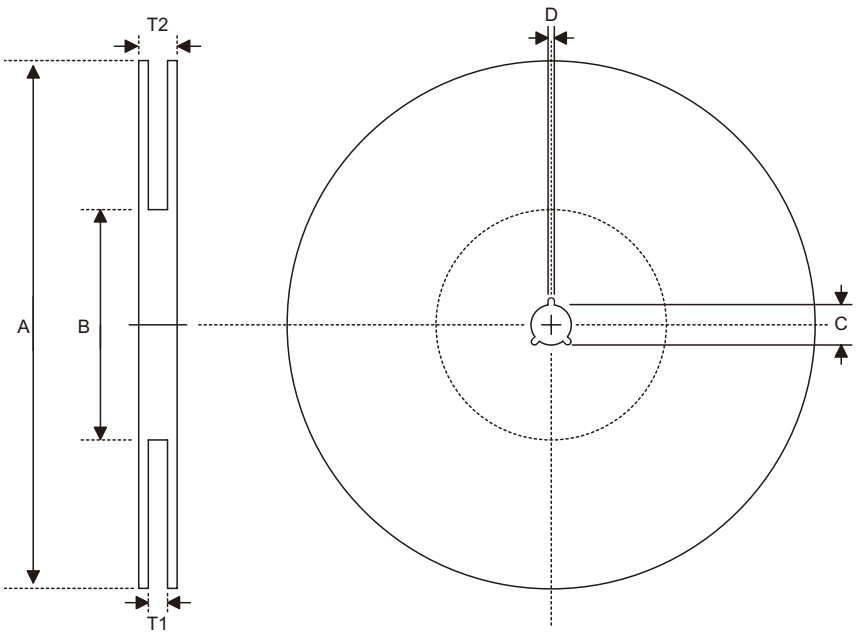
24-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.008	—	0.012
C′	0.335	—	0.346
D	0.054	—	0.060
E	—	0.025	—
F	0.004	—	0.010
G	0.022	—	0.028
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.20		0.30
C′	8.51	—	8.79
D	1.37	—	1.52
E	—	0.64	—
F	0.10	—	0.25
G	0.56	—	0.71
H	0.18	—	0.25
α	0°	—	8°

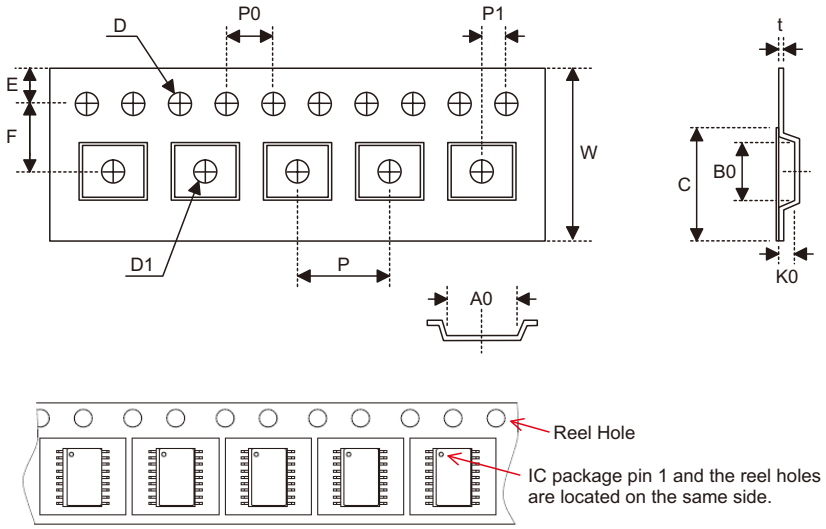
Reel Dimensions



SSOP 24S (150mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	$13.0^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flang	$16.8^{+0.3/-0.2}$
T2	Reel Thickness	22.2±0.2

Carrier Tape Dimensions



SSOP 24S (150mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$16.0^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.5±0.1
B0	Cavity Width	9.5±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	13.3±0.1

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