RAM Mapping 16*8 LED Controller Driver with keyscan

HT16K33

Revision: V.1.10 Date: May 16, 2011

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Table of Contents

Feature

- Operating voltage: 4.5V~5.5V
- Integrated RC oscillator
- I^2C-bus interface
- 16*8 bits RAM for display data storage
- Max. 16 x 8 patterns, 16 segments and 8 commons
- R/W address auto increment
- Max. 13 x 3 matrix key scanning
- 16-step dimming circuit
- Selection of 20/24/28-pin SOP package types

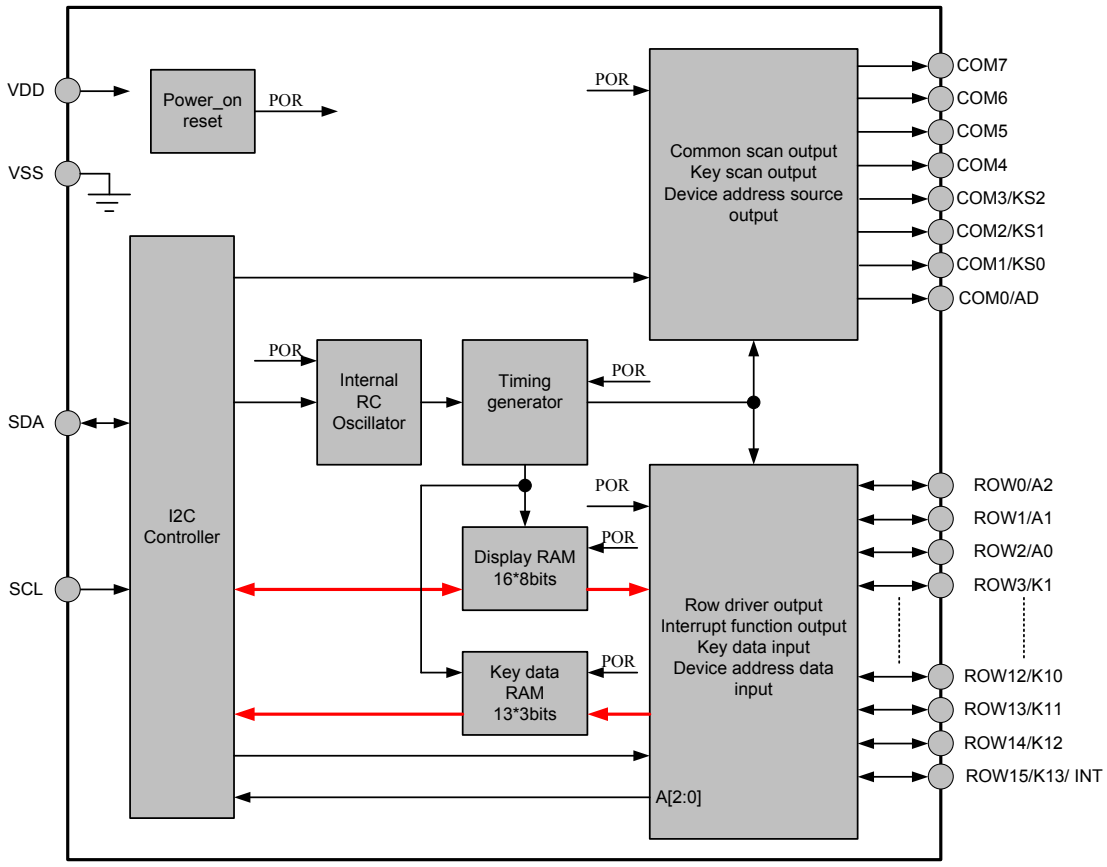
Applications

- Industrial control indicators
- Digital clocks, thermometers, counters, multimeters
- Combo sets
- VCR sets
- Instrumentation readouts
- Other consumer applications
- LED Displays

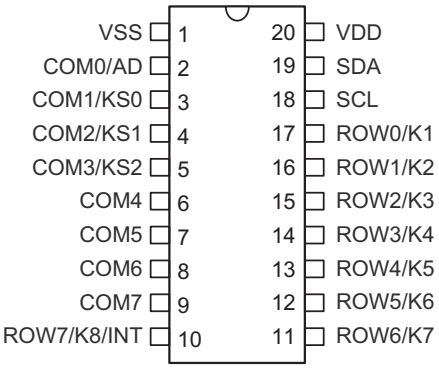
General Description

The HT16K33 is a memory mapping and multi-function LED controller driver. The max. Display segment numbers in the device is 128 patterns (16 segments and 8 commons) with a 13*3 (MAX.) matrix key scan circuit. The software configuration features of the HT16K33 makes it suitable for multiple LED applications including LED modules and display subsystems. The HT16K33 is compatible with most microcontrollers and communicates via a two-line bidirectional I^2C-bus.

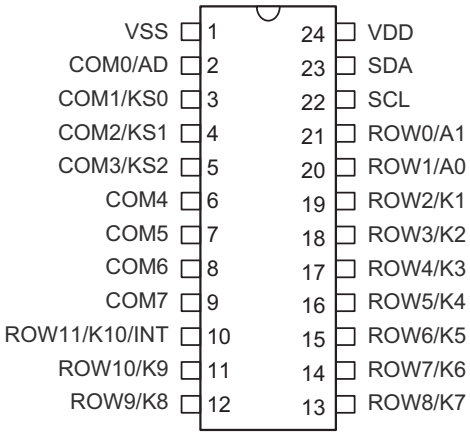
Block Diagram



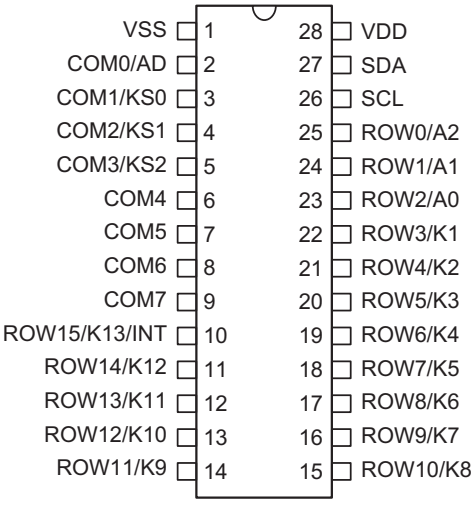
Pin Assignment



HT16K33
20 SOP-A



HT16K33
24 SOP-A

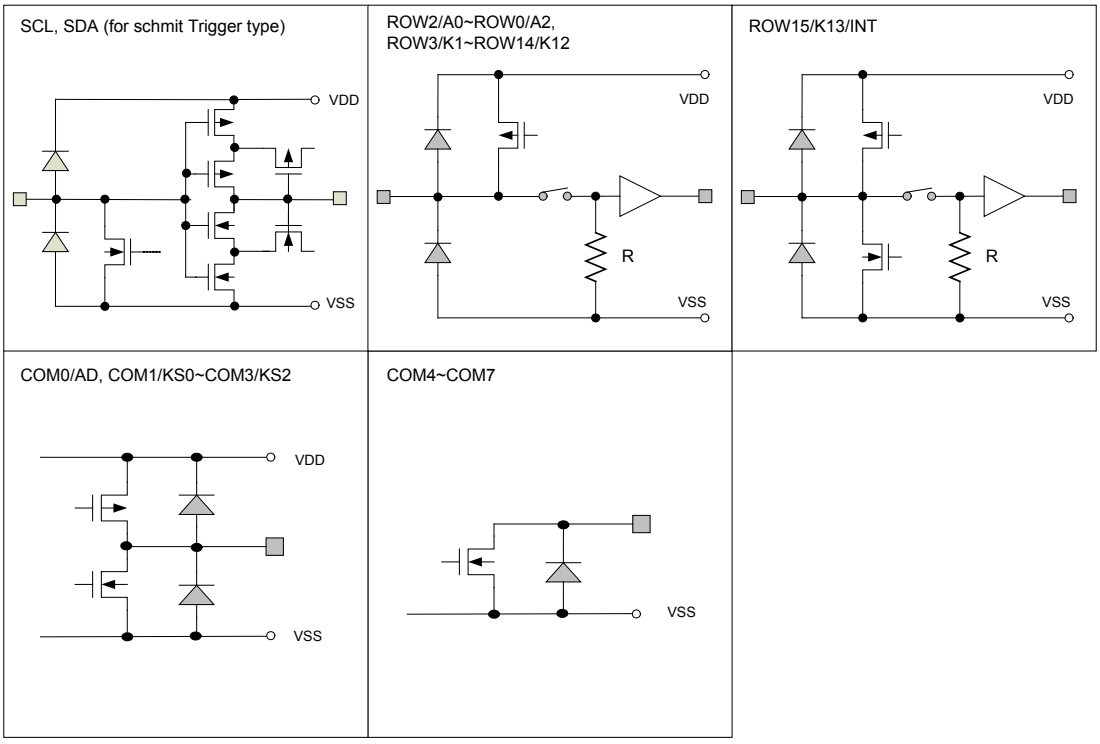


HT16K33
28 SOP-A

Pin Description

Pin Name	Type	Description
SDA	I/O	I^2C interface Serial Data Input/Output
SCL	I	I^2C interface Serial Clock Input
V_{DD}	—	Positive power supply for logic circuit
V_{SS}	—	Negative power supply for logic circuit, ground
COM0/AD	O	• Common output pin, active low during display • Also used as device address source output pin, active high during power on reset and key scan
COM1/KS0~COM3/KS2	O	• Common output pin, active low when displaying • Also used as the Key source output pin, active high during key scan operation
COM4~COM7	O	• Common outputs pin, active low during display.
28 Pin package		
ROW0/A2~ROW2/A0	I/O	• ROW output pin, active high when displaying • Also used as the device address data input pin, internal pull-low during power on reset and during key scan operation
ROW3/K1~ROW14/K12	I/O	• ROW outputs pin, active high during display. • Also used as the Key data input pin, internal pull-low during key scan operation
ROW15/K13 /INT	I/O	• When the “INT/ROW” bit of ROW/INT set register is set to “0”, this pin become a Row driver output pin, active high when displaying, and Key data input during key scan operation. • When the “INT/ROW” bit of ROW/INT set register is set to “1”, this pin become Interrupt signal (INT) output pin. • INT pin output active-high when the “act” bit of the Row/int setup register is set to “0”. • INT pin output active-high when the “act” bit of the ROW/INT register is set to “1”.
24 Pin package		
ROW0/A1~ROW1/A0	I/O	• ROW output pin, active high when displaying • Also used as the device address data input pin, internal pull-low during a power on reset and during a key scan operation
ROW2/K1~ROW10/K9	I/O	• ROW outputs pin, active high when displaying • Also used as the Key data inputs pin, internal pull-low during a key scan operation
ROW11/K10/INT	I/O	• When the “INT/ROW” bit of ROW/INT set register is set to “0”, this pin become a Row driver output, active high when displaying, and Key data input during a keyscan operation • When the “INT/ROW” bit of ROW/INT set register is set to “1”, this pin become an Interrupt signal (INT) output pin. • INT pin output active-high when the “act” bit of the Row/int setup register is set to “0”. • INT pin output active-high when the “act” bit of the Row/int setup register is set to “1”.
20 Pin package		
ROW0/K1~ROW6/K7	I/O	• ROW output pin, active high when displaying • Also used as the Key data inputs pin, internal pull-low during a key scan operation
ROW7/K8 /INT	I/O	• When the “INT/ROW” bit of the ROW/INT setup register is set to “0”, this pin become a Row driver output, active high when displaying, and Key data input during a key scan operation • When the “INT/ROW” bit of the ROW/INT set register is set to “1”, this pin become an Interrupt (INT) signal output pin • INT pin output active-high when the “act” bit of ROW/INT setup register is set to “0” • INT pin output active-high when the “act” bit of the ROW/INT set register is set to “1”

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.5V
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Storage Temperature ..... -50°C to 125°C
Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{DD} =4.5~5.5V; Ta=25°C (Unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	4.5	5	5.5	V
I_{DD}	Operating Current	5	No load, normal operation, INT/ROW bit is set to "0"	—	1	2	mA
I_{STB}	Standby Current	5	No load, standby mode	—	1	10	μA
V_{IH}	Input high Voltage	5	SDA,SCL	$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	Input Low Voltage	5	SDA, SCL	0	—	$0.3V_{DD}$	V
I_{IL}	Input leakage current	—	V_{IN} = V_{SS} or V_{DD}	-1	—	1	μA
R_{PL}	Input pull-low resistor	5	ROW3/K1~ROW15/K13, ROW0/A2~ROW2/A0 Keyscan during	250	—	—	KΩ
I_{OL1}	Low level output current	5	V_{OL}=0.4V; SDA	6	—	—	mA
I_{OL2}	ROW Sink Current	5	V_{OL}=0.4V, INT pin	6	—	—	mA
I_{OH1}	ROW Source Current	5	V_{OH}=V_{DD}-2V, (ROW0~ROW15 pin)	-20	-25	-40	mA
			V_{OH}=V_{DD}-3V, (ROW0~ROW15 pin)	-25	-30	-50	mA
I_{math}	ROW Source Current tolerance	5	V_{OH}=V_{DD}-3V, (ROW0~ROW15 pin)	—	—	5	%
I_{OL3}	COM Sink Current	5	V_{OL}=0.3V, (COM0~COM7 pin)	160	200	—	mA
I_{OH2}	COM Source Current	5	V_{OH}=V_{DD}-2V, (COM0~COM3 pin)	-20	-25	-40	mA

A.C. Characteristics

V_{DD} =4.5~5.5V; Ta=25°C (Unless otherwise specified)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
t_{LED}	LED Frame time	5	1/9 Duty	7.6	9.5	11.4	ms
t_{OFF}	V_{DD} OFF Time	—	V_{DD} drop down to 0V	20	—	—	ms
t_{SR}	V_{DD} Slew Rate	—	—	0.05	—	—	V/ms

Note: 1. If the Power on Reset timing conditions are not satisfied in the power ON/OFF sequence, the internal Power on Reset circuit will not operate normally.

2. If VDD drops below the minimum voltage of the operating voltage spec. during operating, the Power on Reset timing conditions must also be satisfied. That is, VDD must drop to 0V and remain at 0V for 20ms (min.) before rising to the normal operating voltage.

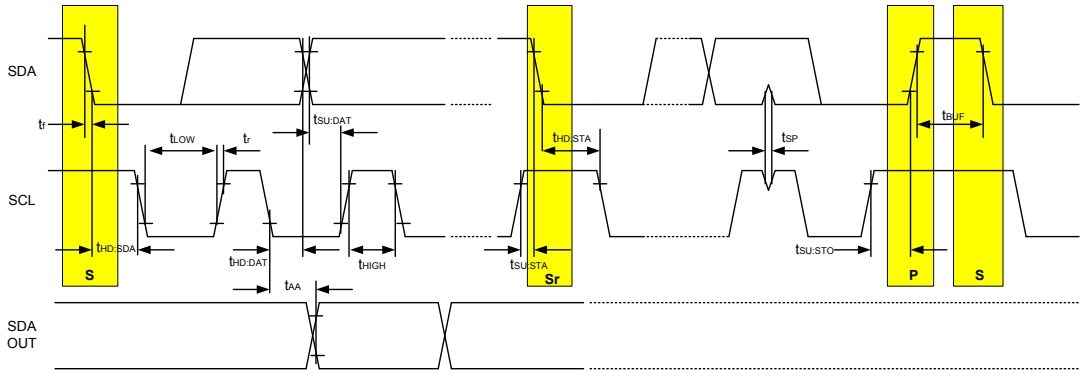
A.C. Characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
		condition			
f_{SCL}	Clock frequency	—	—	400	kHZ
t_{BUF}	Bus free time	Time in which the bus must be free before a new transmission can start	1.3	—	μs
$t_{HD;\ STA}$	Start condition hold time	After this period, the first clock pulse is generated	0.6	—	μs
t_{LOW}	SCL Low time	—	1.3	—	μs
t_{HIGH}	SCL High time	—	0.6	—	μs
$t_{SU;\ STA}$	Start condition set-up time	Only relevant for repeated START condition.	0.6	—	μs
$t_{HD;\ DAT}$	Data hold time	—	0	—	μs
$t_{SU;\ DAT}$	Data set-up time	—	100	—	ns
t_r	Rise time	Note	—	0.3	μs
t_f	Fall time	Note	—	0.3	μs
$t_{SU;\ STO}$	Stop condition set-up time	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	50	ns

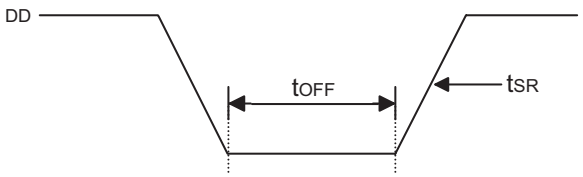
Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

- **I²C Timing**



- **Power-on Reset Timing**



Functional Description

Power-on Reset

When power is applied, the IC is initialised by an internal power-on reset circuit. The status of the internal circuit after initialisation is as follows:

- System Oscillator will be in an off state
- COM0~COM3 outputs are set to V_{DD}
- COM4~COM7 outputs will be high impedance
- All Rows pins are changed input pins
- LED Display is in the off state.
- Key scan stopped
- The combined Row/INT pins are setup as ROW outputs
- Dimming is set to 16/16duty

Data transfers on the I^2C-bus should be avoided for 1 ms following a power-on to allow completion of the reset action.

Standby Mode

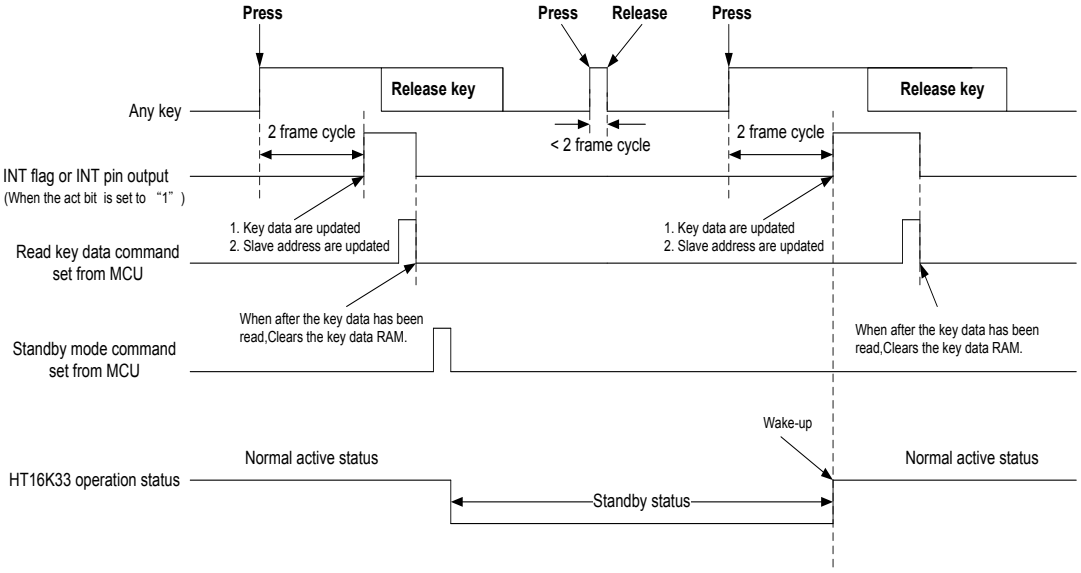
In the standby mode, the HT16K33 can not accept input commands nor write data to the display RAM except using the system setup command.

If the standby mode is selected with the "S" bit of the system setup register set to "0", the status of the standby model is as follows:

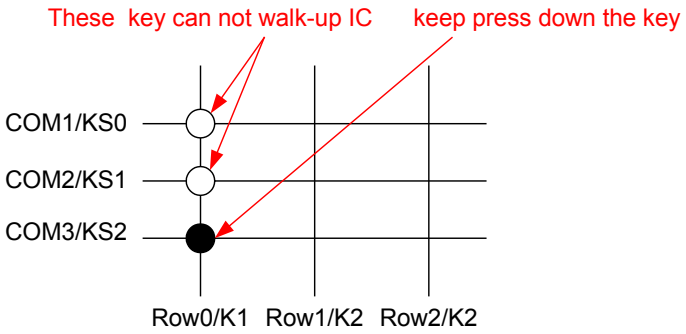
- System Oscillator will be in the off state
- COM0~COM3 outputs are set to VDD
- COM4~COM7 outputs will be high impedance
- LED Display is in the off state.
- Key scan stopped
- All key data and INT flags are cleared until the standby mode is canceled.
- If the key matrix is activated (any key) or the "S" bit of the system setup register is set to "1", the standby mode will be canceled and will cause the device to wake-up.
- If the "INT/ROW" bit of the ROW/INT setup register is set to "0", all rows pins are changed to input pins.
- If the "INT/ROW" bit of the ROW/INT setup register is set to "1": all rows pins are changed to input pins except for the INT pin (output).
- The INT pin output will remain at a high level when the "act" bit of the ROW/INT setup register is set to "0".
- The INT pin output remains at a low level when the "act" bit of the ROW/INT setup register is set to "1".

Wake-up

- Wake-up by a key press from any key or by setting the "S" bit of the system setup register to "1". A key scan will then be performed.
- The System Oscillator restarts for normal operation.
- The previous display data output will be updated by Each Mode command set.
- The relationship between the Wake-up and any key press is shown as follows:



- In the sleep mode, KS0-K1 or KS1-K1 can not wake-up the device when the KS2-K1 keys are kept pressed down. It is a prohibited application as shown in the following figure.



System Setup Register

The system setup register configures system operation or standby for the HT16K33.

- The internal system oscillator is enabled when the 'S' bit of the system setup register is set to "1".
- The internal system clock is disabled and the device will enter the standby mode when the "S" bit of the system setup register is set to "0".
- Before the standby mode command is sent, it is strongly recommended to read the key data first.
- The system setup register command is shown as follows:

Name	Command / Address / Data								Option	Description	Def.
	D15	D14	D13	D12	D11	D10	D9	D8			
System set	0	0	1	0	X	X	X	S	{S} Write only	Defines internal system oscillator on/off • {0}:Turn off System oscillator (standby mode) • {1}:Turn on System oscillator (normal operation mode)	20H

ROW/INT Set Register

The ROW/INT setup register can be set to either an LED Row output, or an INT logic output.

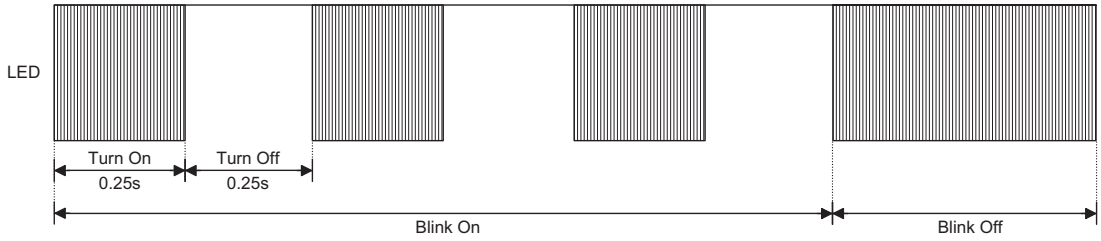
- The INT output is selected when the ROW/INT set register is set to "1".
- The ROW output is selected when the ROW/INT set register is set to "0".
- The INT logic output can be configured as an INT output level controlled by the keyscan circuitry and controlled through the 2-wire interface.
- The INT output is active-low when the 'act' bit of ROW/INT set register is set to "0".
- The INT output is active-high when the 'act' bit of ROW/INT set t register is set to "1".
- The ROW/INT setup register command is shown as follows:

Name	Command / Address / Data								Option	Description	Def.
	D15	D14	D13	D12	D11	D10	D9	D8			
row/int set	1	0	1	0	X	X	act	row/ int	{act, row/int } Write only	• Defines INT/ROW output pin select and INT pin output active level status. • {X 0}: INT/ROW output pin is set to ROW driver output. • {0, 1}: INT/ROW output pin is set to INT output, active low. • {1, 1}: INT/ROW output pin is set to INT output, active high.	A0H

Display Setup Register

The display setup register configures the LED display on/off and the blinking frequency for the HT16K33.

- The LED display is enabled when the 'D' bit of the display setup register is set to "1".
- The LED display is disabled when the 'D' bit of the display setup register is set to "0".
- In the display disable status, all ROW outputs are hi-impedance and all COM outputs are high-impedance during the display period.
- In the display disable status, all ROWs are changed to an input status and the COM0~COM3 continues scanning and COM4~COM7 outputs are high-impedance during the keyscan period.
- The display blinking capabilities of the HT16K33 are very versatile. The whole display can be blinked at frequencies selected by the Blink command. The blinking frequencies are integer multiples of the system frequency; the ratios between the system oscillator and the blinking frequencies depend upon the mode in which the device is operating, is as follows:
- Blinking frequency = 2Hz



Example of Waveform for Blinker

- The display setup register command is as follows:

Name	Command / Address / Data								Option	Description	Def.
	D15	D14	D13	D12	D11	D10	D9	D8			
Display set	1	0	0	0	X	B1	B0	D	{D} Write only	Defines Display on/off status. ● {0}: Display off ● {1}: Display on	80H
									{B1,B0} Write only	Defines the blinking frequency ● {0,0} = Blinking OFF ● {0,1} = 2HZ ● {1,0} = 1HZ ● {1,1} = 0.5HZ	

System Oscillator

- The internal logic and the LED drive signals of the HT16K33 are timed by the integrated RC oscillator.
- The System Clock frequency determines the LED frame frequency. A clock signal must always be supplied to the device; removing the clock may freeze the device if the standby mode command is executed. At initial system power on, the System Oscillator is in the stop state.

Display Data Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialisation of the address pointer by the address pointer command.

Key Data Address Pointer

The addressing mechanism for the key data RAM is implemented using the address pointer. This allows the loading of an individual key data byte, or a series of key data bytes, into any location of the key data RAM. The sequence commences with the initialisation of the address pointer by the Address pointer command.

Register Information Address Pointer

The addressing mechanism for the register data and Interrupt flag information RAM is implemented using the address pointer. This allows the loading of an individual register data and Interrupt flag data byte, or a series of register data and Interrupt flag data bytes, into any location of the register data and Interrupt flag information RAM. The sequence commences with the initialisation of the address pointer by the Address pointer command.

Row Driver Outputs

The LED drive section includes 16 ROW outputs ROW0 to ROW15 which should be connected directly to the LED panel. The Row output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. When less than 15 ROW outputs are required the unused Row outputs should be left open-circuit.

Column Driver Outputs

The LED drive section includes eight column outputs COM0 to COM7 which should be connected directly to the LED panel. The column output signals are generated in accordance with the selected LED drive mode. When less than 8 column outputs are required the unused column outputs should be left open-circuit.

Display Memory – RAM Structure

- The display RAM is a static 16 x 8 -bits RAM which stores the LED data. Logic "1" in the RAM bit-map indicates the "on" state of the corresponding LED Row; similarly, a logic 0 indicates the "off" state.
- There is a one-to-one correspondence between the RAM addresses and the Row outputs, and between the individual bits of a RAM word and the column outputs. The following shows the mapping from the RAM to the LED pattern:

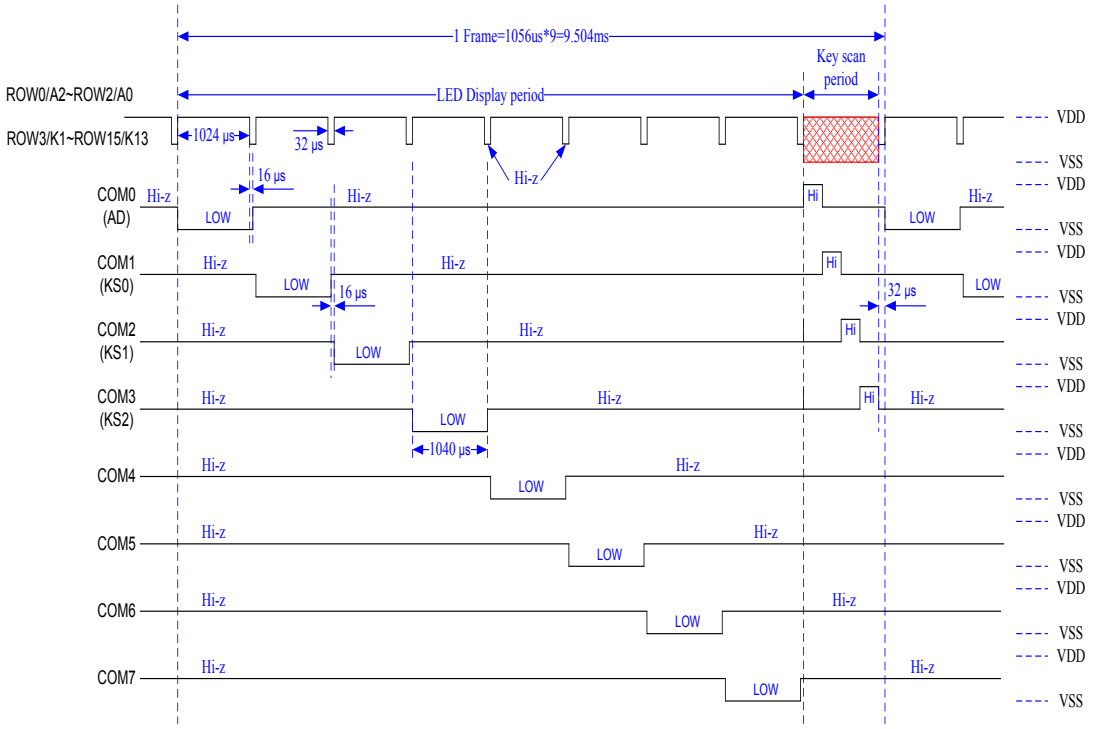
COM0	ROW0	ROW7	ROW8	ROW15
COM0	00H		01H	
COM1	02H		03H	
COM2	04H		05H	
COM3	06H		07H	
COM4	08H		09H	
COM5	0AH		0BH	
COM6	0CH		0DH	
COM7	0EH		0FH	

- I^2C bus display data transfer format

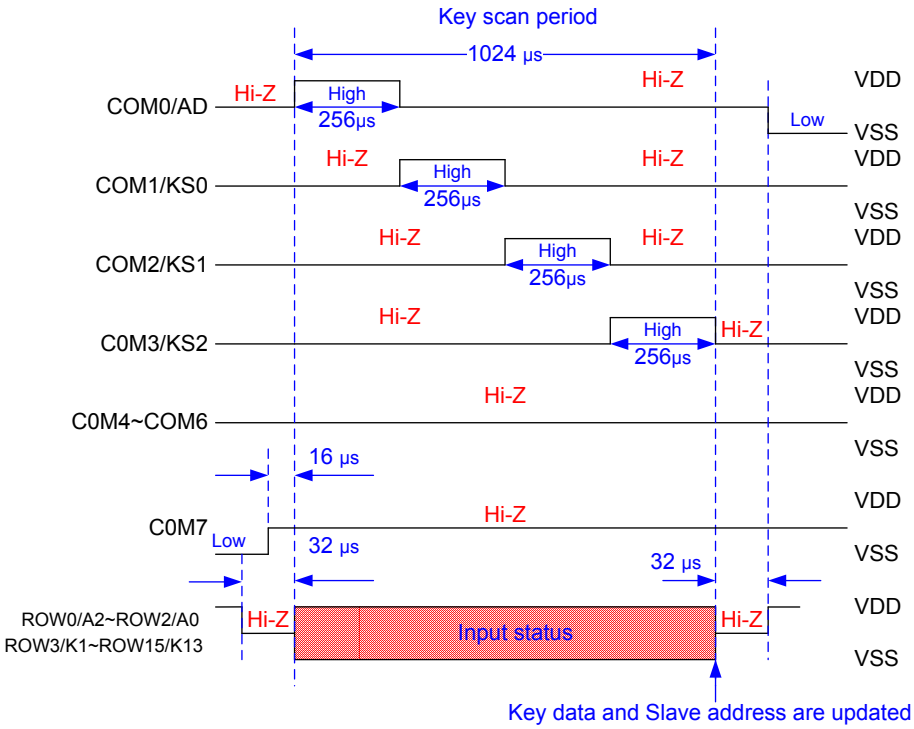
Data byte of I^2C	D7	D6	D5	D4	D3	D2	D1	D0
ROW	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8

LED drive mode waveforms and scanning is as follows:

- The HT16K33 allows use of 1/9 duty mode and the combined ROW/INT pin is set to a ROW driver output as shown:



- Key scan period enlargement



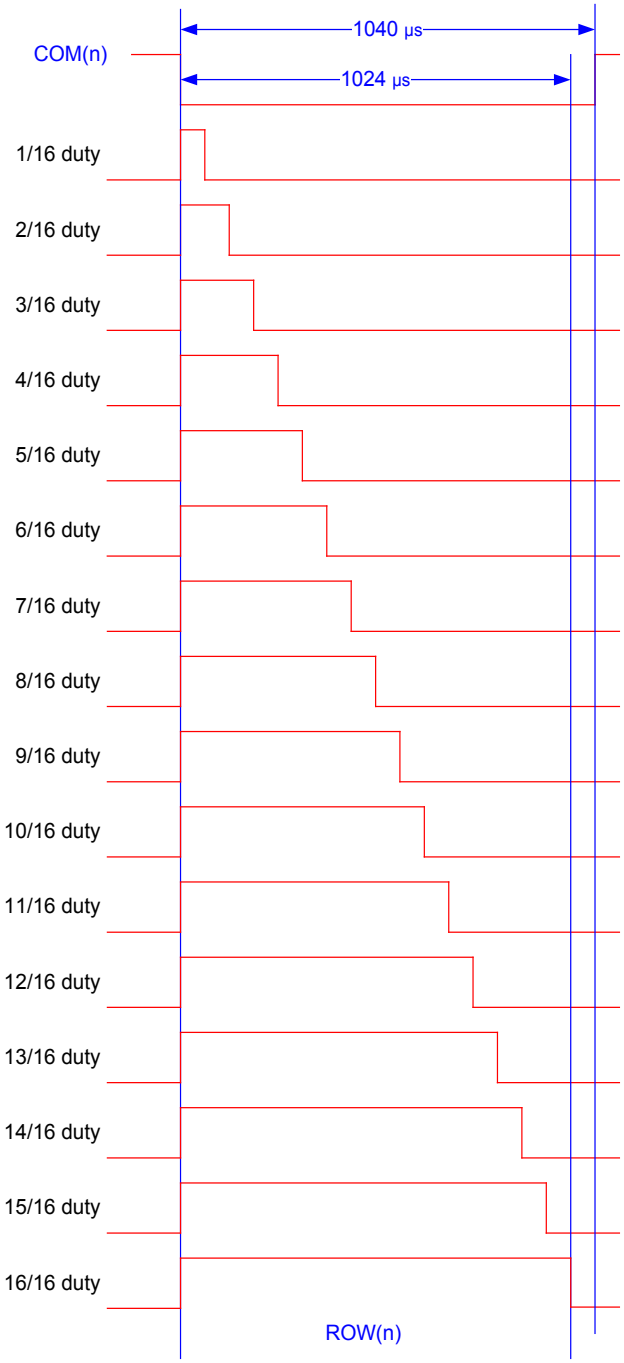
Note: The ROW/IN combined pin is set to a Row driver output.

Digital Dimming Data Input

The Display Dimming capabilities of the HT16K33 are very versatile. The whole display can be dimmed using pulse width modulation techniques for the ROW driver by the Dimming command, as shown:

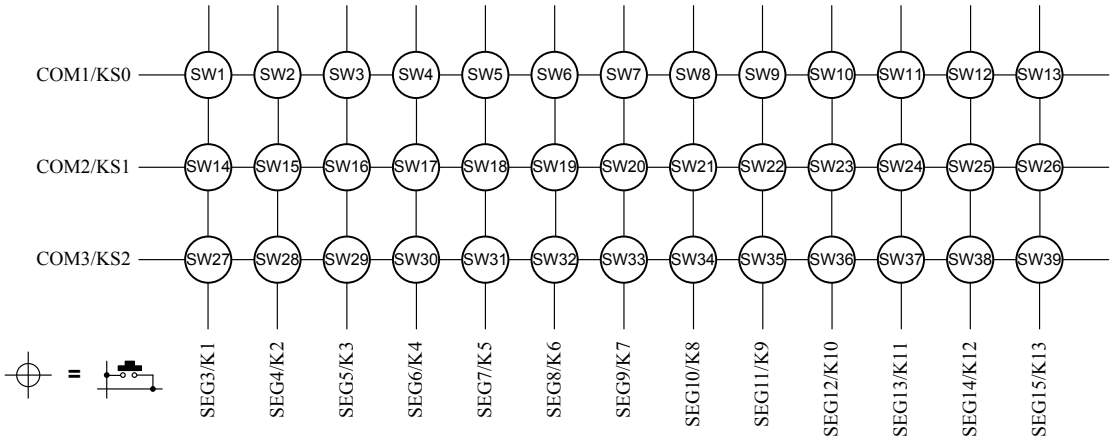
D15	D14	D13	D12	D11	D10	D9	D8	ROW driver output pulse width	Def.
1	1	1	0	P3	P2	P1	P0		
1	1	1	0	0	0	0	0	1/16 duty	—
1	1	1	0	0	0	0	1	2/16 duty	—
1	1	1	0	0	0	1	0	3/16 duty	—
1	1	1	0	0	0	1	1	4/16 duty	—
1	1	1	0	0	1	0	0	5/16 duty	—
1	1	1	0	0	1	0	1	6/16 duty	—
1	1	1	0	0	1	1	0	7/16 duty	—
1	1	1	0	0	1	1	1	8/16 duty	—
1	1	1	0	1	0	0	0	9/16 duty	—
1	1	1	0	1	0	0	1	10/16 duty	—
1	1	1	0	1	0	1	0	11/16 duty	—
1	1	1	0	1	0	1	1	12/16 duty	—
1	1	1	0	1	1	0	0	13/16 duty	—
1	1	1	0	1	1	0	1	14/16 duty	—
1	1	1	0	1	1	1	0	15/16 duty	—
1	1	1	0	1	1	1	1	16/16 duty	Y

- **The relationship between ROW and COM Digital Dimming duty time is as follows:**



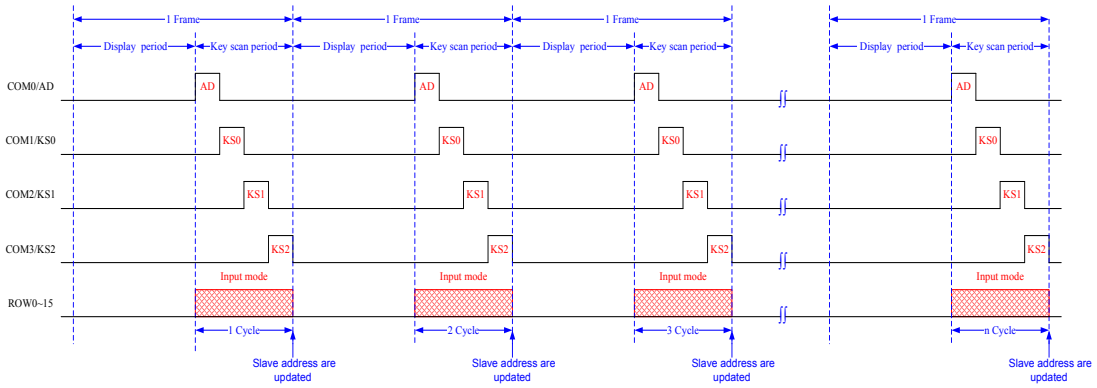
Keyscan

- The keyscan logic uses one, two or three of the KS0, KS1and KS2 logic outputs. An interrupt output that flags a key press is optional. The INT flag can be read (polled) through the serial interface, allowing INT/ROW15 to be used as a general purpose logic output or as a ROW open-drain driver.
- One small-signal diode is required per key switch when more than one key is connected to KS0, KS1 or KS2. The diodes prevent two simultaneous key switch depressions from shorting the COM drivers together. For example, if SW1 and SW14 were pressed together and the diodes were not fitted, COM1/KS0 and COM2/KS1 would be shorted together and the LED multiplexing would be incorrect.
- The keyscanning circuit utilises the COM1/KS0 to COM3/KS2 outputs high as the keyscan output drivers. The outputs COM0 to COM7 pulse low sequentially as the displays are multiplexed. The actual low time varies from 64μs to 1024μs due to pulse width modulation from 1/16th to 16/16th for dimming control. The LED drive mode waveforms and scanning shows the typical situation when all eight LED cathode drivers are used.
- The maximum of thirty-nine keys can only be scanned if the scan-limit register is set to scan the maximum KS0 to KS2.
- The keyscan cycle loops continuously over time, with all thirty-nine keys experiencing a full keyscanning debounce over 20ms. A key press is debounced and an interrupt issued if at least one key that was not pressed in a previous cycle is found to be pressed during both sampling periods.
- The keyscan circuit detects any combination of keys pressed during each debounce cycle (n-key rollover).
- The INT output is active-low when the “act” bit of row/int set register is set to “0”.
- The INT output is active-high when the “act” bit of row/int set register is set to “1”.



Keyscan Timing

The Slave addresses are updated on the keyscan timing as shown:



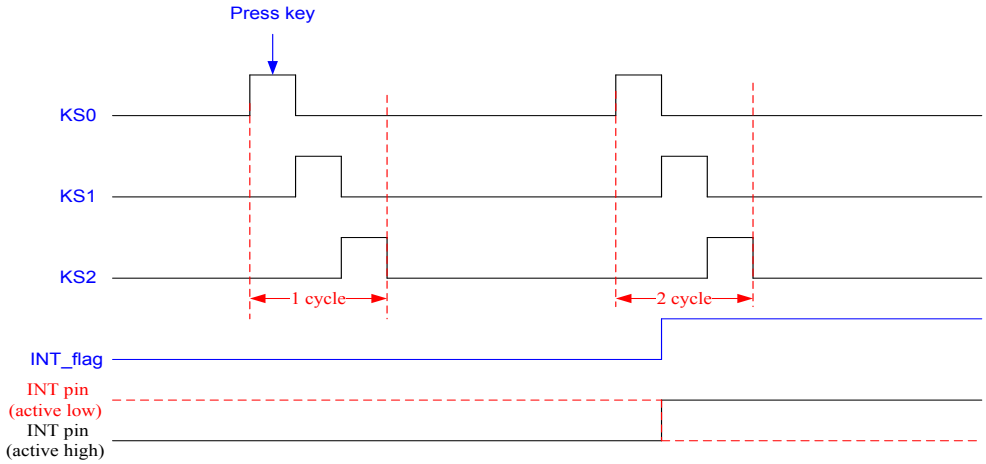
Keyscan & INT Timing

- The key data is updated and the INT function is changed for keys that have been pressed after 2 key-cycles.
- The INT function is changed when the first key has been pressed.
- When after all the key data has been read that clears the key data RAM and the int flag bit is set to "0", the INT pin goes to low when the "act" bit of the row/int set register is set to "1".
- When after all the key data has been read that clears the key data RAM and the int flag bit is set to "0", the INT pin goes to high when the "act" bit of the row/int setup register is set to "0".
- The INT flag register is shown below.
- I^2C bus display data transfer format

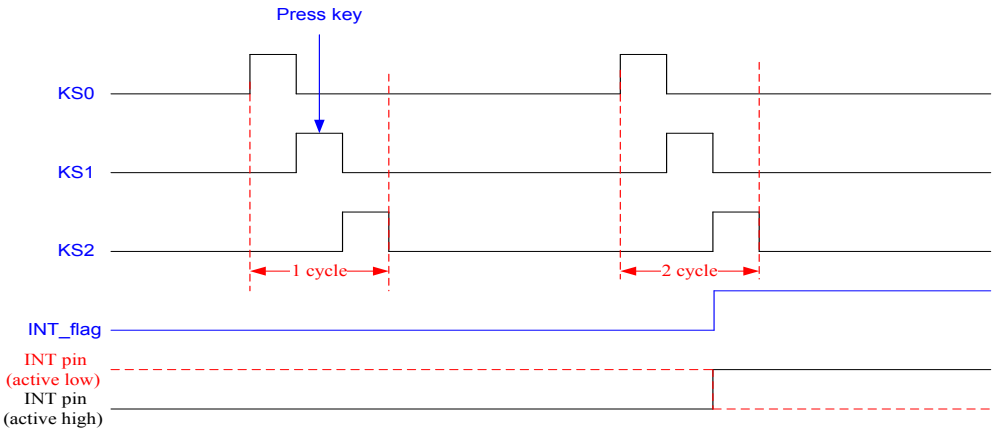
	D7	D6	D5	D4	D3	D2	D1	D0
INT flag register (address point at 60H)	INT flag	INT flag	INT flag	INT flag	INT flag	INT flag	INT flag	INT flag

- The relationship between keyscan signal to the INT signal time is shown below:

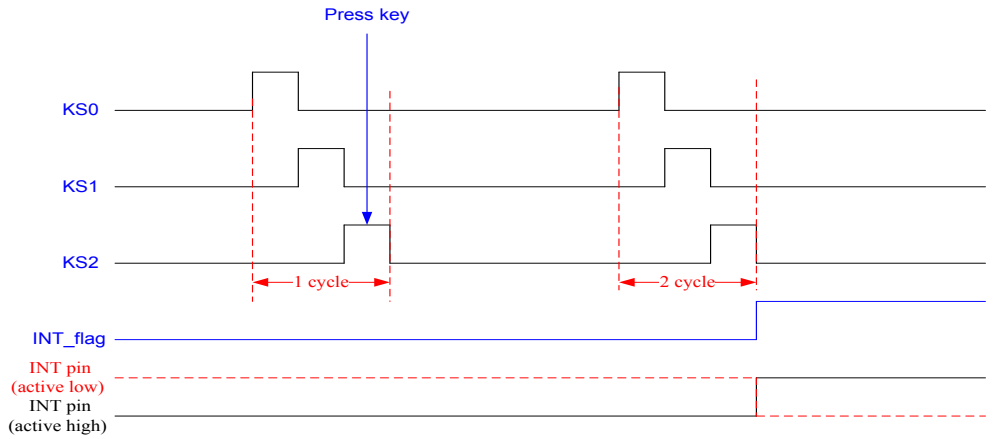
  1. When a key is pressed on the KS0 row



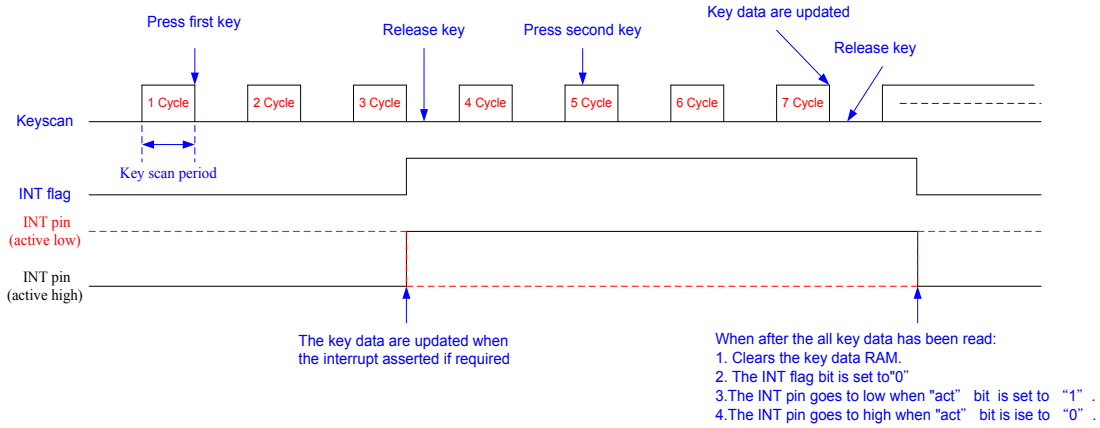
2. When a key is pressed on the KS1 row



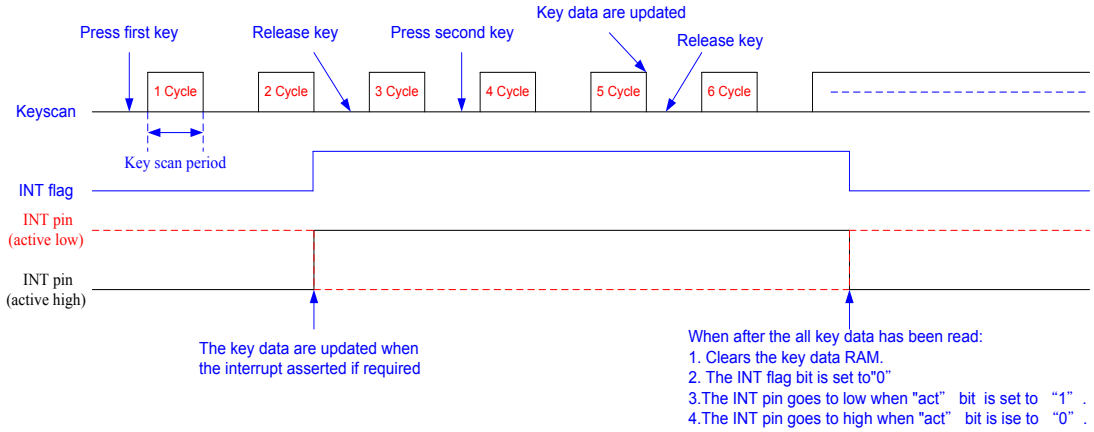
3. When a key is pressed on the KS2 row



- Key pressed during a keyscan cycle period. (i.e. the key is pressed on the KS2 row)



- Key pressed during an LED display period. (i.e. the key is pressed on the KS2 row)



Key Data Memory – RAM Structure

- The RAM is a static 16 x 3 -bits RAM which stores key data which keys have been detected as key data by the key scanning circuit. Each bit in the register corresponds to one key switch. The bit is set to 1 if the switch has been correctly key data since the last key data register read operation.
- Reading the key data RAM clears the key data RAM after the key data has been read, so that future key presses can be identified. If the key data RAM is not read, the key scan data accumulates. There is no FIFO register in the HT16K33. Key-press order, or whether a key has been pressed more than once, cannot be determined unless the all key data RAM is read after each interrupt and before completion of the next keyscan cycle.
- After the all key data RAM has been read, the INT pin output is cleared along with the INT flag status. If a key is pressed and held down, the key is reported as key data (and an INT is issued) only once. The key must be detected as released by the keyscanning circuit before it is key data again.
- The key data RAM is read only. A write to address 0x40~0x45 is ignored.
- It is strongly recommended that the key data RAM is read only and should be started form address 0X40H only, the key data RAM of address 0X40H ~0X45H should be read continuously and in one operation.
- There is a one-to-one correspondence between the key data RAM addresses and the Key data outputs and between the individual bits of a key data RAM word and the key data outputs. The following shows the mapping from the RAM to the key data output:

ROW3~15	K1 K8	K9 K16
COM1/KS0	40H	41H
COM2/KS1	42H	43H
COM3/KS2	44H	45H

- I^2C bus display data transfer format

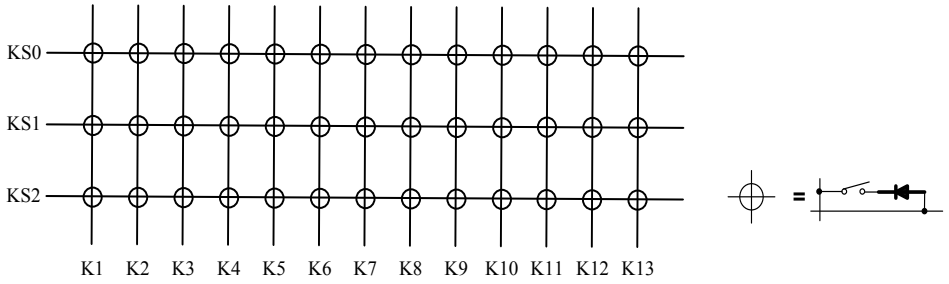
Data byte of I^2C	D7	D6	D5	D4	D3	D2	D1	D0
KS0	K8	K7	K6	K5	K4	K3	K2	K1
	0	0	0	K13	K12	K11	K10	K9
KS1	K8	K7	K6	K5	K4	K3	K2	K1
	0	0	0	K13	K12	K11	K10	K9
KS2	K8	K7	K6	K5	K4	K3	K2	K1
	0	0	0	K13	K12	K11	K10	K9

KEY MATRIX CONFIGURATION

An example of key matrix configurations is shown below.

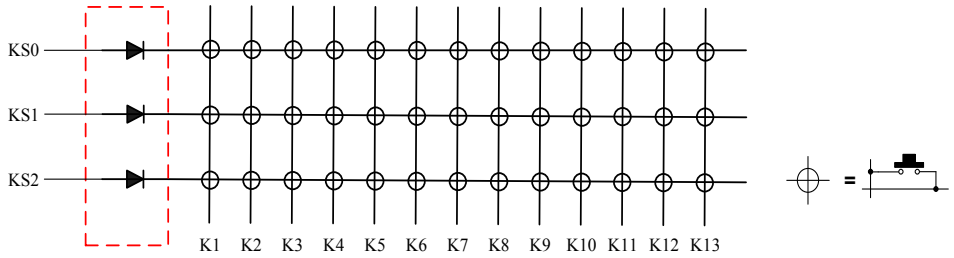
When pressing three or more times is assumed:

A configuration example is shown below. In this configuration, 1 to 39 ON switches can be recognised.

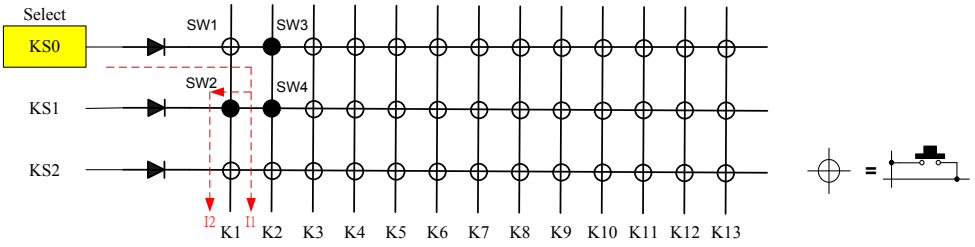


When pressing twice or more times is assumed:

A configuration example is shown below. In this configuration, 0 to 2 ON switches can be recognised.



- In this configuration, pressing three or more times may cause the OFF switches to be determined as being ON.
  For example, if SW2, SW4 are ON and KS0 has been selected (high level) as shown below, SW3, in which current I1 is running is supposed to be detected to be ON. However, since SW2 and SW4 are ON, current I2 runs thus resulting in SW1 to be recognised as being ON (ghost key).

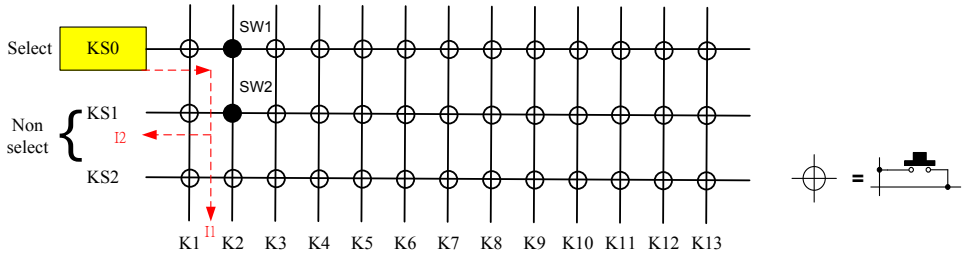


- If a diode is not available, not only the key data may not be read normally but the LED display may be affected or the ICs may be damaged.
  For example, if SW1 and SW2 are ON and KS0 has been selected (high level) as shown below, this will cause not only current I1 which is supposed to run but also a short-circuit current I2 of KS0 to KS1 to flow.

  It is possible that this will then cause the following two problems:

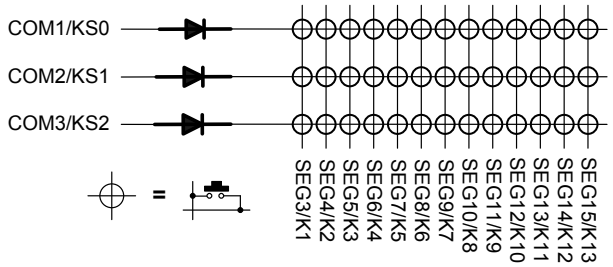
  (1) Since the level to K2 is not correctly sent, the key data cannot be latched correctly.

  (2) Since the short-circuited current (current I2) of KS1 (high level) to KS1 (low level) flows, the device may be damaged.

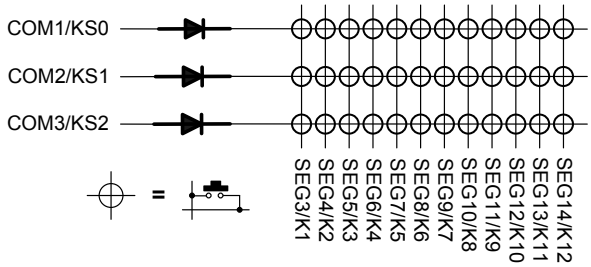


Key matrix combination with 28 pin package

- **Without INT pin**

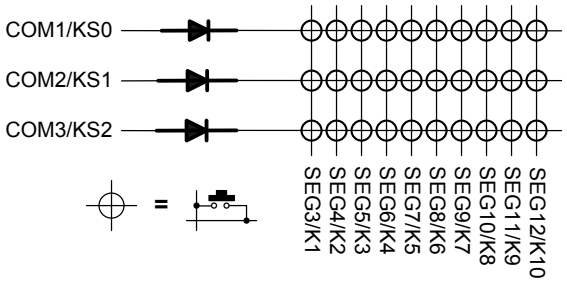


- **With INT pin**

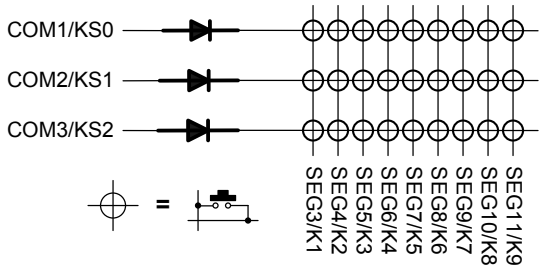


Key matrix combination with 24 pin package

- **Without INT pin**

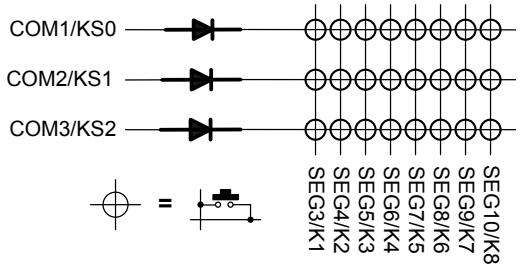


- **With INT pin**

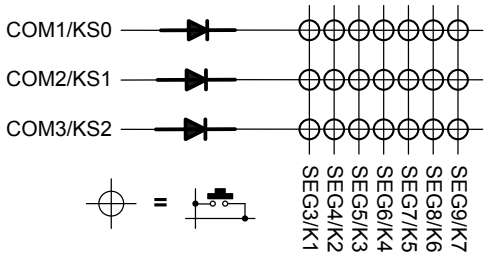


Key matrix combination with 20 pin package

- **Without INT pin**



- **With INT pin**

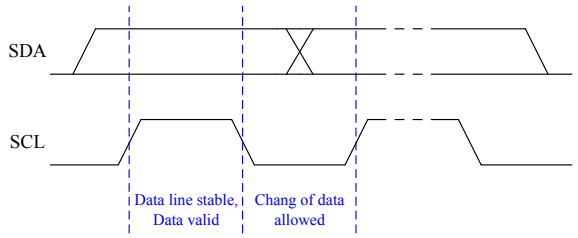


I²C Serial Interface

The HT16K33 includes an I²C serial interface. The I²C bus is used for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to a positive supply via a pull-up resistor. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to perform a wired and function. Data transfer is initiated only when the bus is not busy.

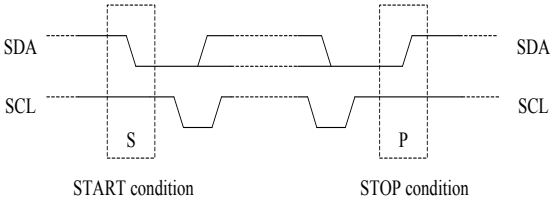
Data validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low (see below).



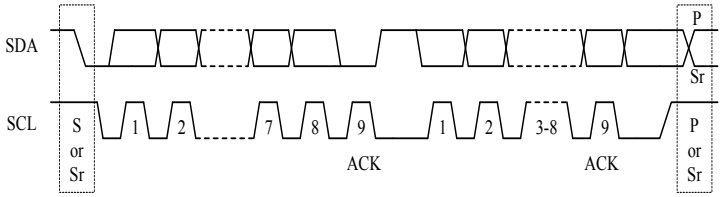
START and STOP conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START(S) and repeated START (Sr) conditions are functionally identical.



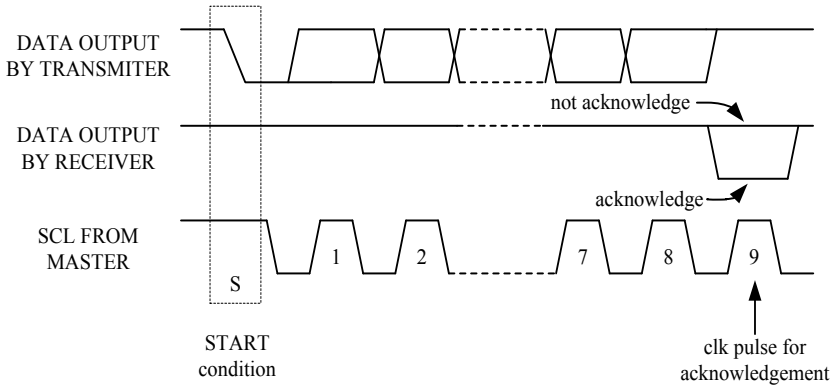
Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



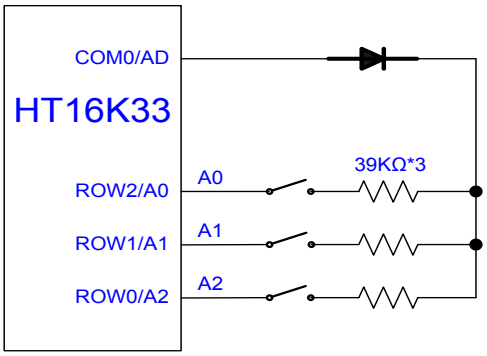
Acknowledge

- Each bytes includes eight bits is followed by a single acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, the master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge (ACK) after the reception of each byte.
- The device that acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Slave Addressing

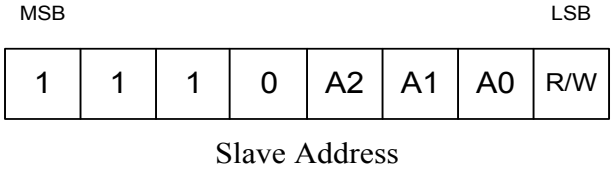
- The HT16K33 device requires an 8-bit slave address word following a start condition to enable the device for a write operation. The device address words consist of a mandatory one, zero sequence for the first four most significant bits (refer to the diagram showing the slave Address). This is common to all LED devices.
- The slave address input circuit is shown below. A2~A0 are set to "0", when A2~A0 are floating. A2~A0 are to "1", when A2~A0 are connected to an AD pin with a diode and resister.
- The slave address set is loaded into the HT16K33 at every frame.



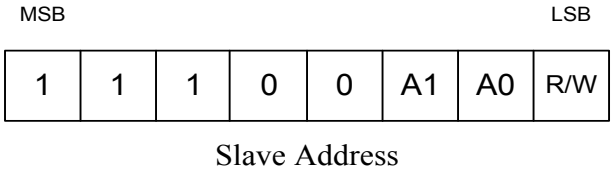
- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/$\overline{W}$ bit are "1", then a read operation is selected. A "0" selects a write operation.

- When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an acknowledge on the SDA line.

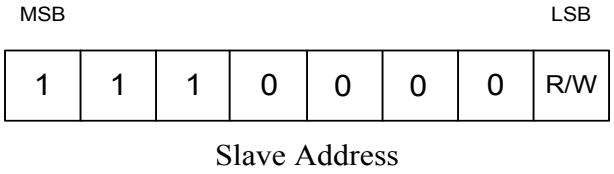
- **28-Pin package:**



- **24-Pin package:**



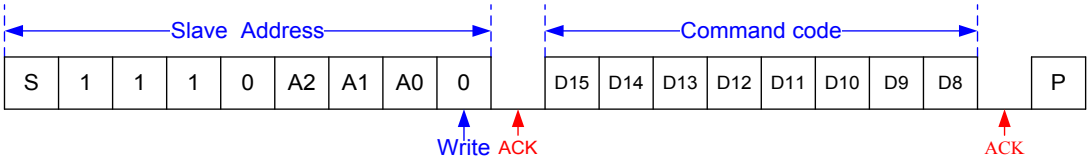
- **20-Pin package:**



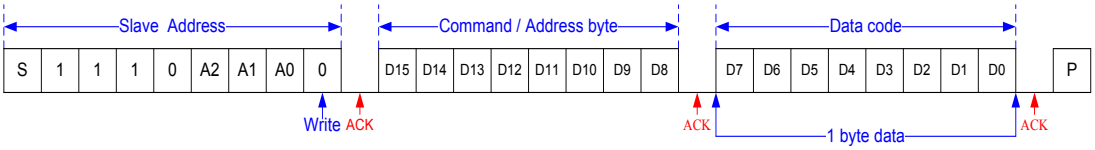
Write Operation

Byte write operation

A byte write operation requires a START condition, slave address with R/$\overline{W}$ bit, a valid Command code / Register address, a Data and a STOP condition.



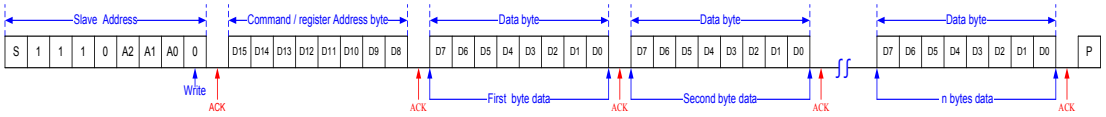
Command Byte Received



Command and Single Data Byte Received

Page write operation

Following a START condition and slave address with R/$\overline{W}$ bit is placed on the bus and indicates to the addressed device that Register Address will follow and is to be written to the address pointer. The data to be written to the memory in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. After reaching the display memory location 0X0FH the pointer will reset to 0X00H (display memory).

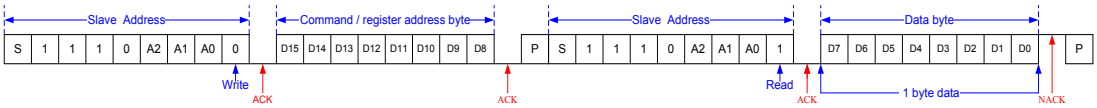


N Data Bytes Received

Read Operation

Byte read operation

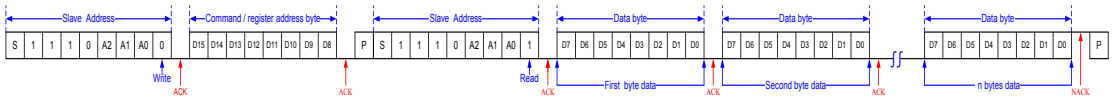
- A byte read operation requires a START condition, slave address with R/$\overline{W}$ bit, a fix valid Register address, slave address with R bit, a Data and a NACK signal and a STOP condition.
- The Byte reads command is not available for Key data reading.



Reading Single Data Bytes from the HT16K33

Page read operation

- In this mode, the master reads the HT16K33 data after setting the slave address. Following a R/$\overline{W}$ bit (="0") and acknowledge bit, the register address (An) is written to the address $\overline{W}$ pointer. Next the START condition and slave address are repeated followed by a R/$\overline{W}$ bit (="1"). The data which was addressed is then transmitted. The address pointer is only incremented on reception of an acknowledge clock. The HT16K33 will place the data at address An+1 on the bus. The master reads and acknowledges the new byte and the address pointer is incremented to "An+2".
- If the register address (An) is 0X00h ~ 0X0Fh, after reaching the memory location 0X0Fh, the pointer will be reset to 0X00h.
- The key data RAM of address 0x40H~0x45H should be read continuously and completed in one operation, so the key data RAM of address should be started from 0x40H only.
- This cycle of reading consecutive addresses will continue until the master sends a NACK signal and STOP condition.



Reading n Data Bytes from the HT16K33

Command Summary

Name	Command / Address								Option	Description	Def.
	D15	D14	D13	D12	D11	D10	D9	D8			
Display data Address pointer	0	0	0	0	A3	A2	A1	A0	{A0~A3} R/W	• Five bits of immediate data, bits A0 to A3, are transferred to the data pointer to define one of sixteen display RAM addresses. • If the Display data register address (An) is 0X00h ~ 0X0Fh, after reaching the memory location 0X0Fh, the pointer will reset to 0X00h	00H
System setup	0	0	1	0	X	X	X	S	{S} Write only	Defines internal system oscillator on/off • {0}:Turn off System oscillator (standby mode) • {1}:Turn on System oscillator (normal operation mode)	20H
Key data Address pointer	0	1	0	0	0	K2	K1	K0	{K0~K2} Read only	• Three bits of immediate data, bits K0 to K2, are transferred to the data pointer to define one of six key data RAM addresses. • It is strongly recommended that the key data RAM of address 0x40H~0x45H should be read continuously and in one operation, so the key data RAM of address should be started at 0x40H only. • If the Key data register address (An) is 0X40h ~ 0X45h, after reaching the memory location 0X45h, the pointer will reset to 0X40h	40H
INT flag Address pointer	0	1	1	0	0	0	0	0	Read only	Defines the INT flag address, Read INT flag status. Interrupt flag signal output. When any key matrix key is pressed, after the completion of two key scan cycles, this int flag bit goes to a high level and remains at a high level until all key data has been read,	60H
Display setup	1	0	0	0	X	B1	B0	D	{D} Write only	Defines Display on/off status. • {0}: Display off • {1}: Display on	80H
									{B1,B0} Write only	Defines the blinking frequency • {0,0} = Blinking OFF • {0,1} = 2HZ • {1,0} = 1HZ • {1,1} = 0.5HZ	

Note: If programmed command data is not defined, the function will not be affected.

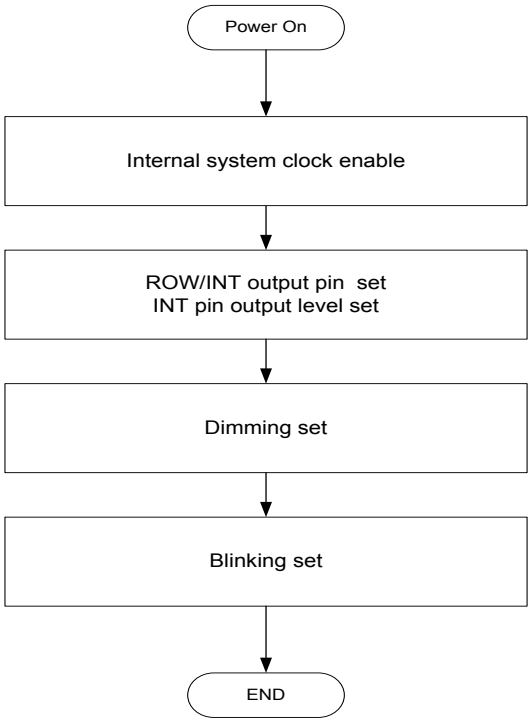
Name	Command / Address								Option	Description	Def.
	D15	D14	D13	D12	D11	D10	D9	D8			
ROW/INT set	1	0	1	0	X	X	act	row/ int	{act, row/ int } Write only	Defines INT/ROW output pin select and INT pin output active level status. ● {X 0}: INT/ROW output pin is set to ROW driver output. ● {0, 1}: INT/ROW output pin is set to INT output, active low. ● {1, 1}: INT/ROW output pin is set to INT output, active high.	A0H
Dimming set	1	1	1	0	P3	P2	P1	P0	{P3~P0} Write only	Defines the pulse width of ROW. ● {0,0,0,0}: 1/16duty ● {0,0,0,1}: 2/16duty ● {0,0,1,0}: 3/16duty ● {0,0,1,1}: 4/16duty ● {0,1,0,0}: 5/16duty ● {0,1,0,1}: 6/16duty ● {0,1,1,0}: 7/16duty ● {0,1,1,1}: 8/16duty ● {1,0,0,0}: 9/16duty ● {1,0,0,1}: 10/16duty ● {1,0,1,0}: 11/16duty ● {1,0,1,1}: 12/16duty ● {1,1,0,0}: 13/16duty ● {1,1,0,1}: 14/16duty ● {1,1,1,0}: 15/16duty ● {1,1,1,1}: 16/16duty	EFH
Test mode	1	1	0	1	1	0	0	1	Write only	HOLTEK use only	D9H

Note: If a programmed command data is not defined, the function will not be affected.

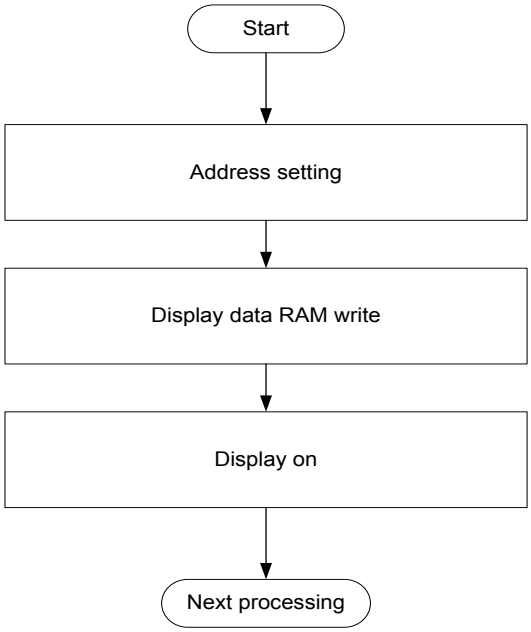
HT16K33 operation flow chart

Access procedures are illustrated below by means of flowcharts.

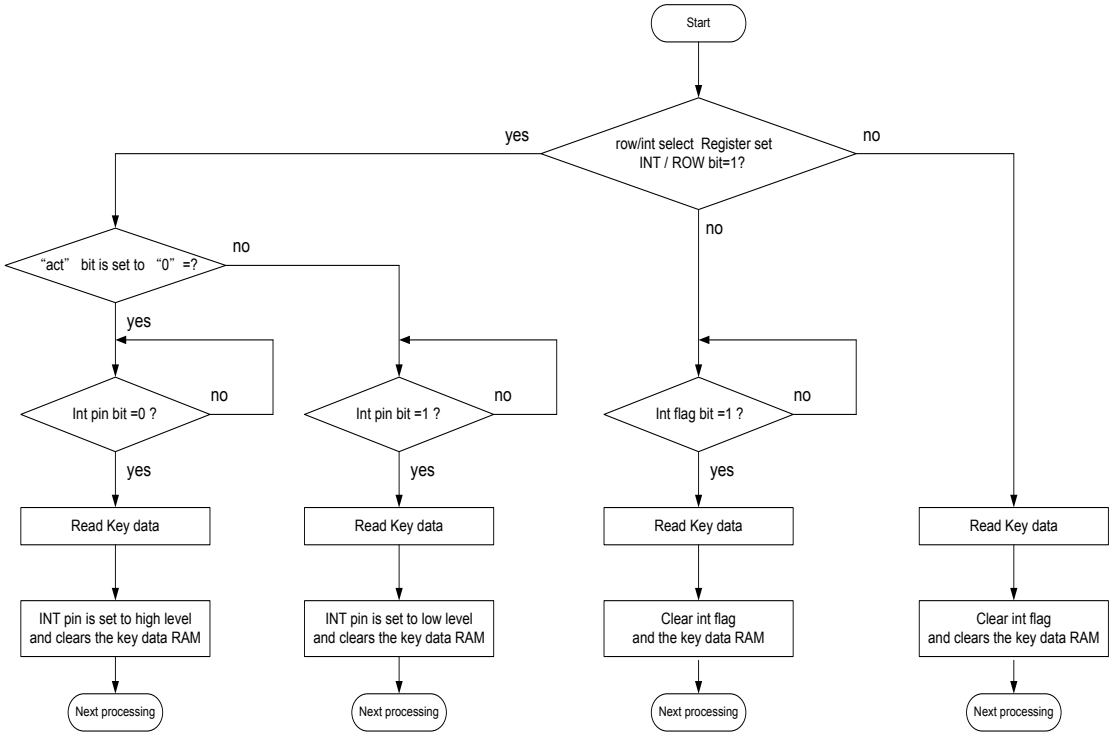
- **Initialisation**



- **Display data rewrite – address setting**

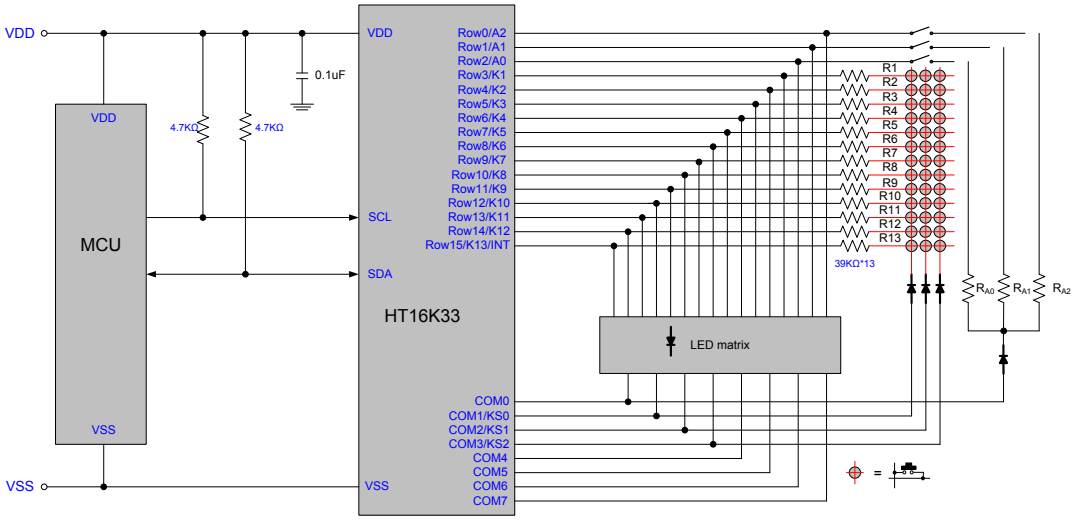


- **Key data read**



Application Circuit

- **16*8 display application: (No INT pin function and 13*3 key function)**

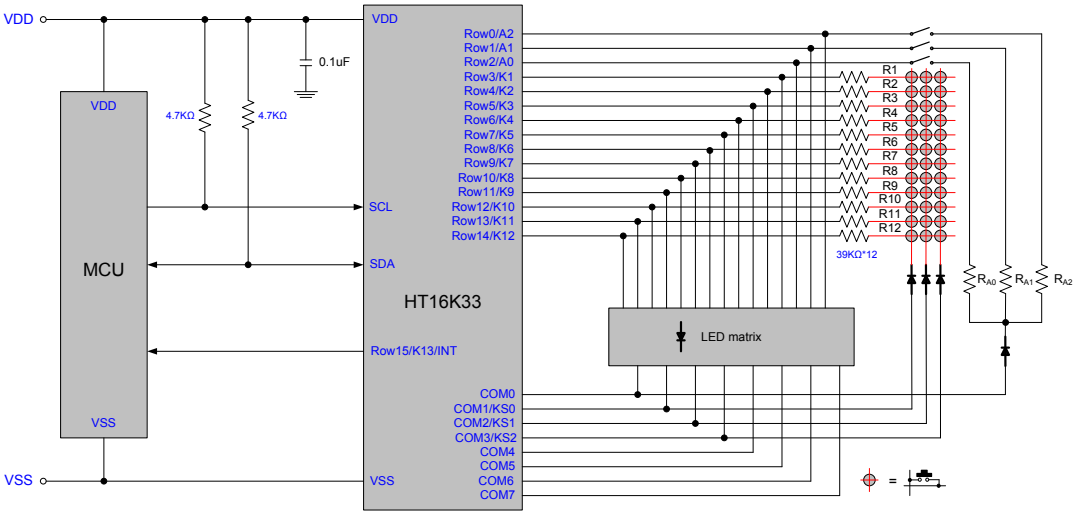


Note: 1. If R_{A0}, R_{A1} and R_{A2} are Open, the I^2C slave address (A0~A2) is set to low.

2. If R_{A0}, R_{A1} and R_{A2} are 39KΩ, the I^2C slave address (A0~A2) is set to high.

3. If the key input is not used for LED display, the resistor in series with the key input (R1~R13) can be omitted.

- **15*8 display application: (INT pin function and 12*3 key function)**

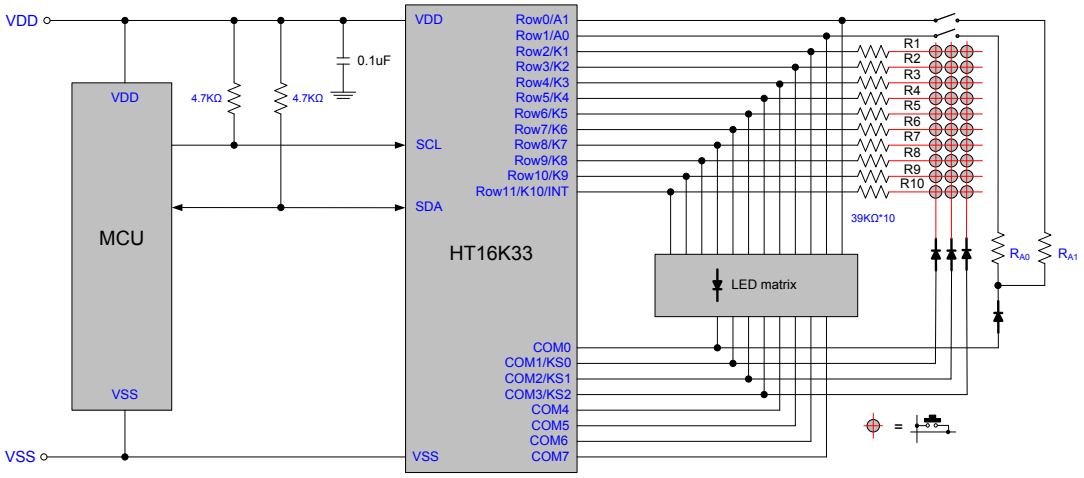


Note: 1. If R_{A0}, R_{A1} and R_{A2} are Open, the I^2C slave address (A0~A2) is set to low.

2. If R_{A0}, R_{A1} and R_{A2} are 39KΩ, the I^2C slave address (A0~A2) is set to high.

3. If the key input is not used for LED display, the resistor in series with the key input (R1~R12) can be omitted.

- **12*8 display application: (No INT pin function and 10*3 key function)**

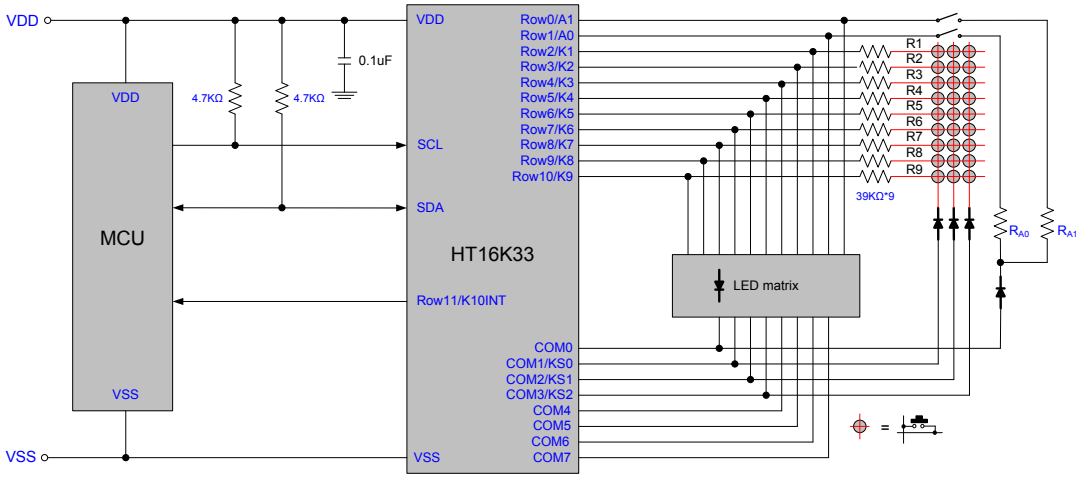


Note: 1. If R_{A0} and R_{A1} are Open, the I^2C slave address (A0~A1) is set to low and A2 is always set to low.

2. If R_{A0} and R_{A1} are 39KΩ, the I^2C slave address (A0~A1) is set to high and A2 is always set to low.

3. If the key input is not used for LED display, the resistor in series with the key input (R1~R10) can be omitted.

- **11*8 display application: (INT pin function and 9*3 key function)**

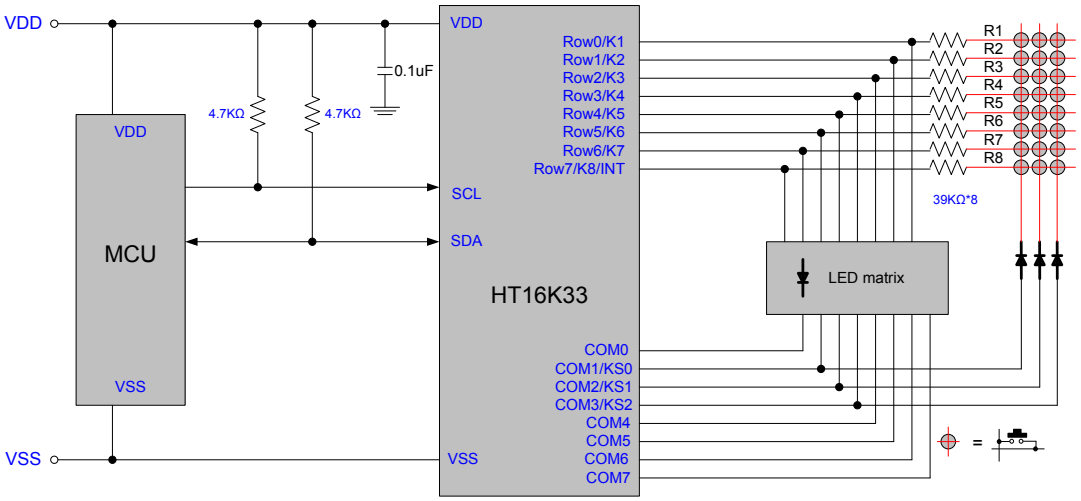


Note: 1. If R_{A0} and R_{A1} are Open, the I^2C slave address (A0~A1) is set to low and A2 is always set to low.

2. If R_{A0} and R_{A1} are 39KΩ, the I^2C slave address (A0~A1) is set to high and A2 is always set to low.

3. If the key input is not used for LED display, the resistor in series with the key input (R1~R9) can be omitted.

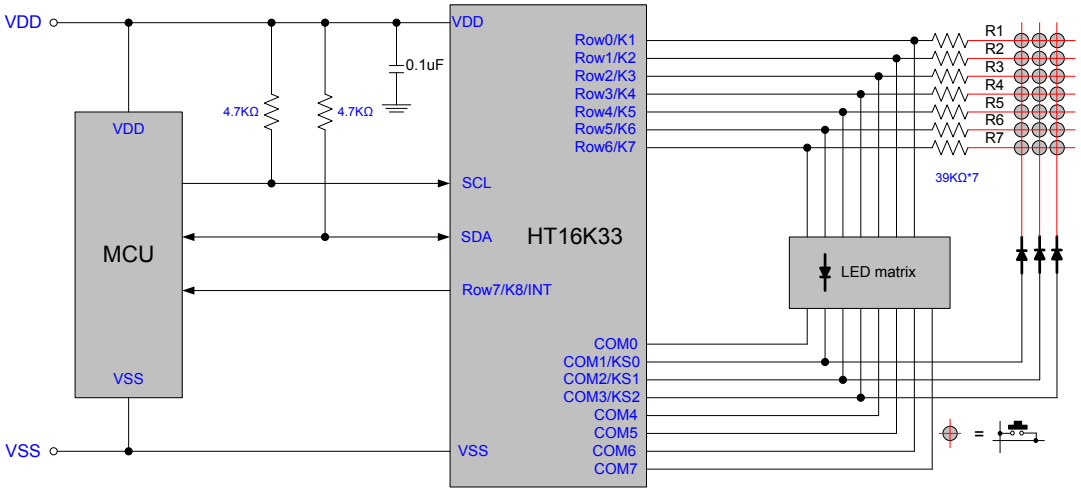
- **8*8 display application: (No INT pin function and 8*3 key function)**



Note: 1. The I^2C slave address (A0~A2) =000.

2. If the key input is not used for LED display, the resistor in series with the key input (R1~R8) can be omitted.

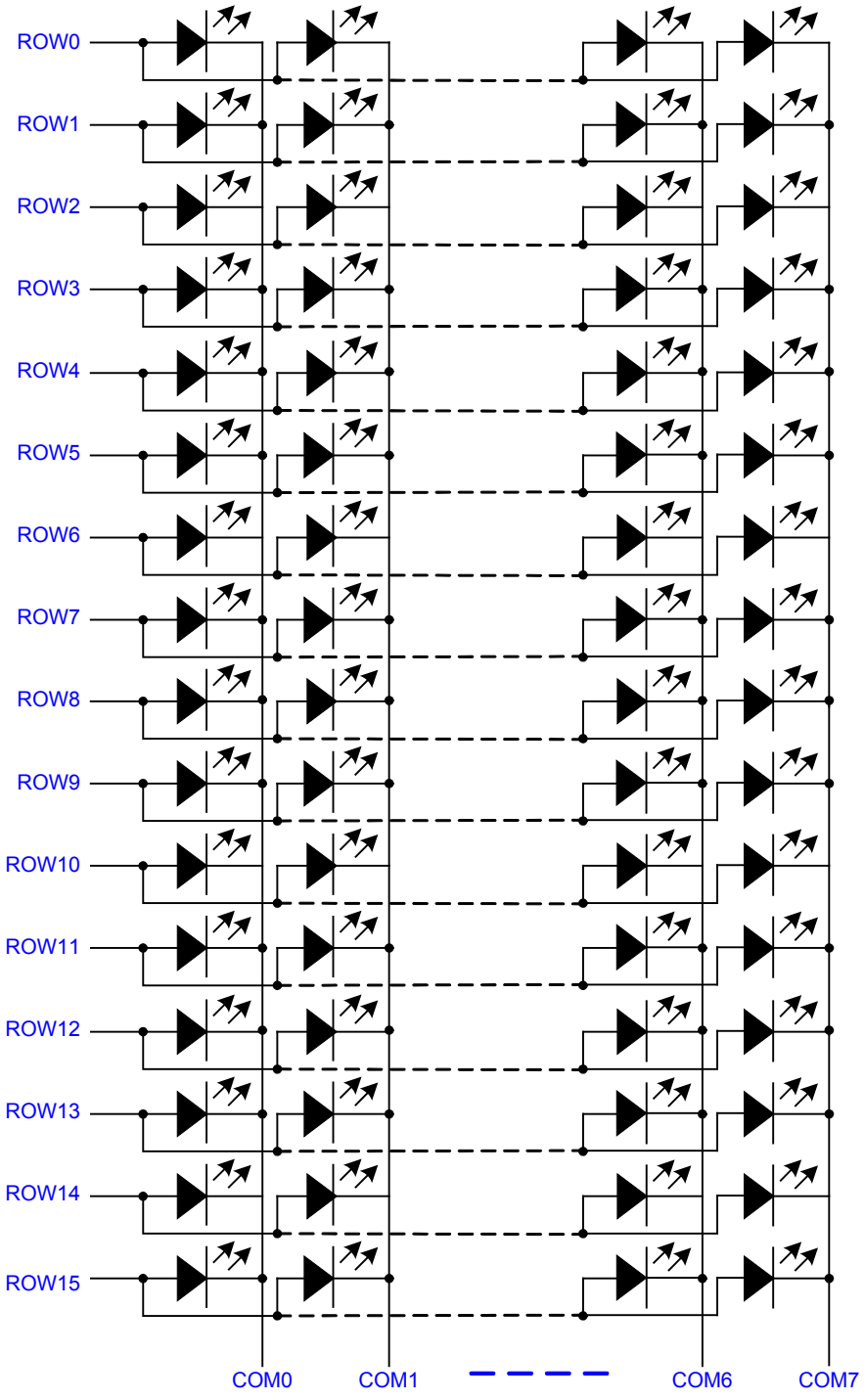
- **7*8 display application: (INT pin function and 7*3 key function)**



Note: 1. The I^2C slave address (A0~A2) =000.

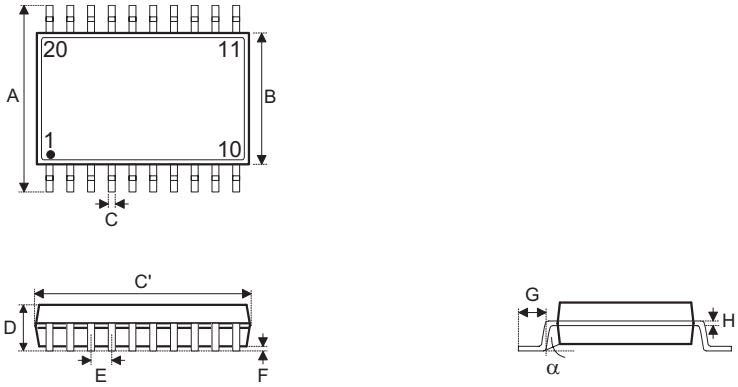
2. If the key input is not used for LED display, the resistor in series with the key input (R1~R7) can be omitted.

LED Matrix Circuit



Package Information

20-pin SOP (300mil) Outline Dimensions

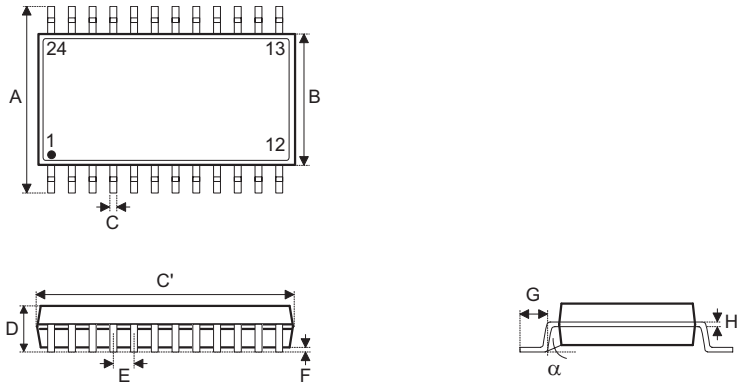


MS-013

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.393	—	0.419
B	0.256	—	0.300
C	0.012	—	0.020
C’	0.496	—	0.512
D	—	—	0.104
E	—	0.050	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.98	—	10.64
B	6.50	—	7.62
C	0.30	—	0.51
C’	12.60	—	13.00
D	—	—	2.64
E	—	1.27	—
F	0.10	—	0.30
G	0.41	—	1.27
H	0.20	—	0.33
α	0°	—	8°

24-pin SOP (300mil) Outline Dimensions

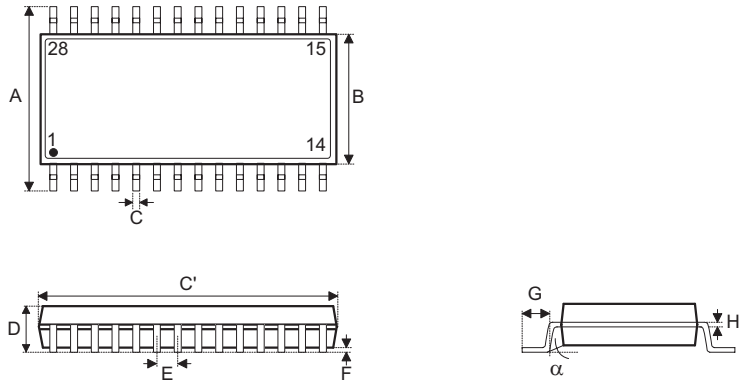


MS-013

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.393	—	0.419
B	0.256	—	0.300
C	0.012	—	0.020
C’	0.598	—	0.613
D	—	—	0.104
E	—	0.050	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.98	—	10.64
B	6.50	—	7.62
C	0.30	—	0.51
C’	15.19	—	15.57
D	—	—	2.64
E	—	1.27	—
F	0.10	—	0.30
G	0.41	—	1.27
H	0.20	—	0.33
α	0°	—	8°

28-pin SOP (300mil) Outline Dimensions

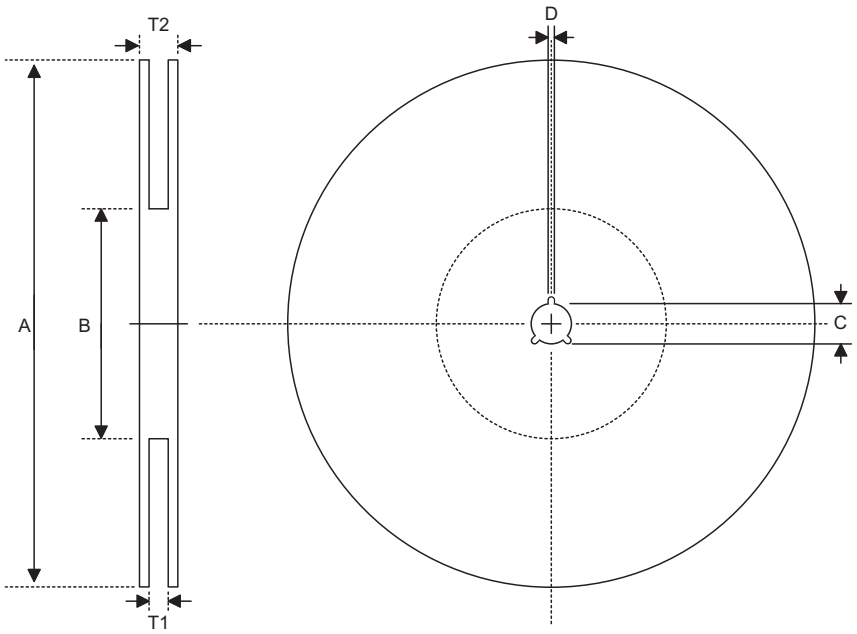


MS-013

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.393	—	0.419
B	0.256	—	0.300
C	0.012	—	0.020
C’	0.697	—	0.713
D	—	—	0.104
E	—	0.050	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.98	—	10.64
B	6.50	—	7.62
C	0.30	—	0.51
C’	17.70	—	18.11
D	—	—	2.64
E	—	1.27	—
F	0.10	—	0.30
G	0.41	—	1.27
H	0.20	—	0.33
α	0°	—	8°

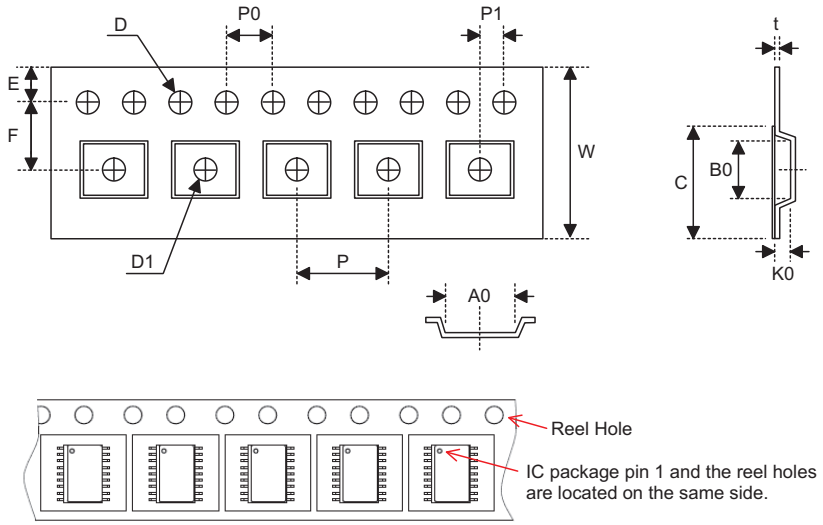
Reel Dimensions



SOP 20W, SOP 24W, SOP 28W (300mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	$13.0^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	$24.8^{+0.3/-0.2}$
T2	Reel Thickness	30.2±0.2

Carrier Tape Dimensions



SOP 20W

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$24.0^{+0.3/-0.1}$
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.8±0.1
B0	Cavity Width	13.3±0.1
K0	Cavity Depth	3.2±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	21.3±0.1

SOP 24W

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0+0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	$1.55^{+0.1/-0.00}$
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.9±0.1
B0	Cavity Width	15.9±0.1
K0	Cavity Depth	3.1±0.1
t	Carrier Tape Thickness	0.35±0.05
C	Cover Tape Width	21.3±0.1

SOP 28W (300mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.85±0.10
B0	Cavity Width	18.34±0.10
K0	Cavity Depth	2.97±0.10
t	Carrier Tape Thickness	0.35±0.01
C	Cover Tape Width	21.3±0.1