Features

MCU Features

- Operating voltage:
  f_{SYS}= 8MHz at 2.2V~5.5V
  f_{SYS}= 12MHz at 2.7V~5.5V
  f_{SYS}= 20MHz at 4.5V~5.5V
- Up to 0.2μs instruction cycle with 20MHz system clock at V_{DD}=5V
- Power down and wake-up functions to reduce power consumption
- Five oscillators
  - External High Speed Xtal
  - External 32.768kHz Xtal
  - External RC
  - Internal High Speed -- no ext. components
  - Internal 32kHz -- no ext. components
- Multi-mode operation: NORMAL, SLOW, IDLE and SLEEP
- Fully integrated internal 4MHz, 8MHz and 12MHz oscillator requires no external components
- All instructions executed in one or two instruction cycles
- Table read instructions
- 63 powerful instructions
- Up to 8 subroutine nesting levels
- Bit manipulation instruction

MCU Peripheral Features

- Flash Program Memory: 1K×14 ~ 12K×16
- RAM Data Memory: 64×8 ~ 576×8
- EEPROM Memory: 32×8 ~ 256×8
- Watchdog Timer function
- Up to 39 bidirectional I/O lines
- Software controlled 4-SCOM lines LCD driver with 1/2 bias
- Multiple pin-shared external interrupts
- Multiple Timer Module for time measure, input capture, compare match output, PWM output or single pulse output functions
- Serial Interface Module -- SIM for SPI or I^2C
- Dual Comparator functions
- Dual Time-Base functions for generation of fixed time interrupt signal
- Low voltage reset function
- Low voltage detect function

SPI to USB chip Features

- Fully compliant with USB 2.0 Full-Speed specification
- 6 endpoints (including endpoint 0)
- FIFO: 8, 8, 8, 64, 8, 64 for endpoint 0 ~ endpoint 5 respectively
- Suspend Mode and Remote Wake-up function
- Multiple USB interrupt generation sources: endpoint access, suspend, resume and reset signals
- CMOS clock input with frequency of 6MHz/12MHz for the USB PLL clock

General Description

The HT68FBx0 series of devices are Flash Memory I/O type 8-bit high performance RISC architecture microcontrollers with a USB interface. Offering users the convenience of Flash Memory multi-programming features, these devices also include a wide range of functions and features. Other memory includes an area of RAM Data Memory as well as an area of EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc.

Analog feature includes dual comparator functions. Multiple and extremely flexible Timer Modules provide timing, pulse generation and PWM generation functions. Communication with the outside world is catered for by including fully integrated SPI or I^2C interface functions, two popular interfaces which provide designers with a means of easy communication with external peripheral hardware. Protective features such as an internal Watchdog Timer, Low Voltage Reset and Low Voltage Detector coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments.

A full choice of HXT, LXT, ERC, HIRC and LIRC oscillator functions are provided including a fully integrated system oscillator which requires no external components for its implementation. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimise microcontroller operation and minimize power consumption.

The device contains a single USB Full-speed interface to allow data communication with an external USB host controller. It is particularly suitable for applications which require data communication between PCs and peripheral USB hardware.

An extensive choice of oscillator functions is provided including a fully integrated system oscillator which requires no external components for its implementation. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimise microcontroller operation and minimise power consumption. The devices also include flexible I/O programming features, Time-Base functions and a range of other features.

Selection Guide

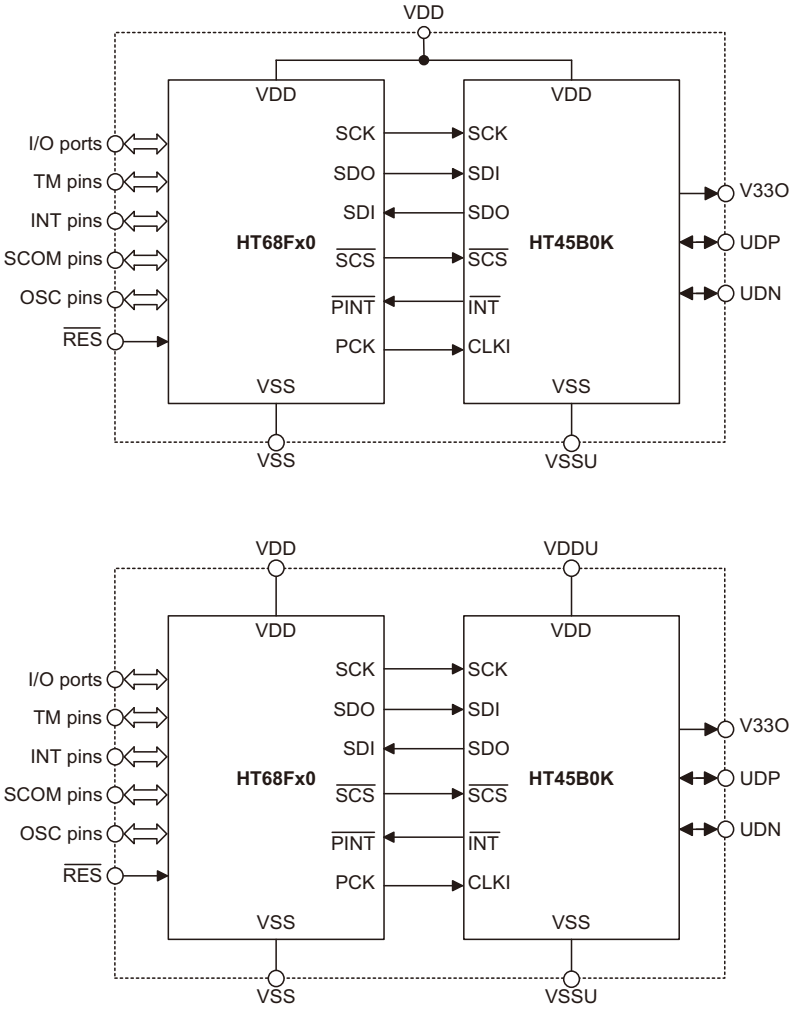
Most features are common to all devices, the main feature distinguishing them are Memory capacity, I/O counts, TM features, stack capacity and package types. The following table summarises the main features of each device.

Part No.	VDD	Program Memory	Data Memory	Data EEPROM	I/O	Ext. Int.	Timer Module	Interface (SPI/I^2C)	USB	Stack	Package
HT68FB30	2.2V~5.5V	2K×14	96×8	64×8	16	2	10-bit CTM×1 10-bit ETM×1	√	√	4	28SKDIP/SOP/SSOP
HT68FB40	2.2V~5.5V	4K×15	192×8	128×8	33	2	10-bit CTM×1 10-bit ETM×1 10-bit STM×1	√	√	8	44LQFP, 48QFN
HT68FB50	2.2V~5.5V	8K×16	384×8	256×8	34	2	10-bit CTM×2 10-bit ETM×1 10-bit STM×1	√	√	8	44LQFP, 48QFN
HT68FB60	2.2V~5.5V	12K×16	576×8	256×8	39	4	10-bit CTM×2 10-bit ETM×1 10-bit STM×1	√	√	8	40/48QFN, 44/48LQFP, 52QFP

Note: As devices exist in more than one package format, the table reflects the situation for the package with the most pins.

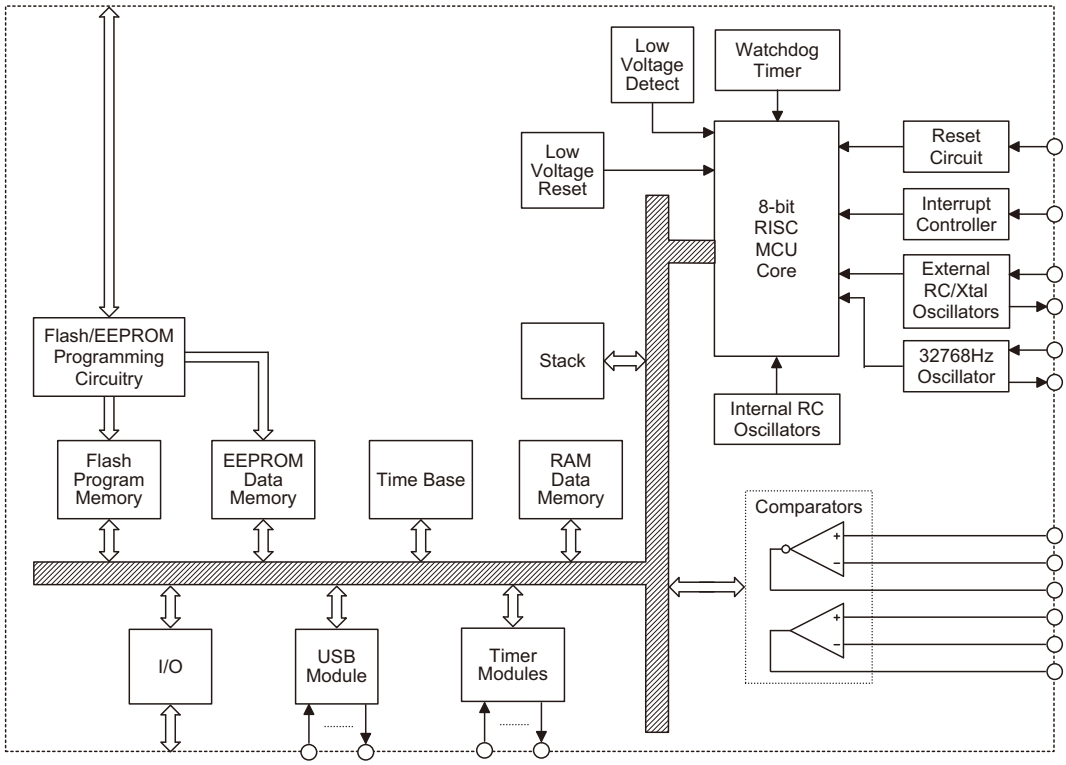
Block Diagram

The following block diagram illustrates the dual-chip structure of the devices, where an individual MCU and SPI to USB chips are combined into a single package.

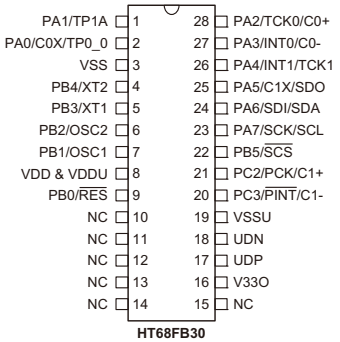


Internal Chip Interconnection Diagram

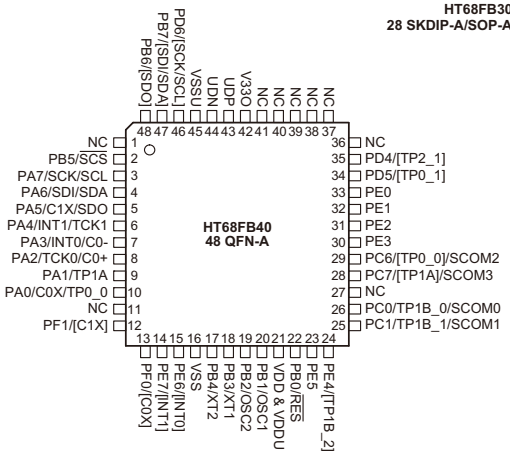
Note: The ground pins of the internal chips are NOT connected together. On some devices the positive power supply pins are connected together and on some they remain independent.

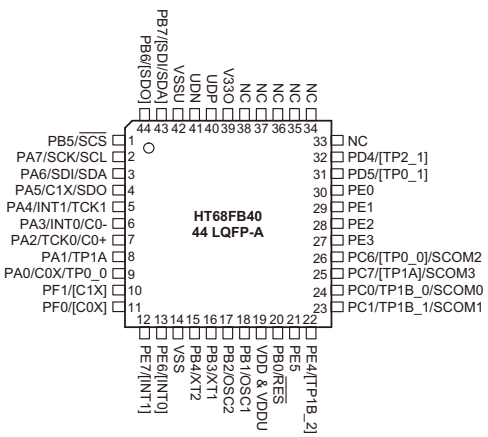


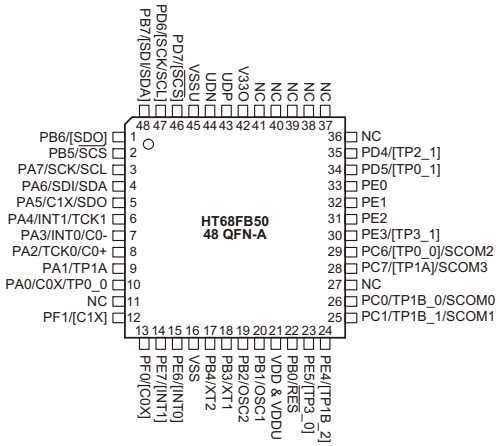
Pin Assignment

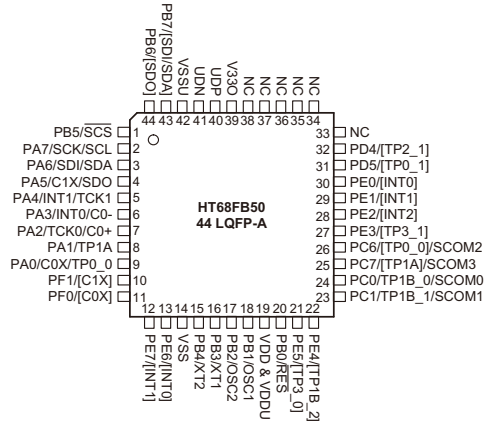


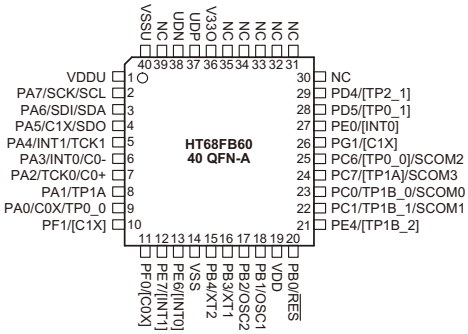
HT68FB30
28 SKDIP-A/SOP-A/SSOP-A

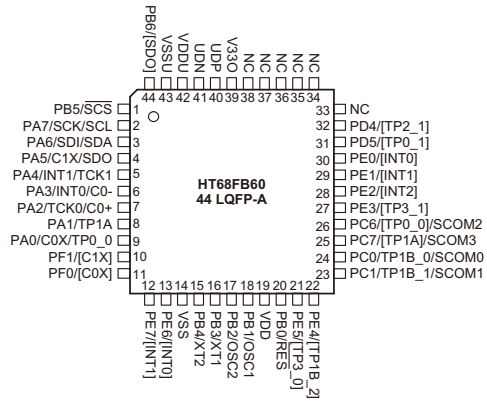


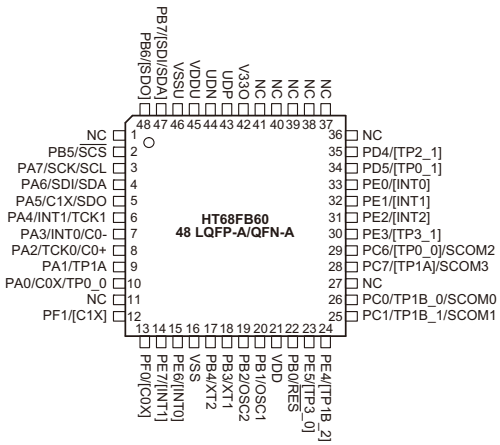


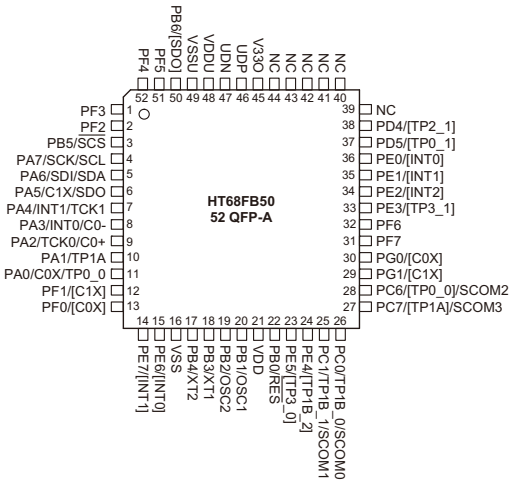












Note: 1. Bracketed pin names indicate non-default pinout remapping locations.

2. For pin-shared pin functions, pin names to the right side of the "/" sign have higher priority.

3. VDD & AVDD & VDDU means the VDD, AVDD and VDDU pins are bonded together.

Pin Description

With the exception of the power pins, all pins on these devices can be referenced by their Port name, e.g. PA.0, PA.1 etc, which refer to the digital I/O function of the pins. However these Port pins are also shared with other function such as the Analog to Digital Converter, Serial Port pins, etc. The function of each pin is listed in the following tables, however the details behind how each pin is configured is contained in individual MCU and SPI to USB chip datasheet. The important point to note here is that some I/O lines are not bonded to the external pins. Users should take special care of these I/O port lines. Refer to the Hardware Considerations section for more details.

HT68FB30

Pin Name	Function	OP	I/T	O/T	Pin-Shared Mapping
PA0~PA7	Port A	PAWU PAPU	ST	CMOS	—
PB0~PB5	Port B	PBPU	ST	CMOS	—
PC2~PC3	Port C	PCPU	ST	CMOS	—
C0-, C1-	Comparator 0, 1 input	CP0C CP1C	AN	—	PA3, PC3
C0+, C1+	Comparator 0, 1 input		AN	—	PA2, PC2
C0X, C1X	Comparator 0, 1 output		—	CMOS	PA0, PA5
TCK0, TCK1	TM0, TM1 input	—	ST	—	PA2, PA4
TP0_0	TM0 I/O	TMPC0	ST	CMOS	PA0
TP1A	TM1 I/O	TMPC0	ST	CMOS	PA1
INT0, INT1	External interrupt 0, 1	—	ST	—	PA3, PA4
$\overline{\text{PINT}}$	Peripheral Interrupt ***	PRM0	ST	—	PC3 or PC4
PCK	Peripheral Clock Output ***	PRM0	—	CMOS	PC2 or PC5
SDI	SPI data input ***	PRM0	ST	—	PA6 or PC0
SDO	SPI data output ***	PRM0	—	CMOS	PA5 or PC1
$\overline{\text{SCS}}$	SPI slave select ***	PRM0	ST	CMOS	PB5 or PC6
SCK	SPI serial clock ***	PRM0	ST	CMOS	PA7 or PC7
SCL	I^2C clock	PRM0	ST	NMOS	PA7
SDA	I^2C data	PRM0	ST	NMOS	PA6
OSC1	HXT/ERC pin	CO	HXT	—	PB1
OSC2	HXT pin	CO	—	HXT	PB2
XT1	LXT pin	CO	LXT	—	PB3
XT2	LXT pin	CO	—	LXT	PB4
$\overline{\text{RES}}$	Reset input	CO	ST	—	PB0
VDD	MCU power supply *	—	PWR	—	—
VSS	MCU ground	—	PWR	—	—
UDP	USB D+ pin	—	ST	CMOS	—
UDN	USB D- pin	—	ST	CMOS	—
V33O	3.3V regulator output pin	—	—	—	—
VDDU	USB power supply *	—	PWR	—	—
VSSU	USB ground	—	PWR	—	—
NC	Not connected, can not be used	—	—	—	—

Note: I/T: Input type; O/T: Output type

OP: Optional by configuration option (CO) or register option

PWR: Power; CO: Configuration option; ST: Schmitt Trigger input

CMOS: CMOS output; NMOS: NMOS output

AN: Analog input pin

HXT: High frequency crystal oscillator

LXT: Low frequency crystal oscillator

*: VDD is the device power supply while VDDU is the USB power supply respectively. The VDDU pin is bonded together internally with VDD.

**: When the $\overline{\text{PINT}}$, PCK and SPI functions are pin-shared remapping to PC4~PC5, PC0~PC1 and PC6~PC7 pins, the SPI pins are to be used as the master SPI signal to communicate with the slave SPI in HT45B0K along with the $\overline{\text{PINT}}$ and PCK pins used as the interrupt input and clock output connected to the SPI to USB chip to control the overall USB functions.

HT68FB40

Pin Name	Function	OP	I/T	O/T	Pin-Shared Mapping
PA0~PA7	Port A	PAWU PAPU	ST	CMOS	—
PB0~PB7	Port B	PBPU	ST	CMOS	—
PC0~PC1, PC6~PC7	Port C	PCPU	ST	CMOS	—
PD4~PD6	Port D	PDPU	ST	CMOS	—
PE0~PE7	Port E	PEPU	ST	CMOS	—
PF0~PF1	Port F	PFPU	ST	CMOS	—
C0-	Comparator 0 input	CP0C	AN	—	PA3
C0+	Comparator 0 input		AN	—	PA2
C0X, C1X	Comparator 0, 1 output	CP0C CP1C PRM0	—	CMOS	PA0, PA5 or PF0, —
TCK0, TCK1	TM0, TM1 input	PRM1	ST	—	PA2, PA4, —
TP0_0, TP0_1	TM0 I/O	TMPC0 PRM2	ST	CMOS	PA0, —, or PC6, PD5
TP1A	TM1 I/O	TMPC0 PRM2	ST	CMOS	PA1 or PC7
TP1B_0~ TP1B_2	TM1 I/O	TMPC0 PRM2	ST	CMOS	PC0, PC1, — or —, —, PE4
TP2_1	TM2 I/O	TMPC1 PRM2	ST	CMOS	— or PD4
INT0, INT1	External interrupt 0, 1	PRM1	ST	—	PA3, PA4 or PE6, PE7
$\overline{\text{PINT}}$	Peripheral Interrupt ***	PRM0	ST	—	— or PC4
PCK	Peripheral Clock Output ***	PRM0	—	CMOS	— or PC5
SDI	SPI data input ***	PRM0	ST	—	PA6 or PD2 or PB7
SDO	SPI data output ***	PRM0	—	CMOS	PA5 or PD3 or PB6
$\overline{\text{SCS}}$	SPI slave select ***	PRM0	ST	CMOS	PB5 or PD0 or PD7
SCK	SPI serial clock ***	PRM0	ST	CMOS	PA7 or PD1 or PD6
SCL	I^2C clock	PRM0	ST	NMOS	PA7 or PD1 or PD6

Pin Name	Function	OP	I/T	O/T	Pin-Shared Mapping
SDA	I^2C data	PRM0	ST	NMOS	PA6 or PD2 or PB7
SCOM0~ SCOM3	SCOM0~SCOM3	SCOMC	—	SCOM	PC0, PC1, PC6, PC7
OSC1	HXT/ERC pin	CO	HXT	—	PB1
OSC2	HXT pin	CO	—	HXT	PB2
XT1	LXT pin	CO	LXT	—	PB3
XT2	LXT pin	CO	—	LXT	PB4
$\overline{RES}$	Reset input	CO	ST	—	PB0
VDD	MCU power supply *	—	PWR	—	—
VSS	MCU ground **	—	PWR	—	—
UDP	USB D+ pin	—	ST	CMOS	—
UDN	USB D- pin	—	ST	CMOS	—
V33O	3.3V regulator output pin	—	—	—	—
VDDU	USB power supply	—	PWR	—	—
VSSU	USB ground	—	PWR	—	—
NC	Not connected, can not be used	—	—	—	—

Note: I/T: Input type; O/T: Output type

OP: Optional by configuration option (CO) or register option

PWR: Power; CO: Configuration option; ST: Schmitt Trigger input

CMOS: CMOS output; NMOS: NMOS output

SCOM: Software controlled LCD COM; AN: Analog input pin

HXT: High frequency crystal oscillator

LXT: Low frequency crystal oscillator

*: VDD is the device power supply while VDDU is the USB power supply respectively. The VDDU pin is bonded together internally with VDD.

**: When the $\overline{PINT}$, PCK and SPI functions are pin-shared remapping to PC4~PC5 and PD0~PD3 pins, the SPI pins are to be used as the master SPI signal to communicate with the slave SPI in HT45B0K along with the $\overline{PINT}$ and PCK pins used as the interrupt input and clock output connected to the SPI to USB chip to control the overall USB functions.

HT68FB50

Pin Name	Function	OP	I/T	O/T	Pin-Shared Mapping
PA0~PA7	Port A	PAWU PAPU	ST	CMOS	—
PB0~PB7	Port B	PBPU	ST	CMOS	—
PC0~PC1, PC6~PC7	Port C	PCPU	ST	CMOS	—
PD4~PD7	Port D	PDPU	ST	CMOS	—
PE0~PE7	Port E	PEPU	ST	CMOS	—
PF0~PF1	Port F	PFPU	ST	CMOS	—
C0-	Comparator 0 input	CP0C	AN	—	PA3
C0+	Comparator 0 input		AN	—	PA2
C0X, C1X	Comparator 0, 1 output	CP0C CP1C PRM0	—	CMOS	PA0, PA5 or PF0, PF1
TCK0, TCK1	TM0, TM1 input	PRM1	ST	—	PA2, PA4, —, —
TP0_0, TP0_1	TM0 I/O	TMPC0 PRM2	ST	CMOS	PA0, —, or PC6, PD5
TP1A	TM1 I/O	TMPC0 PRM2	ST	CMOS	PA1 or PC7
TP1B_0~ TP1B_2	TM1 I/O	TMPC0 PRM2	ST	CMOS	PC0, PC1, — or —, —, PE4
TP2_1	TM2 I/O	TMPC1 PRM2	ST	CMOS	— or PD4
TP3_0, TP3_1	TM3 I/O	TMPC1 PRM2	ST	CMOS	—, —, or PE5, PE3
INT0, INT1	External interrupt 0, 1	PRM1	ST	—	PA3, PA4 or PE6, PE7
$\overline{\text{PINT}}$	Peripheral Interrupt ***	PRM0	ST	—	— or PC4
PCK	Peripheral Clock Output ***	PRM0	—	CMOS	— or PC5
SDI	SPI data input ***	PRM0	ST	—	PA6 or PD2 or PB7
SDO	SPI data output ***	PRM0	—	CMOS	PA5 or PD3 or PB6
$\overline{\text{SCS}}$	SPI slave select ***	PRM0	ST	CMOS	PB5 or PD0 or PD7
SCK	SPI serial clock ***	PRM0	ST	CMOS	PA7 or PD1 or PD6
SCL	I^2C clock	PRM0	ST	NMOS	PA7 or PD1 or PD6
SDA	I^2C data	PRM0	ST	NMOS	PA6 or PD2 or PB7
SCOM0~ SCOM3	SCOM0~SCOM3	SCOMC	—	SCOM	PC0, PC1, PC6, PC7
OSC1	HXT/ERC pin	CO	HXT	—	PB1
OSC2	HXT pin	CO	—	HXT	PB2
XT1	LXT pin	CO	LXT	—	PB3
XT2	LXT pin	CO	—	LXT	PB4
$\overline{\text{RES}}$	Reset input	CO	ST	—	PB0
VDD	MCU power supply *	—	PWR	—	—

Pin Name	Function	OP	I/T	O/T	Pin-Shared Mapping
VSS	MCU ground **	—	PWR	—	—
UDP	USB D+ pin	—	ST	CMOS	—
UDN	USB D- pin	—	ST	CMOS	—
V33O	3.3V regulator output pin	—	—	—	—
VDDU	USB power supply	—	PWR	—	—
VSSU	USB ground	—	PWR	—	—
NC	Not connected, can not be used	—	—	—	—

Note: I/T: Input type; O/T: Output type

OP: Optional by configuration option (CO) or register option

PWR: Power; CO: Configuration option; ST: Schmitt Trigger input

CMOS: CMOS output; NMOS: NMOS output

SCOM: Software controlled LCD COM; AN: Analog input pin

HXT: High frequency crystal oscillator

LXT: Low frequency crystal oscillator

*: VDD is the device power supply while VDDU is the USB power supply respectively. The VDDU pin is bonded together internally with VDD.

**: When the $\overline{\text{PINT}}$, PCK and SPI functions are pin-shared remapping to PC4~PC5 and PD0~PD3 pins, the SPI pins are to be used as the master SPI signal to communicate with the slave SPI in HT45B0K along with the $\overline{\text{PINT}}$ and PCK pins used as the interrupt input and clock output connected to the SPI to USB chip to control the overall USB functions.

HT68FB60

Pin Name	Function	OP	I/T	O/T	Pin-Shared Mapping
PA0~PA7	Port A	PAWU PAPU	ST	CMOS	—
PB0~PB6	Port B	PBPU	ST	CMOS	—
PC0~PC1, PC6~PC7	Port C	PCPU	ST	CMOS	—
PD4~PD5	Port D	PDPU	ST	CMOS	—
PE0~PE7	Port E	PEPU	ST	CMOS	—
PF0~PF7	Port F	PFPU	ST	CMOS	—
PG0~PG1	Port G	PFPU	ST	CMOS	—
C0-	Comparator 0 input	CP0C	AN	—	PA3
C0+	Comparator 0 input		AN	—	PA2
C0X, C1X	Comparator 0, 1 output	CP0C CP1C PRM0	—	CMOS	PA0, PA5 or PF0, PF1 or PG0, PG1
TCK0, TCK1	TM0, TM1 input	PRM1	ST	—	PA2, PA4, —, —
TP0_0, TP0_1	TM0 I/O	TMPC0 PRM2	ST	CMOS	PA0, —, or PC6, PD5
TP1A	TM1 I/O	TMPC0 PRM2	ST	CMOS	PA1 or PC7
TP1B_0~ TP1B_2	TM1 I/O	TMPC0 PRM2	ST	CMOS	PC0, PC1, — or —, —, PE4

Pin Name	Function	OP	I/T	O/T	Pin-Shared Mapping
TP2_1	TM2 I/O	TMPC1 PRM2	ST	CMOS	— or PD4
TP3_0, TP3_1	TM3 I/O	TMPC1 PRM2	ST	CMOS	—, —, or PE5, PE3
INT0~INT2	External interrupt 0~2	PRM1	ST	—	PA3, PA4, — or —, —, PE2, PE0, PE1, —, or PE6, PE7, —
$\overline{\text{PINT}}$	Peripheral Interrupt *	PRM0	ST	—	— or PC4
PCK	Peripheral Clock Output *	PRM0	—	CMOS	— or PC5
SDI	SPI data input *	PRM0	ST	—	PA6 or PD2
SDO	SPI data output *	PRM0	—	CMOS	PA5 or PB6 or PD1
$\overline{\text{SCS}}$	SPI slave select *	PRM0	ST	CMOS	PB5 or PD0
SCK	SPI serial clock *	PRM0	ST	CMOS	PA7 or PD3
SCL	I^2C clock	PRM0	ST	NMOS	PA7
SDA	I^2C data	PRM0	ST	NMOS	PA6
SCOM0~ SCOM3	SCOM0~SCOM3	SCOMC	—	SCOM	PC0, PC1, PC6, PC7
OSC1	HXT/ERC pin	CO	HXT	—	PB1
OSC2	HXT pin	CO	—	HXT	PB2
XT1	LXT pin	CO	LXT	—	PB3
XT2	LXT pin	CO	—	LXT	PB4
$\overline{\text{RES}}$	Reset input	CO	ST	—	PB0
VDD	MCU power supply	—	PWR	—	—
VSS	MCU ground	—	PWR	—	—
UDP	USB D+ pin	—	ST	CMOS	—
UDN	USB D- pin	—	ST	CMOS	—
V33O	3.3V regulator output pin	—	—	—	—
VDDU	USB power supply	—	PWR	—	—
VSSU	USB ground	—	PWR	—	—
NC	Not connected, can not be used	—	—	—	—

Note: I/T: Input type; O/T: Output type

OP: Optional by configuration option (CO) or register option

PWR: Power; CO: Configuration option; ST: Schmitt Trigger input

CMOS: CMOS output; NMOS: NMOS output

SCOM: Software controlled LCD COM; AN: Analog input pin

HXT: High frequency crystal oscillator

LXT: Low frequency crystal oscillator

*: When the $\overline{\text{PINT}}$, PCK and SPI functions are pin-shared remapping to PC4~PC5 and PD0~PD3 pins, the SPI pins are to be used as the master SPI signal to communicate with the slave SPI in HT45B0K along with the $\overline{\text{PINT}}$ and PCK pins used as the interrupt input and clock output connected to the SPI to USB chip to control the overall USB functions.

Internally Connected Pins

Among the pins mentioned in the tables above several pins are not connected to external package pins. These pins are interconnection pins between the MCU and the SPI to USB chips and are listed in the following table. The description is provided from the SPI to USB chip standpoint.

SPI to USB Chip Pin Name	Type	Description
SDI	I	Slave SPI Serial Data In Input Signal Internally connected to the MCU Master SPI SDO output signal
SDO	O	Slave SPI Serial Data Out Output Signal Internally connected to the MCU Master SPI SDI input signal
SCK	I	Slave SPI Serial Clock Input Signal Internally connected to the MCU Master SPI SCK output signal
$\overline{SCS}$	I	Slave SPI Device Select Input Signal Internally connected to the MCU Master SPI $\overline{SCS}$ output signal - connected to pull high resistor
CLKI	I	Clock Input Signal Internally connected to the MCU Master PCK output signal
$\overline{INT}$	O	USB Interrupt Output Signal Internally connected to the MCU Master $\overline{PINT}$ input signal A USB related interrupt will generate a low pulse signal on this line

Functional Description

As these devices packages contain multiple internal chips, for a detailed functional description, users must refer to the relevant individual datasheets for both the MCU and the SPI to USB chips. The following table shows which individual devices are inside each package.

Device	MCU	SPI to USB Chip
HT68FB30	HT68F30	HT45B0K
HT68FB40	HT68F40	HT45B0K
HT68FB50	HT68F50	HT45B0K
HT68FB60	HT68F60	HT45B0K

Multi-chip Internal Devices

Although most of the functional description material will be located in the individual datasheets, there are some special considerations which need to be taken into account when using multi-chip devices. These points will be mentioned in the hardware and software consideration sections

As the complexity of USB data protocol does not permit comprehensive USB operation information to be provided in the related datasheets, the reader should therefore consult other external information for a detailed USB understanding.

Multi-chip Hardware Considerations

As these single-package multi-chip devices are composed of an individual MCU and SPI to USB chip, using them together requires the user to take care of some special points.

- Absolute Maximum Ratings
  The Absolute Maximum Ratings for the two individual chips must be checked for discrepancies and the necessary care taken in device handling and usage.

- Power Supply
  Examination of the block diagram will reveal that the SPI to USB chip Ground pin, VSSU, has no internal connection to the MCU Ground pin, VSS. For this reason these two pins must be connected externally. With the exception of the HT68FB60 device, the SPI to USB chip power supply pin, VDDU, is internally connected to the MCU power supply pin, VDD. For the HT68FB60 device, the SPI to USB chip power supply pin and the MCU power supply pin should be connected together externally.
  To calculate the power consumption for the devices, the total operating current is the sum of the operating current for the MCU specified in the MCU datasheet and the operating current for the SPI to USB chip listed in its datasheet. Similarly, the standby current is the sum of the two individual chip standby currents.

- Power Down and Wake up
  The MCU and SPI to USB chip are powered down independently of each other. The method of powering down the MCU is covered in the relevant MCU datasheet. The SPI to USB chip must be powered down before the MCU is powered down.
  After the device is powered down, it could be also woken up by the SPI to USB chip interrupt except by wake-up sources mentioned in the MCU datasheet. When a USB interrupt occurs on the $\overline{\text{INT}}$ line, it will wake up the MCU if the MCU has entered a power down mode. After the MCU is woken up, the application program must set the corresponding control bits to make the device function normally.

- Interrupts
  When a USB interrupt occurs, a low pulse will be generated on the $\overline{\text{INT}}$ line and sent to the peripheral interrupt line $\overline{\text{PINT}}$ in the MCU to get the attention of the microcontroller. When the USB interrupt caused by one of the USB interrupt generation sources occurs, if the corresponding interrupt control in the host MCU is enabled and the stack is not full, the program will jump to the corresponding interrupt vector where it can be serviced before returning to the main program.
  For a USB interrupt to be serviced, in addition to the bits for the corresponding interrupt enable control in the SPI to USB chip being set, the global interrupt enable control and the related interrupt enable control bits in the host MCU must also be set. If these bits are not set, then the interrupt signal will only be a wake-up source and no interrupt will be serviced.

- Unbonded MCU pins
  Examination of the relevant MCU datasheet will reveal that not all of the MCU I/O port lines are bonded out to external pins. As a result special attention regarding initialisation procedures should be paid to these port lines. If the pins are pin-shared with the analog input pins, they will be setup as analog inputs and the corresponding analog circuits will be disabled after a reset. When these pins are set as analog input pins and the relevant analog circuits are disabled, they will not consume any power even if the input pin conditions are not kept as either high or low logic levels. However, if the pins are not pin-shared with analog input pins, they will be setup as input states without pull high resistors after a reset. Users should therefore ensure that these pins are setup in input states with pull high resistors or in output states with either a high or low levels to avoid additional power consumption resulting from floating input pins.

Multi-chip Programming Considerations

To use the USB function, several important steps must be implemented to ensure that the SPI to USB chip operates normally:

- The SPI pin-remapping function must be properly configured when the SPI functional pins of the microcontroller are used to control the SPI to USB chip and for transmission and reception.
  To ensure proper setup between the MCU Master SPI interface to the SPI to USB chip Slave SPI, the SIM pin-remapping settings for PCK and $\overline{\text{PINT}}$ in the MCU PRM0 register should be setup as shown in the following table.
  - HT68FB30 PRM0 Register – PCK and $\overline{\text{PINT}}$ pin-remap setup

Bit	1	0
Name	SIMPS0	PCKPS
Setting Value	1	1

  - HT68FB40/HT68FB50 PRM0 Register – PCK and $\overline{\text{PINT}}$ pin-remap setup

Bit	2	1	0
Name	SIMPS1	SIMPS0	PCKPS
Setting Value	0	1	1

  - HT68FB60 PRM0 Register – PCK and $\overline{\text{PINT}}$ pin-remap setup

Bit	2	1	0
Name	SIMPS1	SIMPS0	PCKPS
Setting Value	1	1	1

- The SIM operating mode control bits SIM2~SIM0 in the SIMC0 register have to be configured to enable the SIM to operate in the SPI master mode with a different SPI clock frequency.
  - SIM operating mode control bits SIM2~SIM0 in the SIMC0 Register

Bit	2	1	0
Name	SIMPS1	SIMPS0	PCKPS
Setting Value	1	1	1

  000: SPI master mode; SPI clock is $f_{SYS}/4$
  001: SPI master mode; SPI clock is $f_{SYS}/16$
  010: SPI master mode; SPI clock is $f_{SYS}/64$
  011: SPI master mode; SPI clock is f_{TBC}
  100: SPI master mode; SPI clock is TM0 CCRP match frequency/2
  101~111: must not be used

- The PCK control bit is set to 1 to enable the PCK output as the clock source for the USB external clock input with various PCK output frequencies determined by the PCKP1 and PCKP0 bits in the SIMC0 Register.
  - PCK output frequency selection bits PCKP1~PCKP0 in the SIMC0 Register

Bit	1	0
Name	PCKP1	PCKP0
Setting Value	11, 10, 01 or 00	

  00: PCK output frequency is f_{SYS}
  01: PCK output frequency is $f_{SYS}/4$
  10: PCK output frequency is $f_{SYS}/8$
  11: PCK output frequency is TM0 CCRP match frequency/2

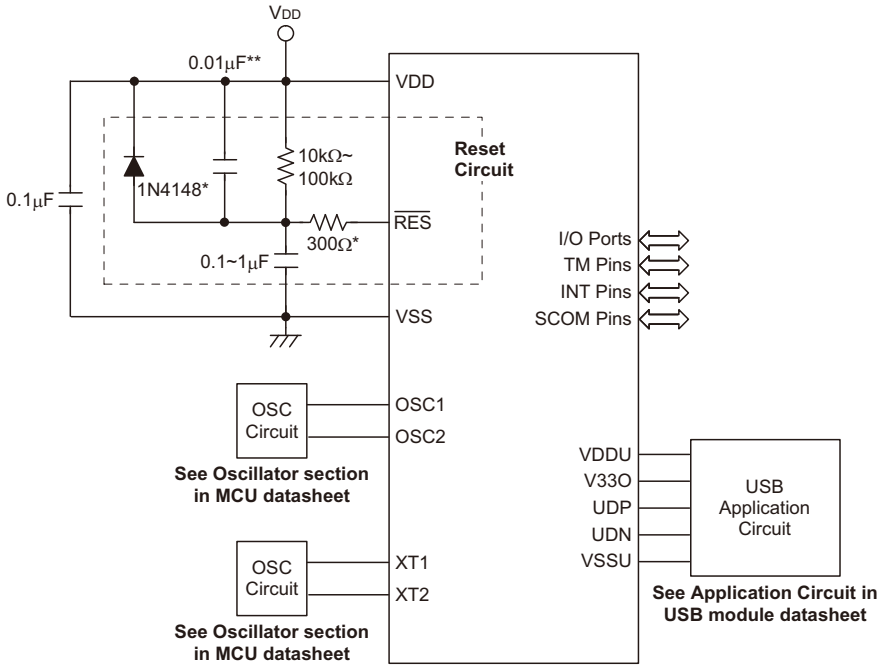
  - PCK output enable control bit PCKEN in the SIMC0 Register

Bit	4
Name	PCKEN
Setting Value	1

  0: Disable PCK output
  1: Enable PCK output

After the above setup conditions have been implemented, the MCU can enable the SIM interface by setting the SIMEN bit high. The MCU can then begin communication with external USB connected appliances using its SPI interface. The detailed functional descriptions of the MCU Master SPI are provided within the Serial Interface Module section of the relevant MCU datasheet.

Application Circuits



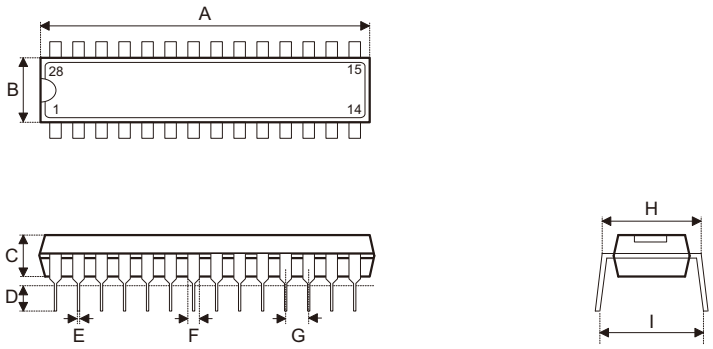
Note: "*" Recommended component for added ESD protection.

"**" Recommended component in environments where power line noise is significant.

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website (http://www.holtek.com.tw/english/literature/package.pdf) for the latest version of the package information.

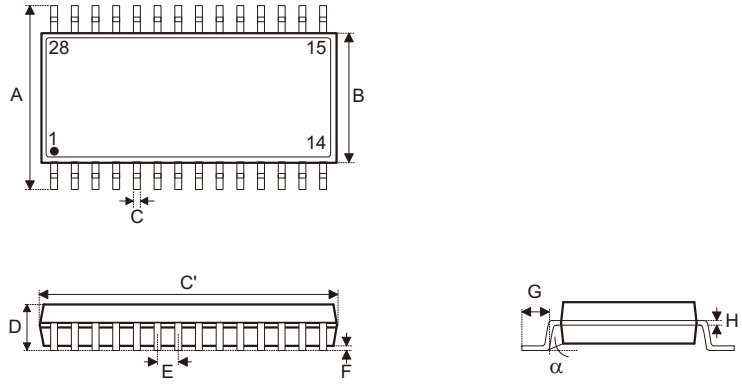
28-pin SKDIP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	1.375	—	1.395
B	0.278	—	0.298
C	0.125	—	0.135
D	0.125	—	0.145
E	0.016	—	0.020
F	0.050	—	0.070
G	—	0.100	—
H	0.295	—	0.315
I	—	0.375	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	34.93	—	35.43
B	7.06	—	7.57
C	3.18	—	3.43
D	3.18	—	3.68
E	0.41	—	0.51
F	1.27	—	1.78
G	—	2.54	—
H	7.49	—	8.00
I	—	9.53	—

28-pin SOP (300mil) Outline Dimensions

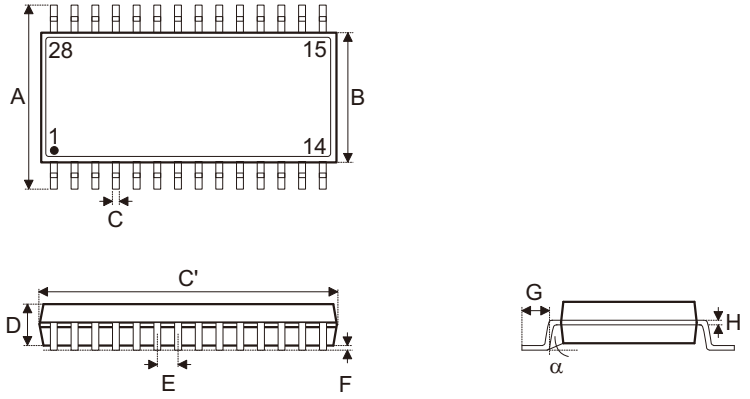


• MS-013

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.393	—	0.419
B	0.256	—	0.300
C	0.012	—	0.020
C′	0.697	—	0.713
D	—	—	0.104
E	—	0.050	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.98	—	10.64
B	6.50	—	7.62
C	0.30	—	0.51
C′	17.70	—	18.11
D	—	—	2.64
E	—	1.27	—
F	0.10	—	0.30
G	0.41	—	1.27
H	0.20	—	0.33
α	0°	—	8°

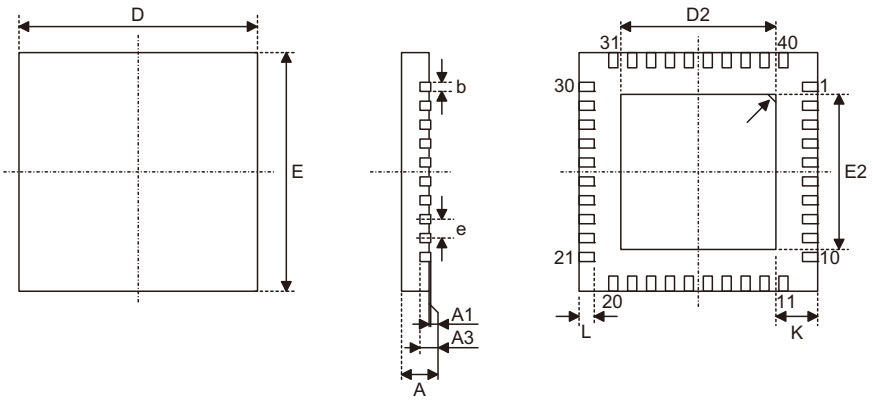
28-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.008	—	0.012
C′	0.386	—	0.394
D	0.054	—	0.060
E	—	0.025	—
F	0.004	—	0.010
G	0.022	—	0.028
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.20	—	0.30
C′	9.80	—	10.01
D	1.37	—	1.52
E	—	0.64	—
F	0.10	—	0.25
G	0.56	—	0.71
H	0.18	—	0.25
α	0°	—	8°

SAW Type 40-pin (6mm×6mm for 0.75mm) QFN Outline Dimensions

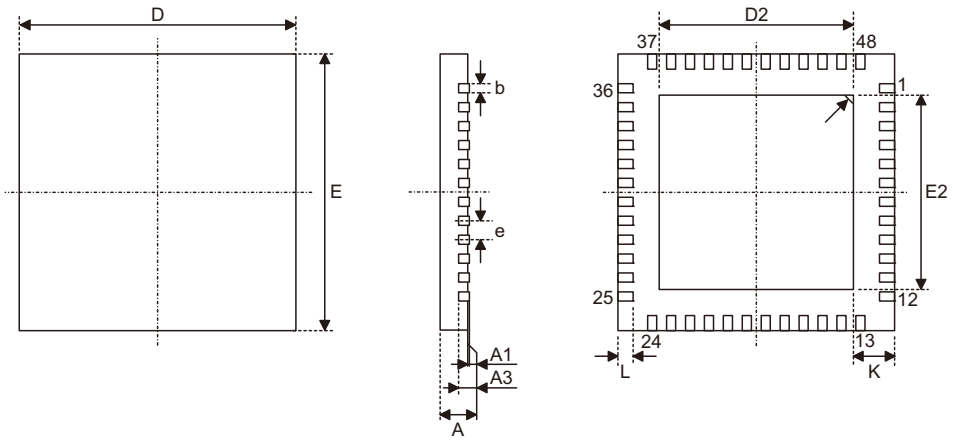


• GTK

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008	—
b	0.007	0.010	0.012
D	—	0.236	—
E	—	0.236	—
e	—	0.020	—
D2	0.173	0.177	0.179
E2	0.173	0.177	0.179
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.20	—
b	0.18	0.25	0.30
D	—	6.00	—
E	—	6.00	—
e	—	0.50	—
D2	4.40	4.50	4.55
E2	4.40	4.50	4.55
L	0.35	0.40	0.45
K	0.20	—	—

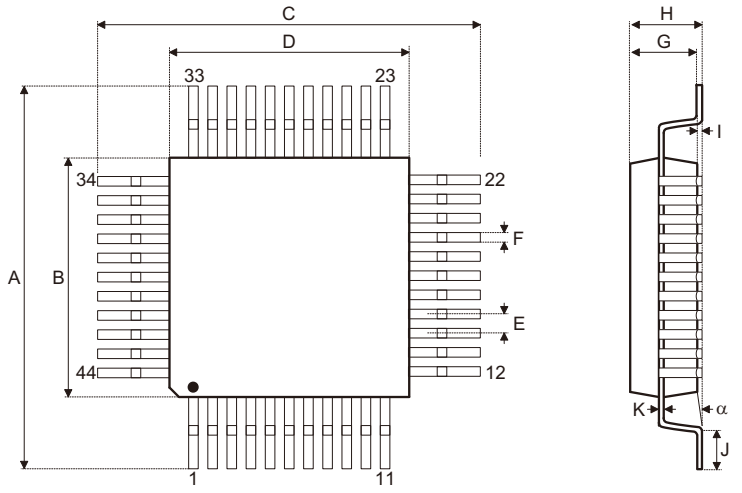
SAW Type 48-pin (7mm×7mm) QFN Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	—	0.031
A1	0.000	—	0.002
A3	—	0.008	—
b	0.007	—	0.012
D	—	0.276	—
E	—	0.276	—
e	—	0.020	—
D2	0.177	—	0.227
E2	0.177	—	0.227
L	0.012	—	0.020
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	—	0.80
A1	0.00	—	0.05
A3	—	0.203	—
b	0.18	—	0.30
D	—	7.00	—
E	—	7.00	—
e	—	0.50	—
D2	4.50	—	5.76
E2	4.50	—	5.76
L	0.30	—	0.50
K	0.20	—	—

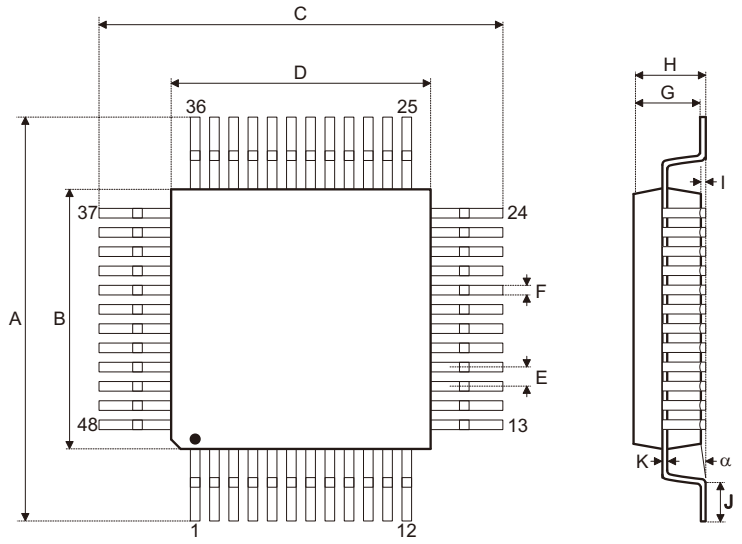
44-pin LQFP (10mm×10mm) (FP2.0mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.469	—	0.476
B	0.390	—	0.398
C	0.469	—	0.476
D	0.390	—	0.398
E	—	0.031	—
F	—	0.012	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	11.90	—	12.10
B	9.90	—	10.10
C	11.90	—	12.10
D	9.90	—	10.10
E	—	0.80	—
F	—	0.30	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

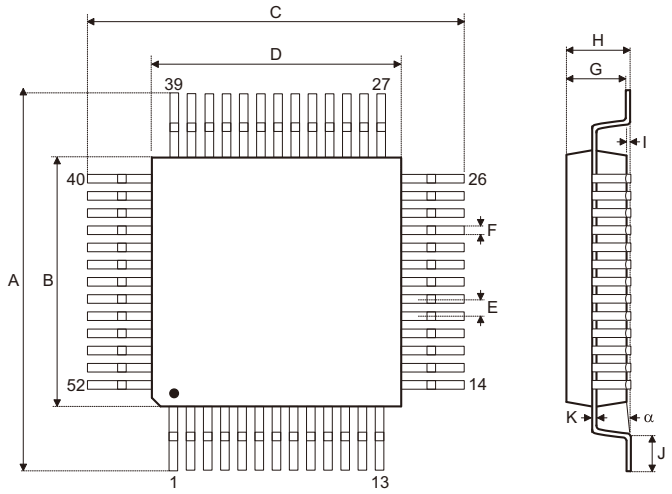
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.020	—
F	—	0.008	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

52-pin QFP (14mm×14mm) Outline Dimensions

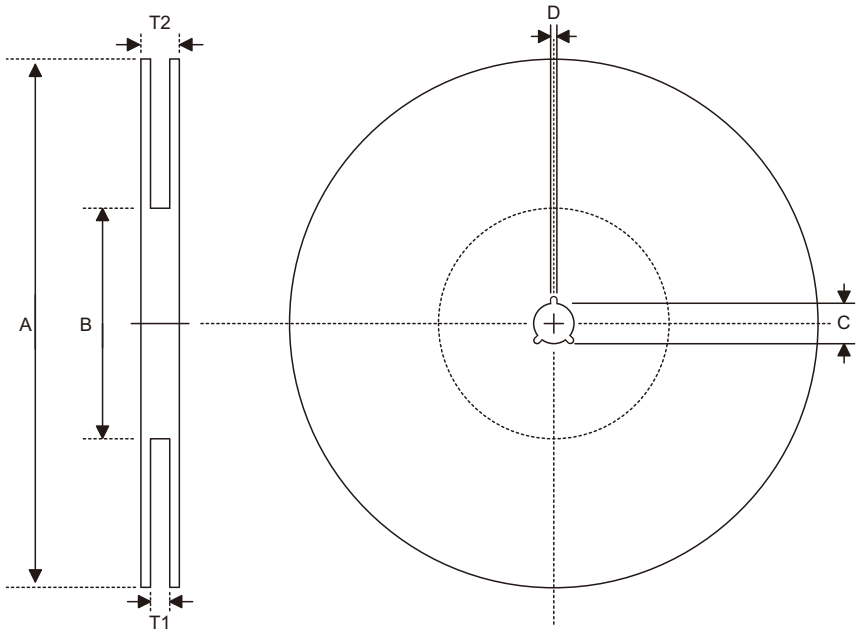


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.681	—	0.689
B	0.547	—	0.555
C	0.681	—	0.689
D	0.547	—	0.555
E	—	0.039	—
F	—	0.016	—
G	0.098	—	0.122
H	—	—	0.134
I	—	0.004	—
J	0.029	—	0.041
K	0.004	—	0.008
L	—	0.004	—
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	17.30	—	17.50
B	13.90	—	14.10
C	17.30	—	17.50
D	13.90	—	14.10
E	—	1.00	—
F	—	0.40	—
G	2.50	—	3.10
H	—	—	3.40
I	—	0.10	—
J	0.73	—	1.03
K	0.10	—	0.20
α	0°	—	7°

Product Tape and Reel Specifications

Reel Dimensions



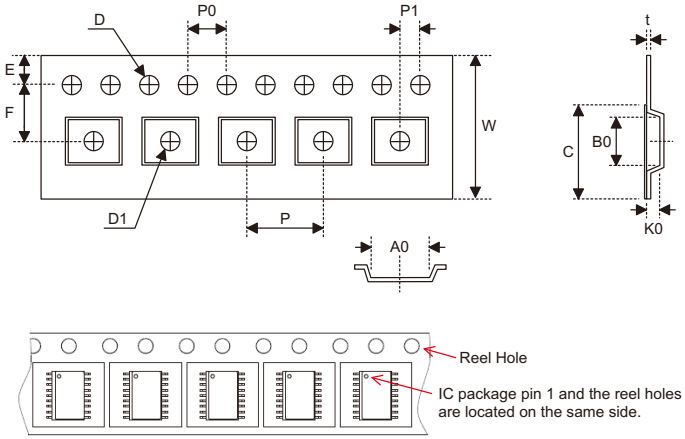
SOP 28W (300mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8 $^{+0.3/-0.2}$
T2	Reel Thickness	30.2±0.2

SSOP 28S (150mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	16.8 $^{+0.3/-0.2}$
T2	Reel Thickness	22.2±0.2

Carrier Tape Dimensions



SOP 28W (300mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.85±0.10
B0	Cavity Width	18.34±0.10
K0	Cavity Depth	2.97±0.10
t	Carrier Tape Thickness	0.35±0.01
C	Cover Tape Width	21.3±0.1

SSOP 28S (150mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0±0.3
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	$1.55^{+0.10/-0.00}$
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.5±0.1
B0	Cavity Width	10.3±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	13.3±0.1

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