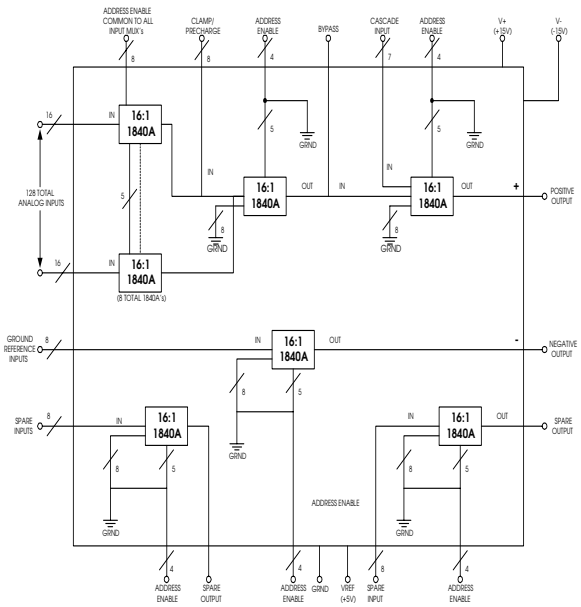
81840
128 Channel Multiplexer

See page 2 for pin assignments.



FEATURES:

- 128 channel multiplexer, MCM
- Package:
  - 256 pin RAD-PAK® quad flat pack
- Total dose hardness:
  - > 300 krads(Si)
- - Dependent upon orbit
- Excellent Single Event Effects:
  SEL: > 110 MeV-cm²/mg
  SEU: > 110 MeV-cm²/mg

DESCRIPTION:

Maxwell Technologies' 81840 high-performance 128-channel multiplexer features a typical 300 krad (Si) total dose tolerance. This datasheet defines the design, performance, and test requirements for a hermetic, telemetry multiplexer, multi-chip-module (MCM), utilizing chip and wire technology to be used in space systems. The 81840 is intended for use in the environments encountered by high reliability spacecraft applications. The patented radiation-hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. Capable of surviving in-space environment, the 81840 is ideal for satellite, spacecraft, and space probe missions. It is available up to Class K screening.

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81840 Pinout Diagram

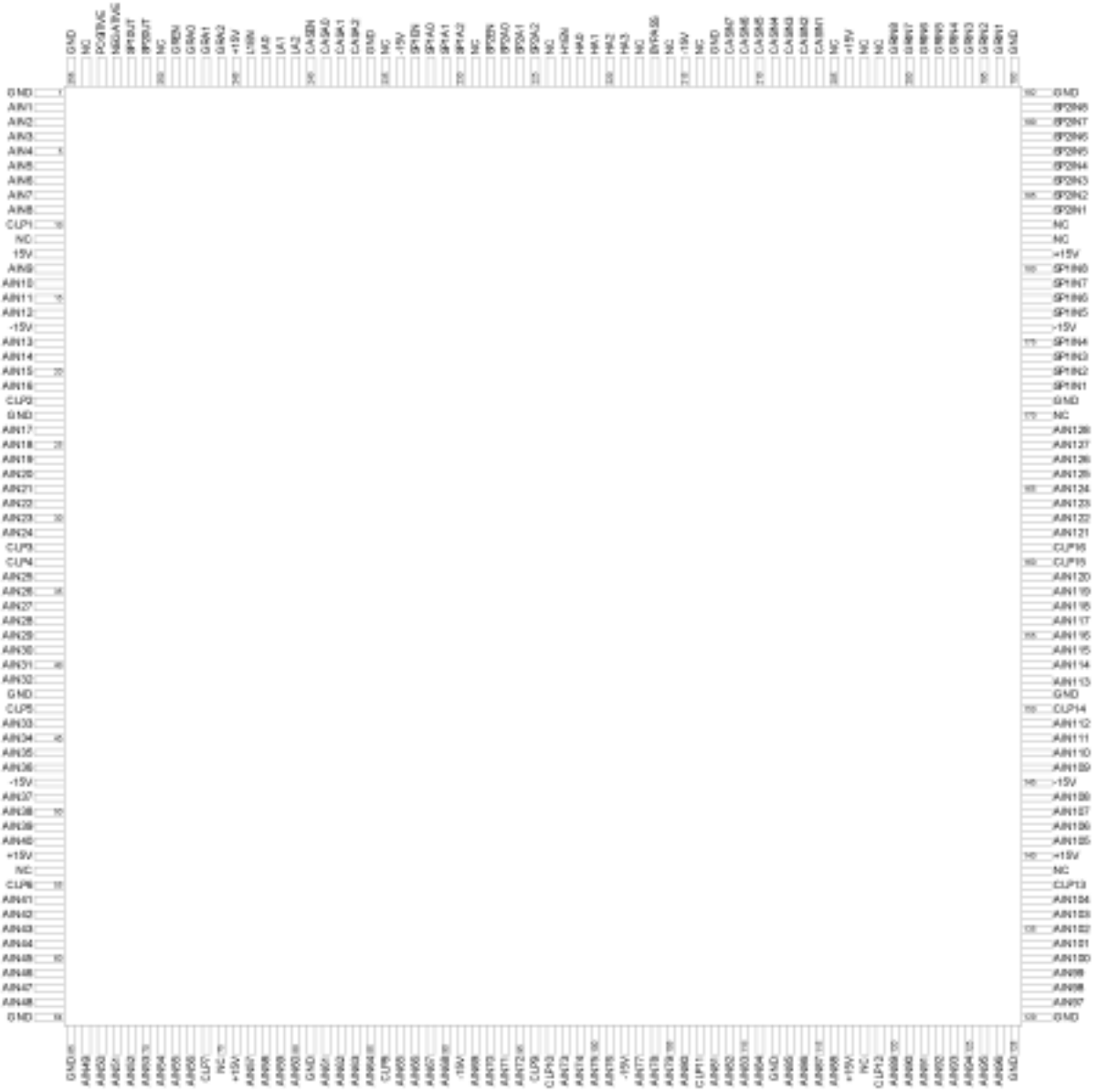


TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 23, 42, 64, 65, 81, 112, 128, 129, 151, 171, 192, 193, 213, 236, 256	GND	
2-9, 13-16, 18-21, 24-31, 34-41, 44-47, 49-52, 56-63, 66-73, 77-80, 82-85, 87-90, 92-95, 98-101, 103-106, 108-111, 113-116, 120-127, 130-137, 141-144, 146-149, 152-159, 162-169,	AIN1 - 128	
10, 22, 32, 33, 43, 55	CLP1 - 6	
11, 54, 75, 96, 97, 107, 117, 118, 138, 139, 150, 160, 161, 170, 182, 203, 214, 223, 228, 233, 240, 244, 249	NC	
12, 53, 76, 117, 140, 181, 204, 245	+15V	
17, 48, 91, 102, 145, 176, 215, 234	-15V	
172-175, 177-180	SP1IN1 - 8	
184-191	SP2IN1 - 8	
194-201	GRIN1 - 8	
183, 202, 250	+5V	
206-212	CASIN1 - 7	
216	H1EN	
217	BYPASS	
218	SP2EN	
224	SP1EN	
222-219	HA0 - 3	
227-225	SP2A0 - 2	
229	CASEN	
233-230	SP1A0 - 2	
235	L1EN	
239-237	CASA0 - 2	
243-241	LA0 - 2	
248-246	GRA0 - 2	
252	SP1OUT	
251	SP2OUT	
253	NEGATIVE	
254	POSITIVE	
255	GREN	

TABLE 2. 81840 ABSOLUTE MAXIMUM RATINGS[1,2,3,4]

ENVIRONMENT	RANGES
V+ To Ground	20V
V- To Ground	-20V
Input Overvoltage, AIN(1) to AIN(128)	35V to-35V (Power ON or OFF)
Input Overvoltage, Logic Inputs	4V over V_{REF} and -4V below Grd
Power Dissipation	500mW Maximum
Storage Temperature	-65 to 150°C
Operating Temperature	-55 to 125°C

1. The LMUX MCM is designed to operate with power supply voltages ranging from ±5.2V to ±20VDC.
2. The maximum voltage each input AIN(128:1) may see without damage is +35V to -35V with respect to ground.
3. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4. T_A = 25°C unless otherwise specified.

TABLE 3. 81840 AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SUBGROUPS	TEST LIMITS						UNITS
			T_A = 25°C		T_A = 125°C		T_A = -55°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
Address Input to I/O Channels Prop. Delay $t_{ON(A)}$ $t_{OFF(A)}$	V_{IN} = 5.0V R_L = 5kΩ C_L = 50pF	9, 10, 11	 -- --	 1500 1500	 -- --	 1500 1500	 -- --	 1500 1500	nsec
Enable to I/O $t_{ON(EN)}$ $t_{OFF(EN)}$	V_{IN} = 5.0V R_L = 5kΩ C_L = 50 pF	9, 10, 11	 -- --	 1500 1500	 -- --	 1500 1500	 -- --	 1500 1500	nsec
On Channel Isolation $V_{ISO(ON)}$	All enable = 0.8V V_{IN} = 3V_{RMS} @ 500kHz[1]	4, 5, 6	45	--	45	--	45	--	db
Off Channel Isolation $V_{ISO(OFF)}$	All enable = 4.0V V_{IN} = 3V_{RMS} @ 500kHz[1]	4, 5, 6	45	--	45	--	45	--	db

1. Controlled by design, not directly tested.

Table 4. Delta Limits

Parameter	Variation
I_{S+}	±10%
I_{S-}	±10%
I_{SB+}	±10%
I_{SB-}	±10%

Table 5. 81840 Electrical Test Table

Parameter	Test Conditions	Subgroups	Test Limits						Units
			T_A = 25°C		T_A = 125°C		T_A =-55°C		
			Min	Max	Min	Max	Min	Max	
Analog Signal Range, V_0			-15	15	-15	15	-15	15	V
Bypass Output, On-Resistance, 5V, $R_{BP(ON)}$	V_{IN} = 5V I_{OUT} = -1.0mA	1, 2, 3	2.0	6.0	2.0	6.0	2.0	6.0	kΩ
Positive Output, On-Resistance, 5V, $R_{PO(ON)}$	V_{IN} = 5V I_{OUT} = -1.0mA	1, 2, 3	3.0	9.0	3.0	9.0	3.0	9.0	kΩ
Negative or Spare Output, On-Resistance, 5V, $R_{NS(ON)}$	V_{IN} = 5V I_{OUT} = -1.0mA	1, 2, 3	1.0	3.0	1.0	3.0	1.0	3.0	kΩ
Bypass Output, On-Resistance, -5V, $R_{BP(ON)}$	V_{IN} = -5V I_{OUT} = 1.0mA	1, 2, 3	2.0	6.0	2.0	6.0	2.0	6.0	kΩ
Positive Output, On-Resistance, -5V, $R_{PO(ON)}$	V_{IN} = -5V I_{OUT} = 1.0mA	1, 2, 3	3.0	9.0	3.0	9.0	3.0	9.0	kΩ
Negative or Spare Output, On-Resistance, -5V, $R_{NS(ON)}$	V_{IN} = -5V I_{OUT} = 1.0mA	1, 2, 3	1.0	3.0	1.0	4.0	1.0	4.0	kΩ
Input Leakage Current, LA0, LA1, LA2, HA0, LIEN, Address or Enable Pins, I_{AH}, I_{AL}	All unused pins = Ground	1, 2, 3	-100	100	-200	200	-200	200	nA
Input Leakage Current, All Other Address or Enable Pins I_{AH}, I_{AL}	All unused pins = Ground	1, 2, 3	-100	100	-200	200	-200	200	nA
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, $+I_{S(OFF)}$	V_{IN} = 10V, All enables = 4.0V All unused inputs & outouts = -10V	1, 2, 3	-20	20	-100	100	-100	100	nA
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, $-I_{S(OFF)}$	V_{IN} = -10V All enables = 4.0V All unused inputs & outputs = +10V	1, 2, 3	-20	20	-100	100	-100	100	nA

TABLE 5. 81840 ELECTRICAL TEST TABLE

PARAMETER	TEST CONDITIONS	SUBGROUPS	TEST LIMITS						UNITS
			T_A = 25°C		T_A = 125°C		T_A =-55°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, Power off, $+I_{S(OFF)PO}$	VIN = 25V V_S+, V_S-, V_{REF}, V_A, V_{EN} & All unused inputs = Ground	1, 2, 3	-50	50	-100	100	-100	100	nA
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, Positive Overvoltage, $+I_{S(OFF)0V}$[1]	VIN = 35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 0.0V All enables = 4.0V All unused = GND	1, 2, 3	-100	100	-200	200	-200	200	nA
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, Negative Overvoltage, $-I_{S(OFF)0V}$[1]	V_{IN} = -35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE =0.0V All enables = 4.0V All unused = GND	1, 2, 3	-100	100	-200	200	-200	200	nA
Leakage Current into MUX Output Channels, SP1OUT, SP2OUT, POSITIVE, NEGATIVE, Positive Overvoltage, $+I_{D(OFF)0V}$[1]	V_{IN} = 35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 0.0V All enables = 4.0V All unused = GND	1, 2, 3	-75	75	-200	200	-200	200	nA
Leakage Current into MUX Output Channels, CLPx, BYPASS, $+I_{D(OFF)0V}$[1]	V_{IN} = 35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 0.0V All enables = 4.0V All unused = GND	1, 2, 3	-100	100	-400	400	-400	400	nA
Leakage Current into MUX Output Channels, SP1OUT, SP2OUT, POSITIVE, NEGATIVE, Negative Overvoltage, $-I_{D(OFF)0V}$[1]	V_{IN} = -35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = -10V All enables = 4.0V All unused = 0.0V	1, 2, 3	-75	75	-200	200	-200	200	nA
Leakage Current into MUX Output Channels, CLPx, BYPASS, $-I_{D(OFF)0V}$[1]	V_{IN} = -35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = -10V All enables = 4.0V All unused = 0.0V	1, 2, 3	-100	100	-400	400	-400	400	nA

TABLE 5. 81840 ELECTRICAL TEST TABLE

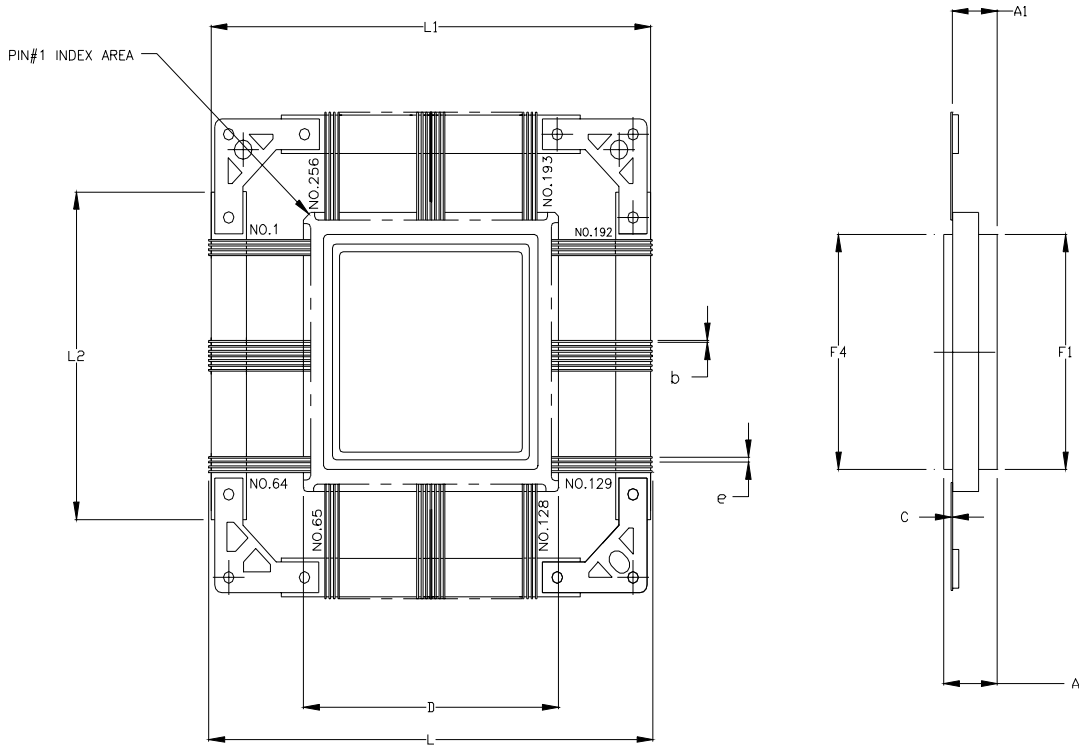
PARAMETER	TEST CONDITIONS	SUBGROUPS	TEST LIMITS						UNITS
			T_A = 25°C		T_A = 125°C		T_A =-55°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
Leakage Current into off MUX Output Channels, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE, $+I_{D(OFF)}$	All V_{IN} = 10V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE NEGATIVE = 10V All enables = 0.8V All unused = 0.0V	1, 2, 3	-20	20	-100	100	-100	100	nA
Leakage Current into off MUX Output Channels, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE, $-I_{D(OFF)}$	All V_{IN} = -10V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 10V All enables = 0.8V All unused = 0.0V	1, 2, 3	-20	20	-100	100	-100	100	nA
Leakage Current into on MUX Output Channels, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE, $-I_{D(ON)}$ Note: Sequence all inputs for each output.	Output and Input Under Test = 10V All unused V_{IN} = 10V All enables = 0.8V	1, 2, 3	-20	20	-100	100	-100	100	nA
Leakage Current into on MUX output Channels, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE, $I_{D(ON)}$ Note: Sequence all inputs for each output	Output and Input Under Test = -10V All unused V_{IN} = -10V All enables = 0.8V	1, 2, 3	-20	20	-100	100	-100	100	nA
V_{REF}		1, 2, 3	4.5	7.0	4.5	7.0	4.5	7.0	V
Input Voltage Low V_{IL}[2]	V_{IN} = 5.0V	1, 2, 3	--	0.3 V_{ref}	--	0.3 V_{ref}	--	0.3 V_{ref}	V
Input Voltage High V_{IH}[2]	V_{IN} = 5.0V	1, 2, 3	0.7 V_{ref}	--	0.7 V_{ref}	--	0.7 V_{ref}	--	V
Supply Current for I_{S+} I_{S-}	All enables = 0.8V	1, 2, 3	0.65 -0.65	6.5 -6.5	0.65 -0.65	6.5 -6.5	0.65 -0.65	6.5 -6.5	mA
Standby Supply Current for I_{SB+} I_{SB-}	All enables = 0.8V	1, 2, 3	0.65 -0.65	6.5 6.5	0.65 -0.65	6.5 -6.5	0.65 -0.65	6.5 -6.5	mA

1. Current limit set to 10 µA during test.

2. For V_{IH} and V_{IL} measurements, V_{REF} will equal 4.5V and 5.5V.
3. Unless otherwise specified:
   - V- = -15.0V
   - V+ = 15.0V
   - V_{REF} = 5.0V
   - V_{AH} = 4.0V
   - V_{AL} = 0.8V

FIGURE 1. 81840 ADDRESS DECODING SCHEME

ADDRESS INPUTS LA (0,4)	TELEMETRY CHANNEL
0 0 0 0 0 0 0	AIN(1)
0 0 0 0 0 0 1	AIN(2)
0 0 0 0 0 1 0	AIN(3)
0 0 0 0 0 1 1	AIN(4)
0 0 0 0 1 0 0	AIN(5)
0 0 0 0 1 0 1	AIN(6)
0 0 0 0 1 1 0	AIN(7)
0 0 0 0 1 1 1	AIN(8)
0 0 0 1 0 0 0	AIN(9)
"	
"	
"	
1 1 1 0 1 1 1	AIN(121)
1 1 1 1 0 0 1	AIN(122)
1 1 1 1 0 1 0	AIN(123)
1 1 1 1 0 1 1	AIN(124)
1 1 1 1 1 0 0	AIN(125)
1 1 1 1 1 0 1	AIN(126)
1 1 1 1 1 1 0	AIN(127)
1 1 1 1 1 1 1	AIN(128)



256-PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	.302	.329	.356
b	.005	.007	.009
c	.005	.006	.007
D	1.438	1.450SQ	1.462
D1		1.260BSC	
e		.020BSC	
L	3.010	3.040	3.070
L1	2.970	3.000	3.030
L2	2.178	2.200	2.222
A1	.253	.275	.297
N		256	
F1	1.215	1.220	1.225
F4	1.215	1.220	1.225

Q256-01
All dimensions in inches

Important Notice:

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