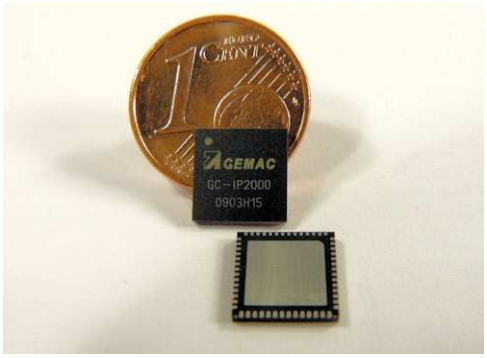
GC-IP2000



Datasheet

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Revision Overview

Date	*Revision*	*Change(s)*
03.05.07	1.0	First version (preliminary), provisional pin assignment
19.03.09	1.1	Package fixed Some Parameter fixed Figures added Application notes added
08.05.09	1.2	Temperature range
26.03.10	1.3	Parameters Pin XA added Parameters reference comparator added Package drawings added Nominal amplitude 80mV_{pp} changed to 75 mV_{pp} Further product links added

Table of Contents

1 Overview

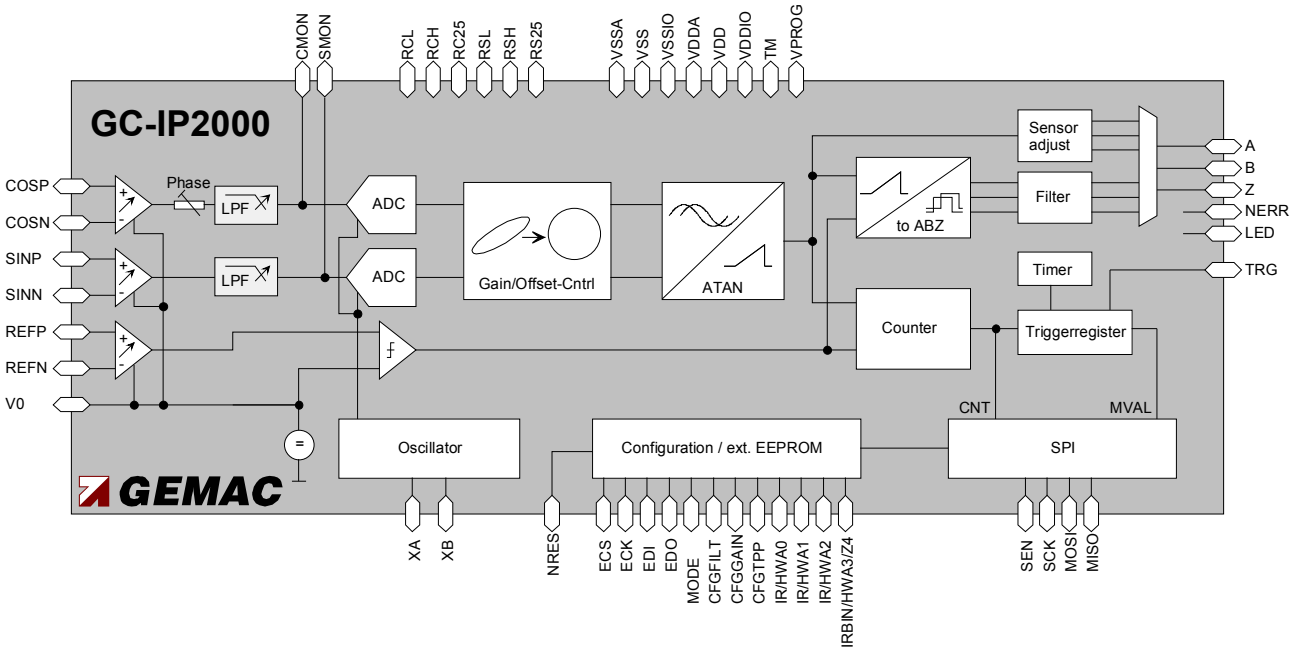
The interpolation circuit GC-IP2000 serves to increase the resolution for incremental position and angular measuring systems with sinusoidal output signals offset by 90°. The IC divides the signal period up to 2048 times.

The GC-IP2000 comprises three instrument amplifiers with adjustable gain factors. Incremental encoders which possess a voltage interface and measuring bridges can be connected directly. Sensors with current interface and photodiode-arrays are adapted by a simple external circuit. The IC may operate with both single-ended and differential input signals. The noise of the sensor signals is prevented by a switching analog filter. Additionally, a digital hysteresis can suppress the edge noise of the output signals at low input frequencies and at standstill. Thus, in case of a short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors.

The input signals are subjected to a GEMAC-patented internal gain and offset control. The amplitude is controlled in the range between 60 % and 120 % of the nominal amplitude. The control range for the offset of the two input signals is ±10 % of the nominal amplitude. The phase displacement of the input signals can be corrected statically between -10° and +10° using a digital potentiometer. The quality of the signals issued by the sensors is monitored in the IC. For that purpose it is possible to activate separately 9 sources producing an error signal.

The propagation delay of the IC is only 5µs. A fast serial interface (SPI) is implemented. This interface operates at a clock frequency of up to 25MHz and is compatible to all important micro-controller and DSP families. In addition, a timer and a multi-stage trigger are implemented. This features make the GC-IP2000 an ideal choice for use in fast controllers or control systems.

The IC is configured specifically to the particular application via configuration pins, an EEPROM or via the serial interface of the GC-IP2000.



2 Features

Table 1 Overview

Analog Part	
Analog input	- Sinusoidal / cosinusoidal / reference (index) signals; differential or single ended - Adjustable amplification for 1 Vpp / 500 mVpp / 250 mVpp / 75 mVpp - Input frequency max. 260 kHz for all resolutions
Digital Part	
Interpolation rate	100 / 128 / 200 / 256 / 400 / 500 / 512 / 800 / 1000 / 1024 / 1600 / 2000 / 2048
Output signals	- 30-bit counter value via serial interface (SPI) - Up to 500000 measurement values per second - 90° square-wave sequences (A/B/Z) - Error signal - Interrupt signal to the µC - Auxiliary signals for sensor adjustment
Signal correction	- Patented digital controller for the offset, control range ±10 % of standard amplitude - Patented digital controller for the amplitude, control range factor 0.5 ... 1.5 - Digital potentiometer with 40 steps for phase correction; selectable range ±5° or ±10° - LED control signal
Possibilities of configuration	Either: via configuration pins, the serial interface (SPI) or EEPROM
SPI	- Compatible to the standard SPI: 16-bit, MSB first - SPI clock up to 25 MHz - For configuration and measuring value output; not required for trivial systems
Miscellaneous	
Supression of disturbances	- Switchable analog noise filter - Digital hysteresis for suppression of the edge noise at the output
Adaptation of IC to subsequent devices	- Adjustable minimum edge interval at the output - Behaviour of IC in case of sensor error can be programmed - Adjustable width zero signal Z of ¼ or 1 period A/B
Data logging	- 2-stage measured-value trigger - Programmable timer - Constant delay between sampling and measurement value of 5 µs for all resolutions
Important Characteristics	
Operating voltage	5 V DC
I/O voltage, digital:	3.3 V DC or 5 V DC
Temperature range:	- 40°C ... 125°C
Housing	
QFN56	- Pitch 0.5mm, 8mm x 8mm package

Ordering Information

Product Type	***Description***	***Item No.***
GC-IP2000	Interpolation IC GC-IP2000, QFN56	PR-44000-50
GP2000	Evaluationboard of Interpolation IC GC-IP2000	PR-44010-00
USB-SPI-GCIP2000	USB adapter to SPI interface of GC-IP2000	PR-44025-00

3 Typical applications of GC-IP2000

Signal Form (Sensor)	Application of GC-IP200
Sinusoidal, Voltage	Direct connection of GC-IP2000 to sensor
Sinusoidal, Current	Additional resistors required
Reference (Index)-Track	Direct connection of GC-IP2000 to sensor
Square wave	ICs are not suitable in principle; Hower, special resistornetwork and configuration allow using of the internal interpolation counter
Signal Form (Sensor)	**Application of GC-IP200**
$1V_{pp}$ nominal	Direct connection of GC-IP2000 to sensor
$75mV_{pp}$ nominal	Direct connection of GC-IP2000 to sensor
$250mV_{pp}$ nominal	Direct connection of GC-IP2000 to sensor
$500mV_{pp}$ nominal	Direct connection of GC-IP2000 to sensor
$2V_{pp}$ nominal	Additional resistors required
Differential signal, DC-Reference Voltage 1.5 ... 3.5V	Direct connection of GC-IP2000 to sensor
Single-Ended, DC-Reference Source in Sensor	Direct connection of GC-IP2000 to sensor
Single-Ended, DC-Reference Source not in Sensor	Direct connection of GC-IP2000 to sensor
Photodiodes 0.5µApp	Additional resistors required
Photodiodes 11..16µApp	Additional resistors required
Resistive bridges (magnetic read head)	Direct connection of GC-IP2000 to sensor
Unstable amplitude of sensor	GC-IP2000 contains automatic controler for amplitudes
Offset not correctable at sensor	GC-IP2000 contains automatic controler for offsets
Phase not correctable at sensor	GC-IP2000 contains potentionmeter for phase correction
Maximum signal frequencies	
Rotary encoder	f_{max} = (revolutions / minute)·(signalperiodes / revolution) / 60
Linear encoder	f_{max} = (v_{MAX} [in m/s] / (signal periode [in mm]) · 1000
f_{max} < 260kHz	**All interpolation rates up to 2048 via SPI**
f_{max} < 22MHz / Interpolation rate	If ABZ outputs are used

Complete System includes µController / DSP / FPGA	
Using of SPI – interface recommended	
System includes more than one channel	Possibility to use simultaneously on only one SPI-bus
Fast trigger processing required	Use trigger capability of GC-IP2000
Äquidistant Sampling required	Use trigger capability or timer; signal `Startsample` provided
Real-time system	Constant delay of only 5µs, SPI-Clock up to 25MHz
IC-Configuration	All registers configurable via SPI
System works with external Interpolation Counter	
ABZ-Mode of GC-IP2000 will be used	
Minimal accepted edge interval of the counter may limit the input frequency	
Maximal frequency of counter know	Adaption of GC-IP2000 possible via `CFGTPP`
Signal specification TTL/CMOS	ABZ-outputs used directly
Signal specification RS422	Driver-IC required
Configuration	EEPROM recommended, Configuration via pins possible
Limited system size	
Package	QFN56-package, 8mm x 8mm outline size
Minimal circuit	14 block-capacitors, quartz, 3 pullup resistors optional: EEPROM, optional:RS422 driver

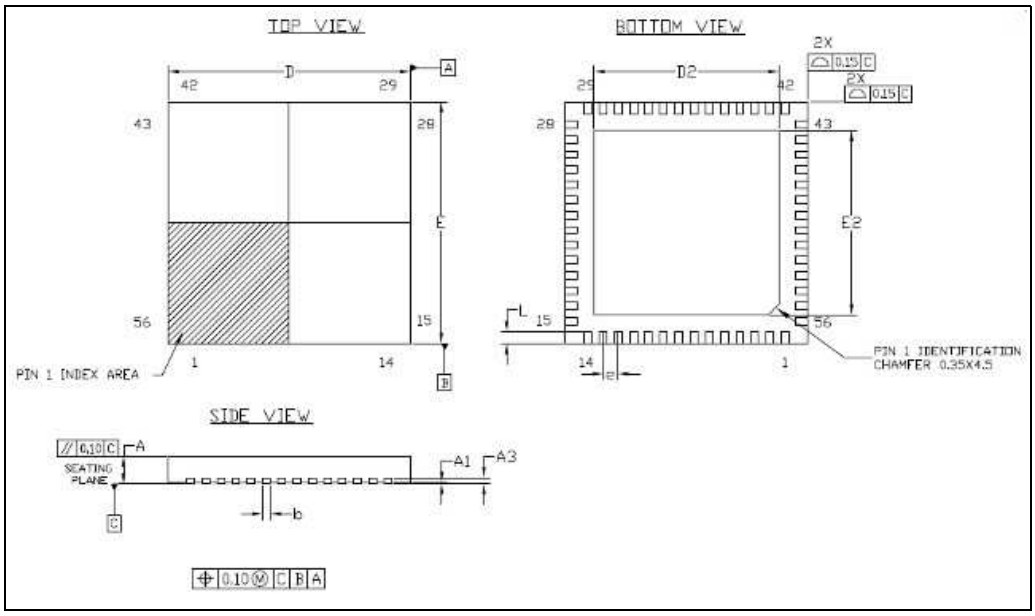
4 Pin Assignment

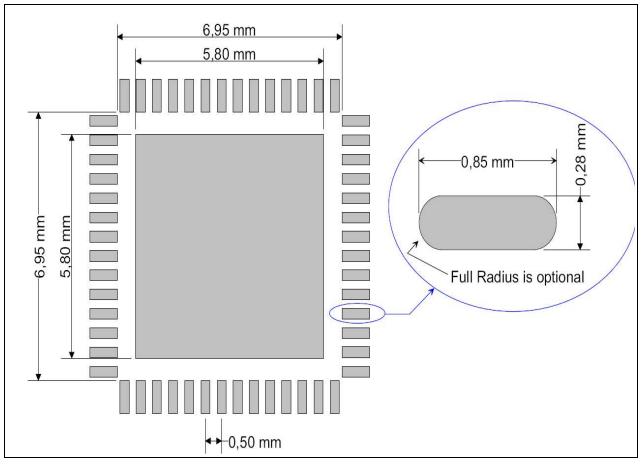
Table 2 Pin assignment

Pin	Name	Type	Meaning
1	N.C.	n.c.	Must not be connected
2	NRES	Analog I/O; Open Drain	Reset
3	TM	Digital input	Test mode; Connect to VSS!
4	XA/CLK	Oscillator	Clock cycle
5	XB	Oscillator	Clock cycle
6	VSS	Power	Digital GND
7	VDD	Power	Supply voltage, digital +5V
8	Z4/IRBIN/HWA3	Configuration input, 4-value	Configuration of the reference-point width, IRATE, SPI hardware address
9	CFGTPP	Configuration input, 4-value	Configuration of the minimum edge interval
10	CFGFILT	Configuration input, 4-value	Configuration of the glitch filter and of the digital hysteresis
11	RS25	Analog	Backup capacitor, ADC reference voltage 6
12	VSSA	Power	Analog GND
13	RSL	Analog	Backup capacitor, ADC reference voltage 4
14	RSH	Analog	Backup capacitor, ADC reference voltage 5
15	CFGGAIN	Configuration input, 4-value	Configuration of gain or standard amplitude
16	SMON	Analog output	Monitor output at instrument amplifier, sinusoidal
17	REFN	Analog input	Reference signal at input, negative
18	REFP	Analog input	Reference signal at input, positive
19	SINN	Analog input	Sinusoidal signal at input, negative
20	SINP	Analog input	Sinusoidal signal at input, positive
21	COSN	Analog input	Cosinusoidal signal at input, negative
22	COSP	Analog input	Cosinusoidal signal at input, positive
23	VDDA	Power	Supply voltage, analog +5V
24	VSSA	Power	Analog GND
25	V0	Analog output	Mean voltage
26	CMON	Analog output	Monitor output at instrument amplifier, cosinusoidal
27	MODE	Configuration input, 4-value	Configuration of the A/B/Z mode and test mode
28	N.C.	n.c.	Must not be connected
29	N.C.	n.c.	Must not be connected
30	RC25	Analog	Backup capacitor, ADC reference voltage 3
31	RCL	Analog	Backup capacitor, ADC reference voltage 1
32	VDDA	Power	Supply voltage, analog +5V
33	VSSA	Power	Analog GND
34	RCH	Analog	Backup capacitor, ADC reference voltage 2
35	LED	Output, 3-value (L,H,VDDIO/2)	Output for triggering an LED control
36	VPROG	Power	Supply voltage, digital +5V
37	VSSIO	Power	GND, digital I/Os
38	VDDIO	Power	Supply voltage, digital I/Os +5V or +3.3V
39	MISO	Digital output	SPI: Data output GC-IP2000
40	MOSI	Digital input	SPI: Data input GS-IP2000
41	SEN	Digital input	SPI:Enable
42	SCK	Digital input	SPI: Clock cycle
43	ECS	Digital output	EEPROM: Enable
44	ECK	Digital output	EEPROM: Clock cycle
45	EDI	Digital output	EEPROM: Data output GC-IP2000
46	EDO	Digital input	EEPROM: Data input GC-IP2000
47	TRG	Digital input	Trigger input
48	IR2/HWA2	Digital input	Configuration of the interpolation rate and SPI hardware address
49	IR1/HWA1	Digital input	Configuration of the interpolation rate and SPI hardware address
50	IR0/HWA0	Digital input	Configuration of the interpolation rate and SPI hardware address
51	VSS	Power	Digital GND
52	A	Digital output	Incremental output A
53	B	Digital output	Incremental output B
54	Z	Digital output	Output for the zero signal Z (reference signal / index)
55	NERR	Digital output; Open Drain	Error signal
56	N.C.	n.c.	Must not be connected
Exposed	DVSS	Package	To DVSS

ⓘ *It is imperative that a defined circuit is connected to each IC input.*

ⓘ *Pull-up resistors are required at the pins NRES, NERR and MISO.*





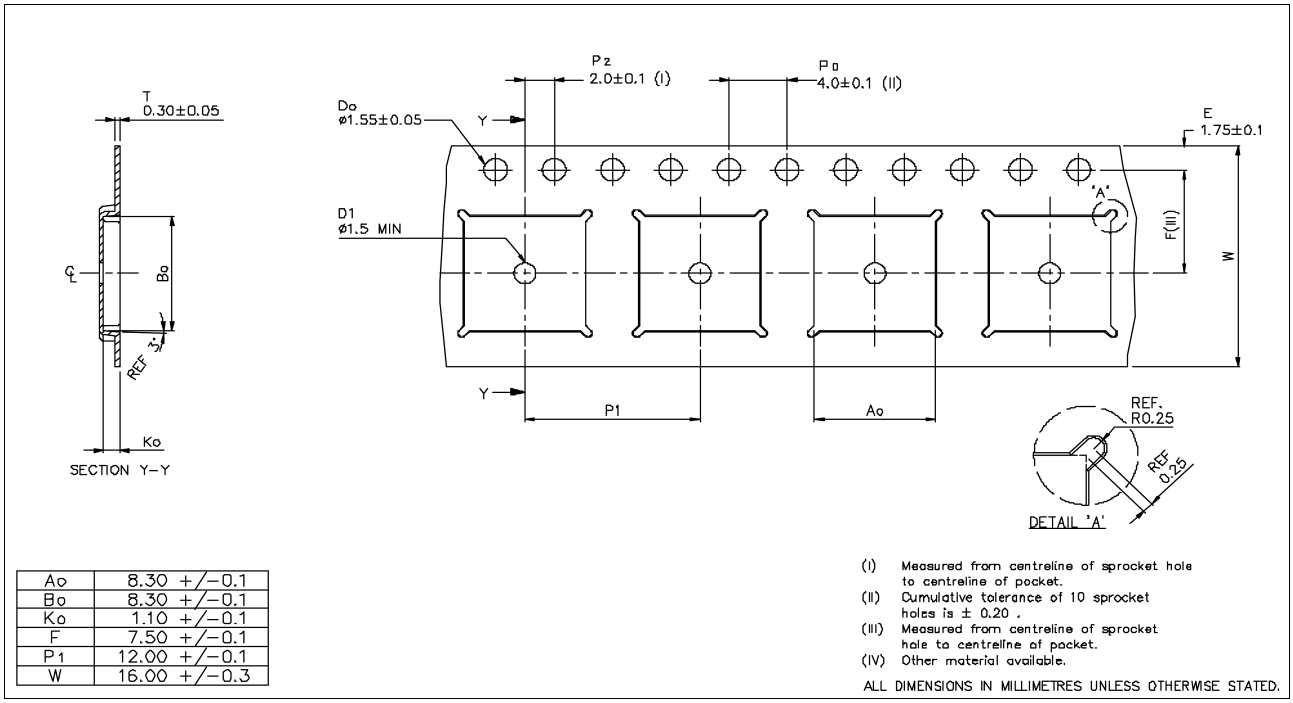
	Millimeter		
	Min	***Nom***	***Max***
A	0.85	0.90	0.95
A1	0.00		0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	7.85	8.00	8.15
D2	5.95	6.10	6.25
E	7.85	8.00	8.15
E2	5.95	6.10	6.25
e		0.50 BSC	
L	0.35	0.40	0.45

	Inch		
	Min	***Nom***	***Max***
A	0.033	0.035	0.037
A1	0.000		0.002
A3		0.008 REF	
b	0.008	0.010	0.012
D	0.310	0.315	0.320
D2	0.234	0.240	0.246
E	0.310	0.315	0.320
E2	0.234	0.240	0.246
e		0.020 BSC	
L	0.014	0.016	0.018

RoHS COMPLIANT 2002/95/EC

Notes

1 Dimensioning and tolerancing conform to ASME Y14.5M – 1994.
2 Controlling dimensions: millimeter. Converted inch dimensions not necessarily exact.
3 Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from terminal tip.
4 Drawings not to scale.
5 The recommended land pattern for pcb layout may be modified regarding to process capabilities.



Ao	8.30 +/−0.1
Bo	8.30 +/−0.1
Ko	1.10 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centrelne of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

5 Configuration

5.1 Reset

After resetting of the IC, all registers are initialised with their default values. Thereafter, the configuration pins are read into the appropriate registers. If a valid EEPROM is connected, the configuration registers are subsequently overwritten with the EEPROM values. During the whole RESET sequence, the pin MISO/nWAIT is maintained at L level. Subsequently, the configuration registers can be modified by way of the serial interface SPI. It is possible to connect the pins NERR and NRES to each other to be able to reconfigure the IC in case of error. In this case, the error pulse is active for at least 8 system cycles.

5.2 Configuration pins

The IC can be matched to the most varied measuring systems and subsequent electronic systems by way of two configuration registers. If the IC is initialised using an EEPROM or the SPI interface, full configuration possibilities are available. If the initialisation is performed via the configuration pins, the most important parameters can be set externally. The table below provides an overview of the configuration possibilities for the GC-IP2000. Further tables specify the meanings of the configuration pins.

Table 3 Configuration possibilities

Parameters	***Possible values***	***Pin***	***Register / bit***
Interpolation rate	2048,2000,1600,1024,1000,800 512,500,400,256,200,128,100	IR2 / IR1 / IR0 / IRBIN	CFG1 / IR(3:0)
Min. edge interval t_{pp}	1, 2, 4, 8, 16, 32, 64, 128	CFGTPP	CFG1 / TPP(2:0)
Reference point	Enable, Disable / 1 period, 1 increment	Z4	CFG1 / DISZ, Z4
Nominal signal amplitude	$1V_{pp}$, $500mV_{pp}$, $250mV_{pp}$, $75mV_{pp}$	CFGGAIN	CFG1 / GAIN(1:0)
Digital hysteresis	Enable, disable	CFGFILT	CFG1 / DHE
Output signals A/B/Z	ABZ mode, DSP mode, sensor adjustment	Mode	CFG1 / MODE (1:0)
Error processing	Masking, latch enable, LED pin	–	CFG1 / Mx, Lx, LEDMODE
Phase correction	± 10° step width 0.5°, ±5° step width 0.25°	–	CFG2 / PHBER, PH(5:0)
Low-pass filter	Enable, disable	–	CFG1 / LPF
Gain controller	Default setting / time constant / enable, disable	–	CNTRLG, CFG2 / GAINCTL, DISCTL
Offset controller	Default setting / time constant / enable, disable	–	CNTRLO, CFG2 / OFFSCTL, DISCTL
Trigger	Trigger pulse edge, measurement timer	–	CFG1 / TRGSLP, CFG2 / VT(1:0),T(7:0)
SPI mode	Synchronous, asynchronous	–	CFG2 / ASYNC, SYNC(4:0)
SPI hardware address	0-15	HWA(3:0)	CMD / SETHWA

Table 4 Configuration of the interpolation rate / SPI hardware address

Interpolation rate	***CFG1 - IR(3:0)***	***Pin IRBIN***	***Pin IR2***	***Pin IR1***	***Pin IR0***	***SPI hardware address***
2000	0000 (0)	VSS or V0	0	0	0	0
1600	0001 (1)	VSS or V0	0	0	1	1
1000	0010 (2)	VSS or V0	0	1	0	2
800	0011 (3)	VSS or V0	0	1	1	3
500	0100 (4)	VSS or V0	1	0	0	4
400	0101 (5)	VSS or V0	1	0	1	5
200	0110 (6)	VSS or V0	1	1	0	6
100	0111 (7)	VSS or V0	1	1	1	7
2048	1000 (8)	VDD or open	0	0	0	8
1024	1001 (9)	VDD or open	0	0	1	9
512	1010 (10)	VDD or open	0	1	0	10
256	1011 (11)	VDD or open	0	1	1	11
128	1100 (12)	VDD or open	1	0	0	12
1000	1101 (13)	VDD or open	1	0	1	13
1000	1110 (14)	VDD or open	1	1	0	14
1000	1111 (15)	VDD or open	1	1	1	15

See Section 6.2.1

Table 5 Configuration of the reference point

Reference-point width	*CFG1 - Z4*	*Pin Z4*
1 increment = ¼ period	0	VSS or VDD
4 increments = 1 period	1	V0 or open

See Section 6.2.2

Reference-point processing	*CFG1 - DISZ*
activated	0
deactivated	1

Table 6 Pin `Z4/IRBIN/HWA3`

Pin `Z4/IRBIN/HWA3`	*Interpolation rate*	*Reference-point width*	*SPI hardware address*
VSS	decimal	1 increment = ¼ period	< 8
VDD	binary	1 increment = ¼ period	≥ 8
V0	decimal	4 increments = 1 period	< 8
open	binary	4 increments = 1 period	≥ 8

Table 7 Configuration of the output signals

ABZ output signals	*CFG1 - MODE (1:0)*	*Pin MODE*
ABZ square-wave	00 (0)	VSS
Controller / DSP	01 (1)	VDD
Sensor adjustment 1	10 (2)	V0
Sensor adjustment 2	11 (3)	open

See Section 6.7

Table 8 Configuration of the signal amplitude (nominal value)

Input signals	*CFG1- GAIN(1:0)*	*Pin GAIN*
1 V_{pp}	00 (0)	VSS
500 mV_{pp}	01 (1)	VDD
250 mV_{pp}	10 (2)	V0
75 mV_{pp}	11 (3)	open

See Section 6.1

Table 9 Configuration of the minimum edge interval

Min. edge interval t_{pp}	*CFG1 – TPP(2:0)*	*Pin CFGTPP*
$1/f_{OSZ}$	000 (0)	VSS
$2/f_{OSZ}$	001 (1)	VDD
$4/f_{OSZ}$	010 (2)	V0
$8/f_{OSZ}$	011 (3)	open
$16/f_{OSZ}$	100 (4)	
$32/f_{OSZ}$	101 (5)	
$64/f_{OSZ}$	110 (6)	
$128/f_{OSZ}$	111 (7)	

See Sections 6.3.1 and 6.6

Table 10 Configuration of the hysteresis

Pin `CFGFILT`	*CFG1- DHE*	*CFG1-Bit 11*	*Digital hysteresis*
VSS	0	1	Don't use this configuration
VDD	1	1	Don't use this configuration
V0	0	0	deactivated
open	1	0	activated

See Section 6.3.2

6 Description of Functions

6.1 Input amplifier

The GC-IP2000 incorporates three instrument amplifiers with adjustable gain factors. Incremental encoders with a voltage interface and measuring bridges can be connected directly. Sensors with current interface are adapted by way of a simple external circuit. The IC operates with both single-ended and differential input signals. The amplification is identical for all signals of the sensor (sinusoidal, cosinusoidal, index/reference). To adapt the GC-IP2000 to customised sensors, the mean voltage of the instrument amplifier is provided at pin V0.

6.1.1 Input signals

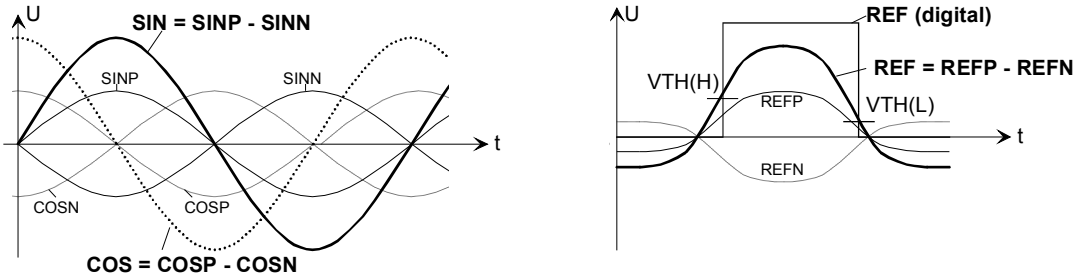


Fig. 1 Input signals

Table 11 Description of the input amplifier

CFGGAIN	***VSS(A)***	***VDD(A)***	***V0***	***open***
Configuration bits CFG1 – GAIN(1:0)	**00**	**01**	**10**	**11**
Input voltage for differential supply [1] (mV_{pp})	500	250	125	37.5
Input voltage U_{Diff} nominal (mV_{pp})	1000	500	250	75
Input voltage range for U_{Diff} (mV_{pp})	600-1200	300-600	150-300	45-90
Lower switching point of the reference comparator, nominal (mV)	+43	+21	+11	+3
Upper switching point of the reference comparator, nominal (mV)	-19	-9	-5	-1
Bit CFG1 / LPF	recommended	recommended	recommended	**necessary**

[1] at each of the inputs SINP, SINN, COSP, COSN

ⓘ *Measuring systems without reference signal require a defined state (always active or always inactive) to be set via the pins REFP and REFN.*

6.2 Interpolation

The signal periods of the analog sinusoidal (SIN) and cosinusoidal input signals (COS) are divided acording to the selected interpolation rate and provided to the serial interface (SPI) as a count value. Up to two measured values can then be saved in the IC asynchronously to the access via the serial interface using a trigger input or a configurable timer. In parallel, square-wave sequences with 90° phase shift (A/B/Z signals) are generated.

ⓘ *Please note that the GC-IP2000 uses the digital interpolation method. This causes the speed-proportional A/B/Z output signals to be overlaid by the inevitable quantising errors (the so-called ±1INK errors) resulting from the A/D converters. The quantisation noise can be suppressed by activating the digital hysteresis.*

6.2.1 Interpolation rate

Possible interpolation rates (IRATE) which can be selected are 2048, 2000, 1600, 1024, 1000, 800, 512, 500, 400, 256, 200, 128 or 100. The term 'interpolation rate' is here understood as the number of increments into which the sinusoidal/cosinusoidal period of the input signals is divided. This corresponds to the number of signal transitions at the A/B outputs per input signal period. The number of square-wave periods at the outputs A and B amounts to ¼ of the interpolation rate.

6.2.2 Zero signal Z

The zero signal Z is generated when the sinusoidal and cosinusoidal analog signals display a phase angle of 45° and at the same time the differential voltage of the reference inputs REFP and REFN exceeds the switching point. The switching points of the reference signal must lie in the range between 45°± [90°...150°]. The width of the zero signal Z (reference pulse) at the output can be switched between 1 and 4 increments, i.e. between ¼ and 1 period of the output signals A and B. If the IC is configured to the reference width of 1 increment (¼ period), the outputs A and B carry H level with activated Z signal.

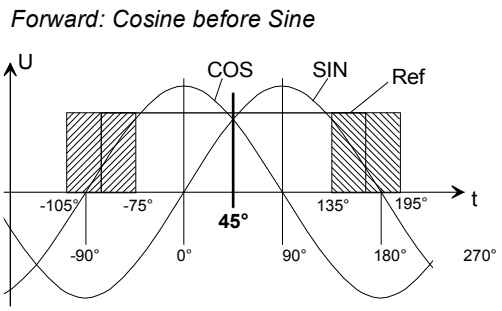


Fig.2 Interpolation input signals

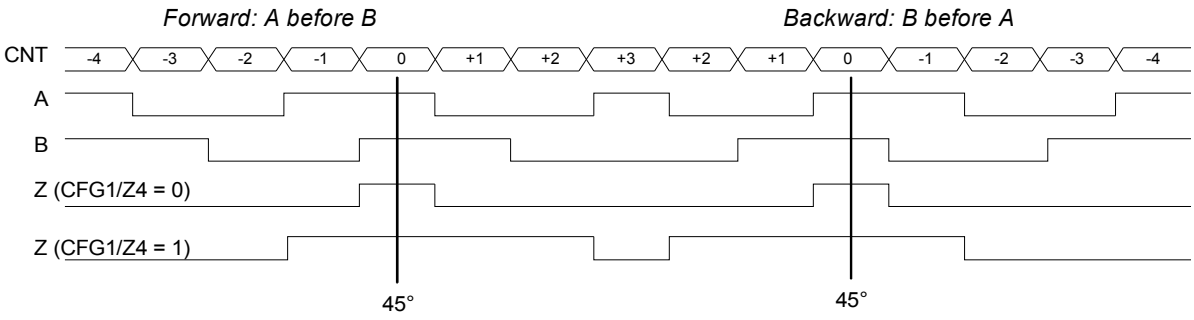


Fig.3 Interpolation output signals

ⓘ The *signals* A, B *and* Z *are offse*t in time by 1 increment if the digital hysteresis is activated.

6.3 Supression of disturbances

6.3.1 Edge interval setting

The minimum time interval t_{pp} at which the output signals A, B and Z may switch can be adjusted in binary steps between $1/f_{OSZ}$ and $128/f_{OSZ}$. After switching of one of the outputs, the subsequent edge of the other signal will only be visible at the IC output after the time t_{pp} has elapsed. Thus, in case of a short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors. The configuration of edge interval t_{pp} depends on the counter connected to A, B and Z. (see Section 6.6.1)

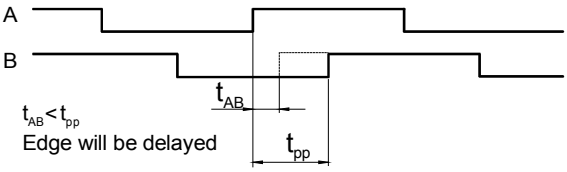


Fig. 4 Edge intervall setting

6.3.2 Noise filter / Digital hysteresis

The instrument amplifiers are connected to the internal A/D converters via a switchable low-pass filter. The corner frequency of the filter can be changed to attenuate the noise of the sensor signals. In this case either the maximum frequency of input signals will be limited to approx. 100KHz or the control range of amplitude will be smaller at high input frequencies.

To suppress the edge noise of the output signals at low input frequencies and standstill, a digital hysteresis can be activated for the signals A, B and Z. This prevents switching of the outputs with static input signals. In this case, all output signals are delayed by one increment.

Following figures show in an exemplary manner the effect of noise filter and digital hysteresis for strong disturbed input signals:

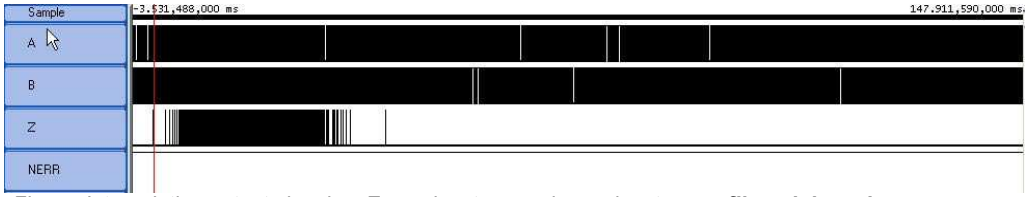


Fig. 5 Interpolation output signals – Example: strong noise on inputs – ***no filter aktivated***

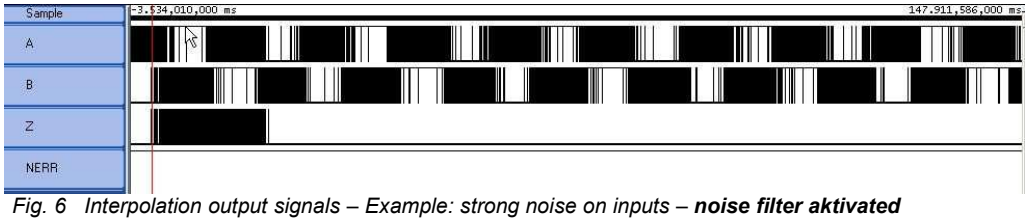


Fig. 6 Interpolation output signals – Example: strong noise on inputs – ***noise filter aktivated***

Fig. 7 Interpolation output signals – Example: strong noise on inputs – ***digital hysteresis aktivated***

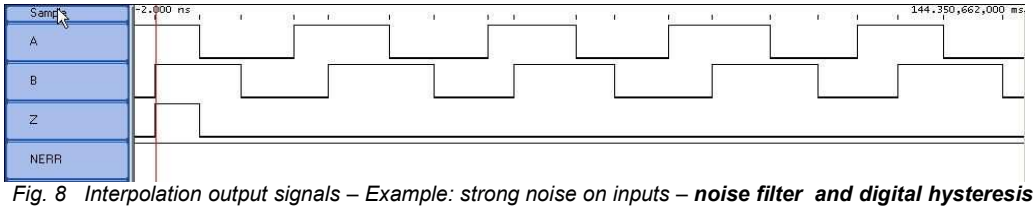


Fig. 8 Interpolation output signals – Example: strong noise on inputs – ***noise filter and digital hysteresis aktivated***

6.4 Signal correction

The input signals are subjected to a GEMAC-patented internal gain and offset control. The amplitudes are controlled in the range between 60 % and 120 % of the standard amplitude. The control range for the offset of the two input signals is ±10 % of the nominal amplitude. The phase displacement of the input signals can be corrected statically in 40 steps using a digital potentiometer. The setting range of the phase is set to approx. ±5° or approx. ±10° by way of a configuration bit. After resetting of the IC, start values to correct amplitude and offset of the two input signals are loaded from the EEPROM. If no EEPROM is connected, these values are set to the centre of the control range. The full measuring accuracy of the IC, however, is only achieved after settling of the internal signal control. To achieve the maximum possible accuracy in the amplitude and offset control, the phase potentiometer must be matched with the sensor connected to the GC-IP2000. Amplitude and offset errors are treated as a unit in the GC-IP2000. This means that for particular applications a larger permissible error may be permitted for the respectively other parameter under certain circumstances. The attenuation of the controlled system implemented in the GC-IP2000 can be adjusted.

Table 12 Signal correction

Parameter	***as a percentage referred to the nominal amplitude (PEAK-PEAK)***	***as a percentage referred to the ADC maximum (PEAK-PEAK)***	***in mV referred to the standard signal ($1V_{pp}$)***	***in V on the pin SMON or CMON***
Maximal value at the input	150	100	1500	3.15
Nominal value of the input signal	**100**	**66.7**	**1000**	**2.10**
Guaranteed control range for the amplitude	60 ... 120	40 ... 80	600 ... 1200	1.26 ... 2.52
Setting range of the amplitude controller	56 ... 168 [1)]	38 ... 112 [1)]	560 ... 1680 [1)]	1.18 ... 3.53 [1)]
Vector monitoring[2)]	30	20	300	0.63
Guaranteed control range for the offset (sensor)	±10	±6.7	±100	± 0.210
Setting range of the offset controller	±25	±17	±250	± 0.525

[1)] The setting range for the amplitude is greater than the control range of the ADC. Therefore, the upper limit of the setting range cannot be fully utilised for the analog signals.

[2)] An aggregate signal from sine and cosine is monitored.

Control ranges amplitude and offset

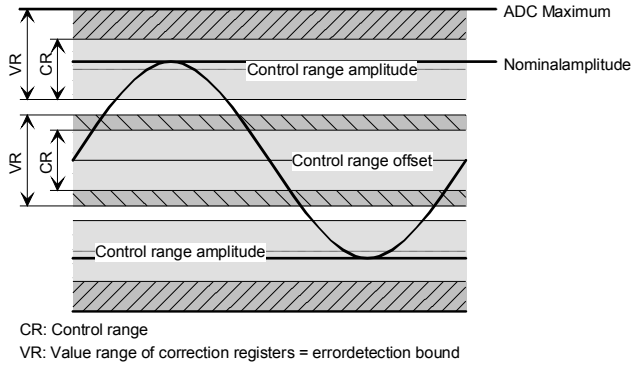


Fig. 9 Signal correction

6.5 Sensor monitoring

The IC provides 9 sources for generation of an error signal. Each source can be activated or deactivated using the relevant bit in the register CFG1. Saving of the individual error flags can be activated using one further configuration bit each. The OR combination of the error signals saved or masked in this way is provided at the pin NERR (L-active). The behaviour of the square-wave outputs in case of error can also be configured. Furthermore, it is possible to connect the pins NERR and NRES to each other to reconfigure the IC in case of error. In this case, the error pulse is active for at least 8 system cycles. The NERR pin is implemented as an open-drain pin. Thus, it is possible to connect the error outputs of several ICs GC-IP2000 to each other.

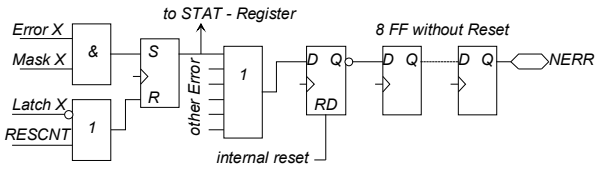


Fig. 10 Error processing

ⓘ If the error signal has been activated or one of the error bits has been set in the result register, the current measurement result and all subsequent results must be discarded. After rectification of the error cause and resetting of the error bits (SPI command: RESCNT), it is imperative to pass through the reference point to be able to perform further absolute measurements.

6.5.1 Behaviour of the outputs A, B and Z in case of error

In case of error, the behaviour of the outputs A, B and Z is not defined. If the HLD bit is set in the register CFG1, the outputs will not change in case of error. The error signal will be active for at least the time t_{pp}. If the latch enable bit (Lx) is set in the register CFG1 for a special error, the appropriate error signal is saved up to the next reset of the IC or until the next SPI command RESCNT.

6.5.2 Error sources

Vector error

The signal vector generated from the sinusoidal and cosinusoidal signals is too small. Usually, the cause is a partly or completely disconnected sensor. Another cause are input signals with very large offset at simultaneously low amplitude.

	Masking	***Memory enable***	***STATUS register***
Bit	MVLOW	LVLOW	EVLOW

ADC error

One or both A/D converters are overdriven. The cause is that the signal amplitude is too high. Another cause are input signals with very large offset at simultaneously high amplitude. If appropriate pull-up or pull-down resistors are connected to the signal inputs, partly or fully disconnected sensors can also be detected by way of this error bit.

	Masking	***Memory enable***	***STATUS register***	
Bit	MADC	LADC	ESADC (sine)	ECADC (cosine)

Offset error

The offset controller has reached its limit. The cause is an excessive signal offset, a partly or fully disconnected sensor or an invalid value for initialisation of the offset controller.

	Masking	***Memory enable***	***STATUS register***	
Bit	MOFF	LOFF	ESOFF (sine)	ECOFF (cosine)

Amplification error

The gain controller has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.

	Masking	***Memory enable***	***STATUS register***	
Bit	MGAIN	LGAIN	ESGAIN (sine)	ECGAIN (cosine)

Speed error

The input frequency is so high that no A/B signals can be generated or the direction can no longer be detected. The monitored frequency is different depending on whether an internal counter or the square-wave outputs A/B/Z are used. See Section 6.6.

	Masking	***Memory enable***	***STATUS register***
Bit	MFAST	LFAST	EFAST

A/B/Z errors

The signals A, B and Z are invalid. The cause is an excessive input frequency. The monitored frequency depends on the set minimum edge interval t_{pp}. This error bit will set also if the interpolation rate or the minimum edge interval t_{pp} is changed. Detection of this error has to be deactivated for using the GC-IP2000 with internal counter only (MABZ = 0).

	Masking	Memory enable	***STATUS register***
Bit	MABZ	LABZ	EABZ

6.5.3 LED pin

The LED pin can be used to signal bad sensor signals or to trigger the LED brightness control in optical encoder systems. The output pin may assume three states (VSS, VDD/2, VDD). To trigger the LED pin, the gain and offset correction values and the ADC values are used.

Default mode (LEDMODE = 0): Sensor check

The L level indicates that the values of the ADC, the gain controller or the offset controller are outside the valid range and thus that the sensor signals need to be adjusted. This state remains for at least 5 input signal periods.

Table 13 Validity ranges for the LED pin

Parameters	***Valid range***	***Register***	***Limit values***
Amplitude (ADC)	Amplitude <147.5% of the nominal amplitude	ADC_C / ADC_S	± 4,032
Offset	Offset < ± 22.5% of the nominal amplitude	CNTRLO_C / CNTRLO_S	-2,432 (Min), +2,431 (Max)
Gain	0.56 < gain < 1.44	CNTRLG_C / CNTRLG_S	128 (Min), 1,919 (Max)

Control mode (LEDMODE = 1): Brightness control

An L-level on the pin indicates that the LED is too dark. An H-level on the pin indicates that the LED is too bright. Correct input signals are indicated with a level of VDD/2 on the pin. This level is also applicable if the error cannot be detected unambiguously.

Table 14 Control mode LED

No.	***Condition***	***LED pin***
1	All gain correction values within the valid range and all ADC values within the valid range	VDD/2
2	One gain correction value (CNTRLG_C/CNTRLG_S) too large, the second too small	VDD/2
3	One gain correction value (CNTRLG_C/CNTRLG_S) too large and condition 2 not fullfilled	L
4	One gain correction value (CNTRLG_C/CNTRLG_S) too small and condition 2 not fullfilled	H
5	One ADC value (ADC_C/ADC_S) too large and condition 2 not fullfilled	H

6.6 Mode / maximum input frequency

The maximum input frequency is dependent on the selected interface at the output. If the square-wave sequences (A/B/Z) are used as the output signal, the maximum input frequency is limited by the interpolation rate and by the minimum edge interval (t_{pp}). If exclusively the internal count value is used, the maximum input frequency is determined by the clock frequency at pin XA (f_{OSZ}) . The mode **and** the monitored frequency are switched by way of the bit MABZ in the register CFG1. If both output interfaces are to be used at the same time, the bit MABZ must be initialised with "1".

Table 15 Maximum input frequency

Mode	***MABZ***	***MFAST***	***Maximum frequency for the counter***	***Maximum frequency for the ABZ output***
Counter	0	1	$f_{MAX} = f_{OSZ} / 95$	No error detection
Square-wave, $t_{pp} = N/f_{OSZ}$ **$N = 2^{CFG1\text{-}TPP(2:0)}$**	1	1	For N = 1 / CFG1-TPP(2:0) = '000' $f_{MAX} \approx 0.9 \cdot f_{OSZ} / IRATE < f_{OSZ} / 95$ For N > 1 / CFG1-TPP(2:0) ≠ '000' $f_{MAX} \approx 0.95 \cdot f_{OSZ} / IRATE < f_{OSZ} / 95$	For N = 1 / CFG1-TPP(2:0) = '000' $f_{MAX} \approx 0.9 \cdot f_{OSZ} / IRATE < f_{OSZ} / 95$ For N > 1 / CFG1-TPP(2:0) ≠ '000' $f_{MAX} \approx 0.95 \cdot f_{OSZ} / IRATE < f_{OSZ} / 95$

The limit values obtained are a maximum input frequency of 260kHz at a clock frequency of f_{OSZ} = 25MHz and a guaranteed edge interval of 128µs at a minimum clock frequency of f_{OSZ} = 1MHz. The GC-IP2000 can be matched to the subsequent electronics in the range between these two values by appropriate selection of clock frequency and edge interval. All values are valid with matched phase between the input signals and after the settling of the internal signal control. The input frequency up to this time may only amount to 50 % of the specified maximum frequency.

ⓘ *In case of activated bit LPF in register CFG1 either the maximum frequency of input signals will be limited to approx. 100KHz or the control range of amplitude will be smaller at high input frequencies.*

6.6.1 Configuring t_{pp} and f_{osz}

The GC-IP2000 is configured in accordance with the requirements of the sensor and of the subsequent electronics.

<table>
<tr><td colspan="4">ABZ output used?</td></tr>
<tr><td>no</td><td colspan="3">yes</td></tr>
<tr><td rowspan="3">CFG1-MFAST = 1
CFG1-MABZ = 0
CFG1-TPP(2:0) any value
$f_{MAX} = f_{OSZ} / 95$</td><td colspan="3">CFG1-MFAST = 1
CFG1-MABZ = 1
Condition: $t_{pp\ (counter\ at\ ABZ)} < t_{pp\ (GC\text{-}IP2000)}$</td></tr>
<tr><td colspan="3">Oscillator frequency specified?</td></tr>
<tr><td>no</td><td colspan="2">yes</td></tr>
<tr><td>CFG1-TPP(2:0) = '001'
$f_{OSZ} < 2/t_{pp\ (Counter\ at\ ABZ)}$
$t_{pp\ (GC\text{-}IP2000)} = 2/f_{OSZ}$
$f_{MAX} \approx 0.95 \cdot f_{OSZ} / (N \cdot IRATE)$
$f_{MAX} < f_{OSZ} / 95;$
$N = 2^{CFG1\text{-}TPP(2:0)}$</td><td>CFG1-TPP(2:0) = '000'
$f_{OSZ} < 1/t_{pp\ (Counter\ at\ ABZ)}$
$t_{pp\ (GC\text{-}IP2000)} = 1/f_{OSZ}$
$f_{MAX} \approx 0.90 \cdot f_{OSZ} / (N \cdot IRATE)$
$f_{MAX} < f_{OSZ} / 95;$
$N = 2^{CFG1\text{-}TPP(2:0)}$</td><td>$N = 2^{CFG1\text{-}TPP(2:0)} > t_{pp\ (counter\ at\ ABZ)} \cdot f_{OSZ}$
$t_{pp\ (GC\text{-}IP2000)} = N/f_{OSZ}$</td></tr>
</table>

Examples:

a) The minimum edge interval of the electronics connected to A, B and Z is 250ns. The interpolation rate is 1000, the maximum input frequency is 1kHz. The oscillator frequency can be selected freely.

CFG1-MFAST = 1
CFG1-MABZ = 1
CFG1-TPP(2:0) = '001'
$f_{OSZ} < 2/250$ ns, 1kHz > $0.95 \cdot f_{OSZ} / (2 \cdot 1000)$
→ 2.11MHz < f_{OSZ} < 8MHz

b) The minimum edge interval of the electronics connected to A, B and Z is 150ns. The interpolation rate is 800. The oscillator frequency is 20MHz. The maximum input frequency is determined on the basis of the specified parameters.

CFG1-MFAST = 1
CFG1-MABZ = 1
$N = 2^{CFG1\text{-}TPP(2:0)} > 150ns \cdot 20MHz \rightarrow N > 3$
→ CFG1-TPP(2:0) = '010', N=4, $f_{MAX} = 0.95 \cdot 20MHz / (4 \cdot 800)$,
→ f_{MAX} = 5.9kHz

6.7 Pins A/B/Z

The meanings of the signals at the pins A, B and Z can be modified. By default, the standard square-wave sequences offset by 90° are generated (see Section 6.2). If the internal counter of the IC is used, the mode "Controller/DSP" can be activated. Thus, it is possible to carry out equidistant measurements, to synchronise additional components with the IC and to transfer measured values to a controller IC controlled by way of interrupts. The test signals to adjust the sensor at the pins A, B and Z are provided in two further modes.

Table 16 ABZ modes

Mode	Use	Pin MODE	CFG1 / MODE	Pin A	Pin B	Pin Z
Default	Standard A/B/Z	VSS	00	Square-wave sequence A	Square-wave sequence B	Zero signal Z
Controller / DSP	Counter to the micro-controller	VDD	01	Timer/trigger interrupt nINT	Synchronous signal StartSample	Counter zero signal ZCNT
Sensor adjustment 1	Sensor adjustment	V0	10	Test signal IR4C	Test signal IR4S	Reference comparator REFCOMP
Sensor adjustment 2	Sensor adjustment	open	11	Test signal IR8C	Test signal IR16C	System deviation NDEV

6.7.1 Controller / DSP

If the measured values of the GC-IP2000 are transferred exclusively via the SPI interface, additional signals can be provided at the pins A, B and Z. The pin NERR maintains its meaning. It is designed as an open-drain pin so that the error signals of several ICs can be connected to each other.

Table 17 Additional output signals

Pin	Signal	Meaning
A	nINT	Interrupt; L-active; an active signal indicates that at least one of the trigger holding registers is occupied. A read access to the register MVAL provides the 'oldest' measured value saved in the registers. The interrupt can be triggered either by the timer or by a signal at the pin TRG. See Section 6.8.
B	StartSample	Synchronous signal; this signal delivers the sampling time of the integrated ADC. It can be used to synchronise further systems.
Z	ZCNT	Counter zero signal; this signal indicates that the internal counter of the GC-IP2000 is reset at the reference point (index point).

6.7.2 Sensor adjustment

To check and adjust the sensor, the output signals of the instrument amplifier are visible at the pins SMON and CMON. The sensor signals can be adjusted to nominal amplitude at these pins. The output signals at A, B and Z can be used for fine adjustment.

Table 18 Sensor adjustment

No.	Adjustment	Settings of the registers CFG1 / CFG2	Instruction
1	Amplitude Sine/cosine	Setting of the gain factor	Move sensor; measure on the pins SMON and CMON Adjustment until both amplitudes display approx. 2.1 V_{pp}.
2	Reference	Mode: "Sensor adjustment 1"	Measure signal REFCOMP; adjustment until the signal width corresponds to approx. one period of the sinusoidal signals
3	Offset Cosine	Mode: "Sensor adjustment 1" Deactivate Controller (Bit DISCNTRL = 1) Controller disabled; correction values in the middle of the setting range	Move sensor; measure on CMON and at signal IR4C Adjustment until mark-to-space ratio at IR4C is 50% of the period at CMON.
4	Offset Sine	Mode: "Sensor adjustment 1" Deactivate Controller (Bit DISCNTRL = 1) correction values in the middle of the setting range	Move sensor; measure on SMON and at signal IR4S Adjustment until mark-to-space ratio at IR4S is 50% of the period at SMON.
5	Phase (coarse)	Mode: "Sensor adjustment 2" Activate Controller (Bit DISCNTRL = 0)	Move sensor; measure on the pins CMON and signal IR16C, coarse adjustment of the phase until all edges on IR16C are distributed evenly within the sinusoidal period
5	Phase (fine)	Mode: "Sensor adjustment 2" Activate Controller (Bit DISCNTRL = 0)	Move sensor, measure at CMON and Signal NDEV, adjust phase until frequency at NDEV does not correlate with the frequency of the sinusoidal signal.
6	Amplitude coincidence	Mode: "Sensor adjustment 2" Deactivate Controller (Bit DISCNTRL = 1) correction values in the middle of the setting range	Move sensor, measure at CMON and signal IR8C, adjust signal amplitudes until all edges at IR8C are distributed evenly within the sinusoidal period

6.8 Measured-value trigger / timer

The current count value is written to one of the two trigger holding registers by way of a signal edge at pin TRG. The trigger edge (falling or rising) can be set using the bit TRGSLP in the register CFG1. Furthermore, a timer is integrated which can also initiate a triggering at freely programmable intervals. The respectively 'oldest' value from the trigger holding registers is provided when accessing the register MVAL for reading. If no value is saved, the current count is displayed. The trigger holding register is re-enabled after reading. The trigger source of the next value to be read (bits: TRGPIN and TRGTIM) is saved in the status register. Furthermore, the bit TRGOVL indicates whether a timer or a trigger pulse was lost. In addition, it can be detected from the bit TRG of the register MVAL whether the value was read from the timer or from the trigger. The signal nINT on pin A indicates with an L level whether or not one of the trigger holding registers is occupied. See also Section 6.7.1.

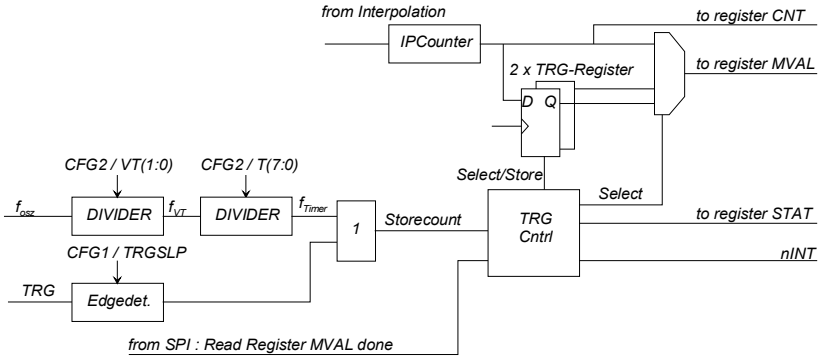


Fig. 11 Block diagramm Trigger / Timer

6.8.1 Timer

The time constant of the timer is defined using the bits T(7:0) and VT(1:0) in the register CFG2. If both T(7:0) and VT(1:0) are equal to "0", the timer is disabled. The time constant of the timer is calculated as follows:

$t_{Timer} = (T+1) / f_{VT}$ T: corresponds to T(7:0) in the register CFG2
f_{VT}: Counting frequency as per table 19

Table 19 Timer

CFG2-VT(1:0)	Counting frequency f_{VT}
00	f_{OSZ}/32
01	f_{OSZ}/512
10	f_{OSZ}/8192
11	f_{OSZ}/32768

6.8.2 Fast equidistant measurements via SPI

Table 20 Equidistant measurements

Time base	Timer	Pin TRG	SPI interface	Remark
From the GC-IP2000	Time base	For asynchronous trigger events	ASYNC mode	Reading of the measured values via SPI must be completed within the timer interval.
From the SPI interface	Inactive	For asynchronous trigger events	SYNC mode	The clock frequency at the SPI interface must be derived from the clock frequency at XA.
External	Inactive	Time base	ASYNC mode	Reading of the measured values via SPI must be completed within the measuring interval.

The diagram below shows an example for a timer-controlled equidistant measurement using the signal nINT.

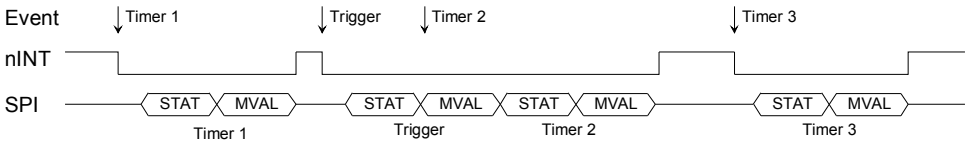


Fig. 12 Example for a timer / trigger

7 Digital interfaces

7.1 Serial interface SPI

7.1.1 Signals

The GC-IP2000 operates in the slave mode. In other words: It cannot start communication itself. Up to sixteen GC-IP2000 can be operated on a single interface bus. The interface is compatible to the most important micro-controller families. It is not compatible to the GC-IP1000 or GC-IP200!

Table 21 SPI signals

Signal	Meaning	
SCK	Clock cycle The data at MOSI is sampled by IC with the rising edge at SCK. The data at MOSI is modified by IC with the falling edge at SCK.	IN
SEN	Enable Low: Interface is enabled High: Interface is disabled, MISO becomes high-resistant or is set to nWAIT Rising edge: Command is executed.	IN
MOSI	Master OUT / slave IN Data input	IN
MISO/nWAIT	Master IN / slave OUT Data output and status signal	OUT (tristate-capable)

SPI mode: 16-bit, MSB first, SCLK default = L, sampling with rising clock signal edge. While the IC is reset or during the waiting time of a synchronous SPI read command, the MISO line is kept at L level (meaning nWAIT).

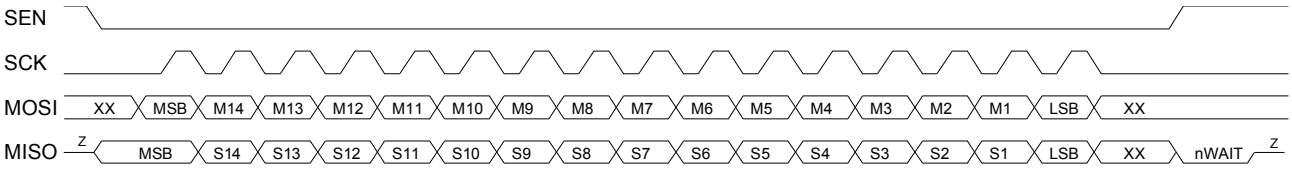


Fig. 13 SPI transfer

7.1.2 Protocol

Any data transfer is initiated by the host processor sending of an SPI word. An SPI word consists of 4 bits OP code, 4 bits hardware address and up to 8 bits data. OP codes for reading of a register result in data output at the pin MISO in the subsequent SPI access. OP codes are only accepted if the hardware address sent coincides with the hardware address of the GC-IP2000. The hardware address of the IC after a reset is '0000'. The command SETHWA (see Section 8, register CMD) can be used to read the pins HWA<3:0> into the IC as the new hardware address.

Table 22 SPI protocol

OP code	Description	Bit at signal MOSI															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		OPC				HWA				DATA							
WRA	Write address	1	0	0	nB	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	A1	A0
WRD	Write data	1	0	1	nB	H3	H2	H1	H0	D7	D6	D5	D4	D3	D2	D1	D0
RD0/ST	Read bytes 0+1 (LSB)	1	1	0	X	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	0	0
RD1	Read bytes 2+3 (MSB)	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
NOP	Output read register	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

nB:	Broadcast (L-active)	0: Command to all ICs 1: Command to the IC addressed by way of H(3:0)
H(3:0):	Hardware address	Hardware address, default: '0000', Is not evaluated if nB = 0
A(7:0):	Register address	Register address within an IC
D(7:0):	Data word	Write data (read data will appear at the pin MISO)

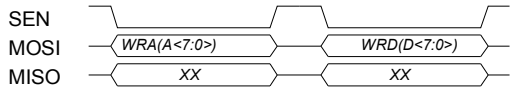
7.1.3 Register access

To write a GC-IP2000 register, first the register address must be set using the SPI word WRA. Subsequently, the register can be programmed using WRD. The register is programmed byte by byte.
Data to be read are stored into a 32-bit holding register using the SPI word RD0/ST. The data from the two least significant bytes are output on the pin MISO during the **next** SPI access (see Fig. 14). To read a 32-bit register, the commands RD0/ST, RD1 and NOP are usually executed one after another. To read several registers in succession, the sequence: RD0 – RD1 – RD0 – RD1... can be used.
The data are taken over into the holding register synchronously to the internal IC sequence. The value SYNC in the register CFG2 can be used to shift the time relative to the sampling time of the ADC. Thus, it is possible to carry out equidistant measurements with small delays. To read the registers MVAL, CNT and ADC_x, any value can be set for SYNC. The default value '00000' provides a small delay between the calculated count value and the data output at the SPI interface. To read the registers PHI, DPHI, BQ and CADC_x, a value of '00100' must be used.

The pin MISO is low during the waiting time (nWAIT). If the bit ASYNC in the register CFG2 is set, the data are stored immediately after the rising edge at the signal SEN. The time reference to the sampling of the analog signals will be lost. Thus, higher baud rates are achieved.

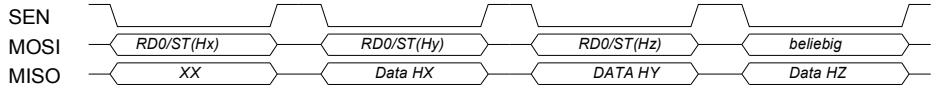
Fig.14 SPI examples

Write access 8 Bit

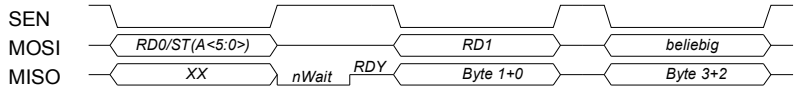


Read access 32 Bit, asynchron

Read access 16Bit, 3 IC, asynchron



Read access 32 Bit, synchron



7.1.4 Timing

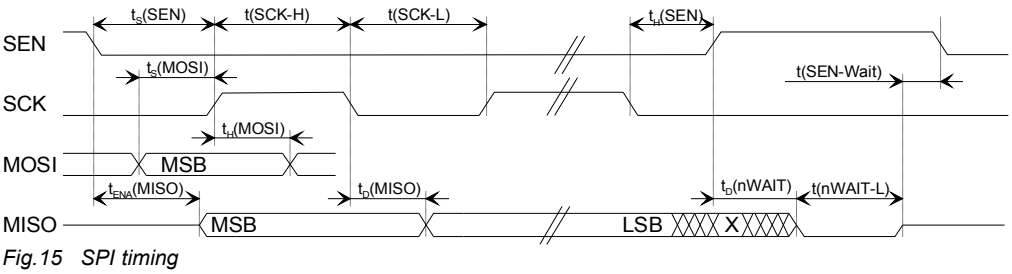


Fig.15 SPI timing

Table 23 SPI timing

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
t(SCK-H)	SPI clock, H time	20			ns
t(SCK-L)	SPI clock, L time	20			ns
t_S(SEN)	Setup time SEN falling before SCK rising	20			ns
t_H(SEN)	Hold time SEN rising after SCK falling	20			ns
t_s(MOSI)	Setup time MOSI rising before SCK	5			ns
t_H(MOSI)	Hold time MOSI rising after SCK	5			ns
t_D(MISO)	Delay time SCK falling until MISO	0	10	15	ns
t_{ENA}(MISO) [1]	Delay time SEN falling until MISO is active	0	10	15	ns
t_D(nWAIT)	Delay time SEN rising until nWAIT is active	0	60	70	ns
t(nWAIT-L)	Waiting time rising after SEN	$2/f_{OSZ}$		$4/f_{OSZ}$ + 20	ns
	Waiting time rising after SEN (synchronous reading)	$2/f_{OSZ}$		$36/f_{OSZ}$ + 20	ns
t(SEN-Wait)	Time between wait state and next access	0			ns

[1] For non-read commands, the pin MISO may remain in the tri-state state (inactive).

7.2 EEPROM

All configuration data and controller values can be written to an EEPROM. If no EEPROM is connected, the IC will use the values set on the configuration pins. After reset, a test is performed to determine whether the EEPROM is connected; if necessary, it is read out. Writing to the EEPROM is always performed via the SPI interface. For this reason, it is imperative to operate the IC with the SPI interface once to adapt measuring system and GC-IP2000. The address allocation in the EEPROM corresponds to the addressing via SPI (write accesses). **A valid EEPROM must contain the identifier 0x99 at address 0x00.**

EEPROM with Microwire interface, type *93C56*, are supported in the 8-bit mode. Examples for this EEPROM type are the AT93C56A from ATMEL, the 93LC56 from Microchip or the M93C56 from ST. Where necessary, access to any memory cells of the EEPROM is possible via the SPI interface. To this end, start the following sequence:

Table 24 Accessing the EEPROM

EEPROM	Step 1	Step 2	Step 3	Step 4	Step 5
Re-reading of the GC-IP2000 configuration from the EEPROM	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Set the bit **RCFG** in the register CMD.	Check the BSY bits in the register EEPSTAT; if necessary, wait.		
Writing the GC-IP2000 configuration to the EEPROM	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write the EEP OPCode **EWEN**(0x3) to the register EEPOPC	Set the bit **WCFG** in the register CMD.	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write the EEP OPCode **EWDS**(0x0) to the register EEPOPC
Reading the memory cell	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write address to register **EEPADR**	Write the EEP OPCode **READ** (0x8) to the register EEPOPC	Check the bit EEPBSY in the register EEPSTAT; if necessary, wait.	Read from register **EEPDAT**
Activating the EEPROM write and erase commands	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write the EEP OPCode **EWEN**(0x3) to the register EEPOPC			
Deactivating the EEPROM write and erase commands	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write the EEP OPCode **EWDS**(0x0) to the register EEPOPC			
Writing a memory cell [1]	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write address to register **EEPADR**	Write data to the register **EEPDAT**	Write the EEP OPCode **WRITE** (0x4) to the register EEPOPC	Wait during the programming time of the EEPROM
Erasing a memory cell [1]	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write address to register **EEPADR**	Write the EEP OPCode **ERASE** (0xC) to the register EEPOPC	Wait during the erase time of the EEPROM	
Writing all memory cells [1] [2]	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write data to the register **EEPDAT**	Write the EEP-OP code **WRAL** (0x1) to the register EEPOPC	Wait during the programming time of the EEPROM	
Erasing all memory cells [1] [2]	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write the EEP-OP code **ERAL** (0x2) to the register EEPOPC	Wait during the erase time of the EEPROM		
Marking EEPPROM as IP2000 EEPROM [1]	Check the BSY bits in the register EEPSTAT; if necessary, wait.	Write **address 0x00** to register **EEPADR**	Write **data 0x99** to the register **EEPDAT**	Write the EEP-OP code **WRITE** (0x4) to the register EEPOPC	Wait during the programming time of the EEPROM

[1] The write and erase commands should already have been activated using EWEN.
[2] The operating voltage VDD on the EEPROM and the voltage VDDIO must be 5V.

8 Description of registers

Address	Meaning	Byte 3	Byte 2	Byte 1	Byte 0
0x00	Measured value / trigger value	MVAL			
0x04	Count value	CNT			
0x08	Status / command	CMD	ID/REV	STAT / ERROR	
0x0C	Configuration 1	CFG1_H		CFG1_L	
0x10	Configuration 2	CFG2			
0x14	Controller: Gain correction value	CNTRLG_S		CNTRLG_C	
0x18	Controller: Offset correction value	CNTRLO_S		CNTRLO_C	
0x1C	Reserved			RSV	
0x20	EEPROM		EEPOPC	EEPADR / EEPSTAT	EEPDAT
0x24	ADC values	ADC_S		ADC_C	
0x28	Corrected ADC values	CADC_S		CADC_C	
0x2C	Interpolation result 1	DPHI		PHI	
0x30	Interpolation result 2	BQ		PHI	

The highlighted registers are read from the EEPROM after reset. The registers marked blue are set beforehand using the Config pins.

ID/REV ***ASIC identifier***

Address for reading: 0x08 Address for writing: -

31	30	29	28	27	26	25	24	23 22 21 20	19 18 17 16
-	-	-	-	-	-	-	-	ASICID	ASICREV

Bit	Name	Reset value	Format	Value	Meaning
23-20	ASICID	1001	Binary	1001	The IC is a GC-IP2000.
19-16	ASICREV	0011	Binary		Silicon revision of the IC

RSV ***Reserved for the IC manufacturer***

Address for reading: 0x1C Address for writing: 0x1C (bits 7-0)
0x1D (bits 15-8)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	LEDSP	LED1	LED0	-	-	ZZSP	ZZ2	ZZ1	ZZ0	-	-

This register is reserved for the IC manufacturer. It **must** be initialised with 0x0000.

MVAL ***Measured value / trigger value***

Address for reading: 0x00 Address for writing: -

31:2	1	0
CNT/TVAL	TRG	ERR

Bit	Name	Reset value	Format	Value	Meaning
31-2	CNT/TRG	0x0000	Signed		Measured value; value corresponds to count value or contents of a trigger holding register; See Section 6.8
1	TRG	0	Bit	0 1	Measured value corresponds to current count value Measured value corresponds to contents of a trigger holding register
0	ERR	0	Bit	0 1	Measured value is valid An error has occurred. The current measured value and all subsequent values are to be discarded. After rectification of the error cause and resetting of the error bits (SPI command: RESCNT), it is imperative to pass through the reference point to be able to perform further absolute measurements. See Section 6.5.2.

CNT ***Count value***

Address for reading: 0x04 Address for writing: -

31:2	1	0
CNT	ZSTAT	ERR

Bit	Name	Reset value	Format	Value	Meaning
31-2	CNT	0x0000	Signed		Count value
1	ZSTAT	0	Bit	0 1	The reference mark (index) of the scale has not yet been passed or the reference of count value and reference mark was lost due to an error. The reference mark (index) of the scale has been passed; GC-IP2000 and scale operate synchronously.
0	ERR	0	Bit	0 1	Measured value is valid An error has occurred. The current measured value and all subsequent values are to be discarded. After rectification of the error cause and resetting of the error bits (SPI command: RESCNT), it is imperative to pass through the reference point to be able to perform further absolute measurements. See Section 6.5.2.

STAT / ERROR ***Status***

Address for reading: 0x08 Address for writing: -

15	14:13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	LEDPIN	ZSTAT	TRGOVL	TRGTIM	TRGPIN	ESOFF	ECOFF	ESGAIN	ECGAIN	EABZ	EFAST	ESADC	ECADC	EVLOW

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
14-13	LEDPIN	00	Binary	00 01 1x	The pin LED is at L level. The pin LED is at H level. The pin LED is at VDD/2 level.
12	ZSTAT	0	Bit	0 1	The reference mark (index) of the scale has not yet been passed or the reference of count value and refence mark was lost due to an error. The reference mark (index) of the scale has been passed; GC-IP2000 and scale operate synchronously.
11	TRGOVL	0	Bit	0 1	No overflow of the trigger holding register Overflow of the trigger holding register; Trigger or timer event was lost
10	TRGTIM	0	Bit	0 1	Next measured value read at address 0x00 was not triggered by the timer Next measured value read at address 0x00 was triggered by the timer
9	TRGPIN	0	Bit	0 1	Next measured value read at address 0x00 was not triggered by pin TRG Next measured value read at address 0x00 was triggered by pin TRG
8	ESOFF	0	Bit	0 1	No offset error at sinusoidal signal The offset controller for the sinusoidal signal has reached its limit. The cause is an excessive signal offset, a partly or fully disconnected sensor or an invalid value for initialisation of the controller.
7	ECOFF	0	Bit	0 1	No offset error at cosinusoidal signal The offset controller for the cosinusoidal signal has reached its limit. The cause is an excessive signal offset, a partly or fully disconnected sensor or an invalid value for initialisation of the controller.
6	ESGAIN	0	Bit	0 1	No amplitude error at sinusoidal signal The gain controller for the sinusoidal signal has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.
5	ECGAIN	0	Bit	0 1	No amplitude error at cosinusoidal signal The gain controller for the cosinusoidal signal has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.
4	EABZ	0	Bit	0 1	No error at A/B/Z The signals A, B and Z are invalid. The cause is an excessive input frequency. The monitored frequency depends on the set minimum edge interval t_{pp}. This error also occurs if the interpolation rate or the minimum edge interval is changed. Detection of this error is deactivated for the counter mode.
3	EFAST	0	Bit	0 1	No speed error The input frequency is so high that no A/B signals can be generated or the direction can no longer be detected. The monitored frequency is different depending on whether an internal counter or the square-wave outputs A/B/Z are used.
2	ESADC	0	Bit	0 1	No ADC error at the sinusoidal signal The A/D converter for the sinusoidal signal is overdriven. The cause is that the signal amplitude is too high. This error may also occur with signals with very large offset at simultaneously high amplitude.
1	ECADC	0	Bit	0 1	No ADC error at the cosinusoidal signal The A/D converter for the cosinusoidal signal is overdriven. The cause is that the signal amplitude is too high. This error may also occur with signals with very large offset at simultaneously high amplitude.
0	EVLOW	0	Bit	0 1	No vector error The signal vector generated from the sinusoidal and cosinusoidal signals is too small. Usually, the cause is a partly or completely disconnected sensor. This error may also occur with signals with very large offset at simultaneously low amplitude.

CMD ***Command***

Address for reading: - Adress for writing: 0x0B

7	6	5	4	3	2	1	0
-	-	SETHWA	WCFG	RCFG	CLRZ	RESCTL	RESCNT

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
5	SETHWA			0 1	The command SETHWA is not executed. The pins HWA3, HWA2, HWA1 and HWA0 are read into the IC as hardware addresses. If several ICs are to be connected to one SPI interface, this command **must** be sent first to all connected ICs. See Section 7.1.2.
4	WCFG			0 1	The command WCFG is not executed. The contents of the registers CFG1, CFG2, CNTRLG_S, CNTRLG_C, CNTRLO_S, CNTRLO_C and RSV are transferred to the EEPROM. More important notes are shown in Section 7.2.
3	RCFG			0 1	The command RCFG is not executed. The contents of the registers CFG1, CFG2, CNTRLG_S, CNTRLG_C, CNTRLO_S, CNTRLO_C and RSV are read from the EEPROM.
2	CLRZ			0 1	The command CLRZ is not executed. The status bit ZSTAT is reset.
1	RESCTL			0 1	The command RESCTL is not executed. The internal controller for gain and offset is reset, i.e. all correction values for offset and gain are set to the centre of their range of values.
0	RESCNT			0 1	The command RESCNT is not executed. The count value is set to "0", all error flags in the status register are reset, and the status bit ZSTAT is also reset.

CFG1 ***Configuration 1***

Address for reading: 0x0C

Address for writing: 0x0C (bits 7-0)
0x0D (bits 15-8)
0x0E (bits 23-16)
0x0F (bits 31-24)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	LPF	LOFF	LGAIN	LABZ	LFAST	LADC	LVLOW	LEDMODE	HLD	MOFF	MGAIN	MABZ	MFAST	MADC	MVLOW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAIN1	GAIN0	TRGSLP	DHE	RSV	TPP2	TPP1	TPP0	MODE1	MODE0	DISZ	Z4	IR3	IR2	IR1	IR0

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
30	LPF	0	Bit	0 1	Noise filter inactive Noise filter active; maximum input frequency is limited
29	LOFF	0	Bit	0 1	Detected offset errors (ESOFF/ ECOFF) are not saved. Detected offset errors (ESOFF/ ECOFF) are saved.
28	LGAIN	0	Bit	0 1	Detected gain errors (ESGAIN/ECGAIN) are not saved. Detected gain errors (ESGAIN/ECGAIN) are saved.
27	LABZ	0	Bit	0 1	Detected A/B/Z errors (EABZ) are not saved. Detected A/B/Z errors (EABZ) are saved.
26	LFAST	0	Bit	0 1	Detected speed errors (EFAST) are not saved. Detected speed errors (EFAST) are saved.
25	LADC	0	Bit	0 1	Detected ADC errors (ESADC/ECADC) are not saved. Detected ADC errors (ESADC/ECADC) are saved.
24	LVLOW	0	Bit	0 1	Detected vector errors (LVLOW) are not saved. Detected vector errors (LVLOW) are saved.
23	LEDMODE	0	Bit	0 1	L level at pin LED indicates that the signals at the sensor need to be adjusted. The pin LED operates in the "Control" mode; See Section 6.5.3.
22	HLD	1	Bit	0 1	The behaviour of the signals A,B and Z is not defined in case of error. The signals A,B and Z do not change in case of error; the level is maintained.
21	MOFF	1	Bit	0 1	The detection of offset errors (ESOFF/ ECOFF) is deactivated. The detection of offset errors (ESOFF/ ECOFF) is activated.
20	MGAIN	1	Bit	0 1	The detection of gain errors (ESGAIN/ECGAIN) is deactivated. The detection of gain errors (ESGAIN/ECGAIN) is activated.
19	MABZ	1	Bit	0 1	The detection of A/B/Z errors (EABZ) is deactivated; the IC operates in the counter mode. The detection of A/B/Z errors (EABZ) is activated; the IC operates in the square-wave mode.
18	MFAST	1	Bit	0 1	The detection of speed errors (EFAST) is deactivated. The detection of speed errors (EFAST) is activated.
17	MADC	1	Bit	0 1	The detection of ADC errors (ESADC/ECADC) is deactivated. The detection of ADC errors (ESADC/ECADC) is activated.
16	MVLOW	1	Bit	0 1	The detection of vector errors (EVLOW) is deactivated. The detection of vector errors (EVLOW) is activated.
15-14	GAIN1-0	Pin CFGGAIN	Binary		Configuration of the signal amplitude as per table 8
13	TRGSLP	0	Bit	0 1	A falling edge at pin TRG accepts the measured value into the trigger holding register A rising edge at pin TRG accepts the measured value into the trigger holding register
12	DHE	Pin CFGFILT	Bit	0 1	Digital hysteresis is deactivated Digital hysteresis is activated
11	RSV	Pin CFGFILT	Bit	0 1	Default value Don't use this configuration
10	TPP2	0	Binary		Configuration of the minimum edge interval t_{pp} as per table 9
9-8	TPP1-0	Pin CFGTPP			
7-6	MODE	Pin mode	Binary		Configuration of the outputs A, B and Z as per table 16
5	DISZ	0	Bit	0 1	Reference-point processing is activated Reference-point processing is deactivated
4	Z4	Pin Z4/IRBIN	Bit	0 1	The width of the zero signal Z is one increment = ¼ period. The width of the zero signal Z is four increments = 1 period.
3	IR3	Pin Z4/IRBIN	Binary		Configuration of the interpolation rate as per table 4
2	IR2	Pin IR2			
1	IR1	Pin IR1			
0	IR0	Pin IR0			

ⓘ *For the counter mode, it is recommended to activate saving of all signal errors. To this end, set the bits MVLOW, MADC, MFAST, MGAIN, MOFF, LVLOW, LADC, LFAST, LGAIN and LOFF to "1". The bit MABZ must be 0. See also Sections 6.5.2 and 6.6.*

ⓘ *For square-wave mode (A/B/Z), it is recommended to activate detection of all signal errors, but to deactivate saving. To this end, set the bits MVLOW, MADC, MFAST, MGAIN, MOFF and MABZ to "1". LVLOW, LADC, LFAST, LGAIN, LOFF and LABZ are "0". See also Sections 6.5.2 and 6.6.*

ⓘ *For activated noise filter (bit LPF) the maximum input frequency will be limited. For using the IC with a nominal value of amplitude of 75mV$_{pp}$, that is Gain(1:0) = '11', Bit LPF **must** be '1'.*

CFG2 *Configuration 2*

Address for reading: 0x10

Address for writing: 0x10 (bits 7-0)
0x11 (bits 15-8)
0x12 (bits 23-16)
0x13 (bits 31-24)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	PHBER	PH5	PH4	PH3	PH2	PH1	PH0	-	-	-	OFFSCTL	OFFSCTL	GAINCTL	GAINCTL	DISCTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	VT1	VT0	T7	T6	T5	T4	T3	T2	T1	T0

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
30	PHBER	0	Bit	0 1	The setting range of the phase correction potentiometer is ± 5°. The step size is 0.250° The setting range of the phase correction potentiometer is ± 10°. The step size is 0.500°
29-24	PH5-0	000000	Signed	PH -20 +20	Setting value of the phase correction potentiometer Largest phase displacement negative Largest phase displacement positive
20-19	OFFSCTL	00	Binary	00 01 10 11	Default value for the settling time of the offset controller. This configuration must be selected if the sensor signal has a lower input frequency or is overlaid by noise, or the phase between sinusoidal and cosinusoidal signals cannot be fully adjusted using the phase correction potentiometer. Reduction of the settling time of the offset controller by a factor of approx. 2 Reduction of the settling time of the offset controller by a factor of approx. 4 Reduction of the settling time of the offset controller by a factor of approx. 8
18-17	GAINCTL	00	Binary	00 01 10 11	Default value for the settling time of the gain controller. This configuration must be selected if the sensor signal has a lower input frequency or is overlaid by noise, or the phase between sinusoidal and cosinusoidal signals cannot be fully adjusted using the phase correction potentiometer. Reduction of the settling time of the gain controller by a factor of approx. 2 Reduction of the settling time of the gain controller by a factor of approx. 4 Reduction of the settling time of the gain controller by a factor of approx. 8
16	DISCTL	0	Bit	0 1	The internal controller for gain and offset is activated. The internal controller for gain and offset is deactivated.
15	ASYNC	0	Bit	0 1	The data to be read are accepted into a 32-bit holding register synchronously to the internal sequence using the SPI word RD0/ST. The time of acceptance can be shifted relative to the sampling time using the value of SYNC. Data to be read are accepted asynchronously into a 32-bit holding register using the SPI word RD0/ST. The value of SYNC is not evaluated.
14-10	SYNC4-0	00000	Unsigned		Displacement of an SPI read access relative to the sampling time. To read the registers MVAL, CNT and ADC_x, any value can be set. The default value '00000' provides a small delay between the calculated count value and the data output at the SPI interface. To read the registers PHI, DPHI, BQ and CADC_x, a value of '00100' must be used.
9-8	VT1-0	00	Binary		Configuration of the time constant for the timer. $t_{Timer} = (T+ 1) / f_{VT}$; f_{VT} as per table 19. If both VT and T are equal to "0", the timer is deactivated. See Section 6.8.1.
7-0	T7-0	0x00	Unsigned		Configuration of the time constant for the timer. $t_{Timer} = (T+ 1) / f_{VT}$; f_{VT} as per table 19. If both VT and T are equal to "0", the timer is deactivated. See Section 6.8.1.

CNTRLG *Controller: Gain correction value*

Address for reading: 0x14

Address for writing: 0x14 (bits 7-0)
0x15 (bits 15-8)
0x16 (bits 23-16)
0x17 (bits 31-24)

When writing the bits 26-16, the bits 23-16 must be written first to address 0x16. Subsequently, the whole correction value is refreshed in the register by writing of the bits 26-24 to address 0x17.

When writing the bits 10-0, the bits 7-0 must be written first to address 0x14. Subsequently, the whole correction value is refreshed in the register by writing of the bits 10-8 to address 0x15.

Please note that the correction values are changed automatically by the IC with active signal control.

31	30	29	28	27	26:16
-	-	-	-	-	CNTRLG_S

15	14	13	12	11	10:0
-	-	-	-	-	CNTRLG_C

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
26-16	CNTRLG_S	0x400	Unsigned	CNTRLG	CADC_S = [2·ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048) CADC_C = [2·ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048)
10-0	CNTRLG_C	0x400	Unsigned	0x000	Minimum value; the offset-corrected ADC values of the sinusoidal signal are multiplied by 0.5.
				0x400	Mean value; the offset-corrected ADC values of the sinusoidal signal are multiplied by 1.0.
				0x7FF	Maximum value; the offset-corrected ADC values of the sinusoidal signal are multiplied by 1.5.

CNTRLO ***Controller: Offset correction value***

Address for reading: 0x18 Address for writing: 0x18 (bits 7-0)
0x19 (bits 15-8)
0x1A (bits 23-16)
0x1B (bits 31-24)

When writing the bits 28-16, the bits 23-16 must be written first to address 0x1A. Subsequently, the whole correction value is refreshed in the register by writing of the bits 28-24 to address 0x1B. If the value to be written lies outside the valid range of -2730...+2729, the correction register is no longer refreshed, and the bit ESOFF in the register STAT/ERR is set. When writing the registers, it is imperative that all 28 bits are always transferred in the specified order.

When writing the bits 12-0, the bits 7-0 must be written first to address 0x18. Subsequently, the whole correction value is refreshed in the register by writing of the bits 12-8 to address 0x19. If the value to be written lies outside the valid range of -2730...+2729, the correction register is no longer refreshed, and the bit ECOFF in the register STAT/ERR is set. When writing the registers, it is imperative that all 28 bits are always transferred in the specified order.

Please note that the correction values are changed automatically by the IC with active signal control.

31	30	29	28:16
-	-	-	CNTRLO_S

15	14	13	12:0
-	-	-	CNTRLO_C

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
28-16	CNTRLO_S	0x0000	Signed	CNTRLO	CADC_S = [2·ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048) CADC_C = [2·ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048)
12-0	CNTRLO_C	0x0000	Signed	0x1556 0x0000 0x0AA9	Minimum value -2730 Mean value 0; no offset correction Maximum value +2729

ADC ***ADC value***

Address for reading: 0x24 Address for writing: -

31:16
ADC_S

15:0
ADC_C

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
31-16	ADC_S		Signed	0xF000 0x0000	Minimum value -4096; corresponds to a differential voltage of approx. -750mV at the input of the instrument amplifier Mean value 0; corresponds to a differential voltage of approx. 0mV at the input of the instrument amplifier
15-0	ADC_C		Signed	0x0FFF	Maximum value +4095; corresponds to a differential voltage of approx. +750mV at the input of the instrument amplifier

CADC ***Corrected ADC value***

Address for reading: 0x28 Address for writing: -

31	30	29:16
VZ(CADC_S)	0	Abs(CADC_S)

15	14	13:0
VZ(CADC_C)	0	Abs(CADC_C)

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
31	VZ(CADC_S)		Bit	0 1	Corrected ADC value, sinusoidal ≥ 0 Corrected ADC value, sinusoidal < 0
29 -16	Abs(CADC_S)		Unsigned	0 0x3FFF	Corrected ADC value sinusoidal (absolute value) Minimum value Maximum value
15	VZ(CADC_C)		Bit	0 1	Corrected ADC value, cosinusoidal ≥ 0 Corrected ADC value, cosinusoidal < 0
13-0	Abs(CADC_C)		Unsigned	0 0x3FFF	Corrected ADC value cosinusoidal (absolute value) Minimum value Maximum value
31-16	CADC_S		Sign + Absolute value		Corrected ADC value, sinusoidal CADC_S = [2·ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048)
15:0	CADC_C		Sign + Absolute value		Corrected ADC value, cosinusoidal CADC_C = [2·ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048)

PHI Angular value

Address for reading: 0x2C or 0x30 Address for writing: -

15:0
PHI

Bit	Name	Reset value	Format	Value	Meaning
15-0	PHI		Unsigned	0x0000 Maximum	The phase angle of sinusoidal and cosinusoidal signals is 0°. The phase angle of sinusoidal and cosinusoidal signals is 360° - ε. The maximum value is dependent on the set interpolation rate. Maximum value 2047 for the interpolation rates 2048,1024, 512, 256 and 128. Maximum value 1999 for the interpolation rates 2000,1000 and 500 Maximum value 1599 for the interpolation rates 1600, 800, 400, 200 and 100.

DPHI Angle difference

Address for reading: 0x2C Address for writing: -

31:16
DPHI

Bit	Name	Reset value	Format	Value	Meaning
31-16	DPHI		Signed	DPHI	The value DPHI is the difference in the phase angle of sinusoidal and cosinusoidal signals between two samplings. The range of values is dependent on the set interpolation rate. -759 ≤ DPHI < 759 for the interpolation rates **2048** (IRATE0),1024, 512, 256 and 128 -741 ≤ DPHI < 741 for the interpolation rates **2000** (IRATE0), 1000 and 500 -593 ≤ DPHI < 593 for the interpolation rates **1600** (IRATE0),800, 400, 200 and 100 $DPHI = 32 \cdot IRATE0 \cdot f_{Input}/f_{OSZ}$

BQ Controller value

Address for reading: 0x30 Address for writing: -

31:16
BQ

Bit	Name	Reset value	Format	Value	Meaning
31-16	BQ		Unsigned	BQ	The value BQ contains the deviation of the gain and offset controller from the setpoint. If offset and gain are adjusted completely, the value of this register is 321.

EEPDAT EEPROM data

Address for reading: 0x20 Address for writing: 0x20

7:0
EEPDAT

Bit	Name	Reset value	Format	Value	Meaning
7-0	EEPDAT	0x00	Binary		EEPROM data. To program the EEPROM, the data must be written to this register before activating the OP code. Once the EEPROM has been read, this register will receive the EEPROM data. The register must not be written if one of the BSY bits in the register EEPSTAT is active.

EEPADR EEPROM address

Address for reading: -- Adress for writing: 0x21

7:0
EEPADR

Bit	Name	Reset value	Format	Value	Meaning
7-0	EEPADR	0x00	Binary		EEPROM address. To program or read the EEPROM, the address must be written to this register before activating the OPCode. The register must not be written if one of the BSY bits in the register EEPSTAT is active.

EEPOPC EEPROM OPCode

Address for reading: - Adress for writing: 0x22

EEP OPCode Writing to this register triggers an EEPROM access. The register must not be written if one of the BSY bits in the register EEPSTAT is active.

7	6	5	4	3:0
–	–	–	–	EEPOPC

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
3-0	EEPOPC	0000	Binär	0x8 (READ) 0x4 (WRITE) 0xC (ERASE) 0x3 (EWEN) 0x0 (EWDS) 0x2 (ERAL) 0x1 (WRAL)	Read the memory cell Write to the memory cell Erase the memory cell Permit write and erase commands Forbid write and erase commands Erase all memory cells; VDD at EEPROM and VDDIO must be 5V Write to all memory cells; VDD at EEPROM and VDDIO must be 5V

EEPSTAT EEPROM status

Address for reading: 0x20 Address for writing: -

15	14	13	12	11	10	9	8
–	–	–	–	EEPBSY	WCFGBSY	RCFGBSY	EEPEXIST

Bit	*Name*	*Reset value*	*Format*	*Value*	*Meaning*
11	EEPBSY	0	Bit	0 1	No EEPROM access active EEPROM access active. No further command may be sent to the EEPROM. Note: Write and erase accesses to the EEPROM require additional waiting time; please refer to the data sheet of the EEPROM. The status bit `EEPBSY` merely indicates that a command is being transferred to the EEPROM.
10	WCFGBSY	0	Bit	0 1	The command `WCFG` is not being executed. The command `WCFG` is being executed. No further command may be sent to the EEPROM.
9	RCFGBSY	0	Bit	0 1	The command `RCFG` is not being executed. The command `RCFG` is being executed. No further command may be sent to the EEPROM.
8	EEPEXIST	0	Bit	0 1	No EEPROM with the identifier 0x99 was found. An EEPROM with the identifier 0x99 was found.

9 Characteristic Values

Table 25 Absolute maximum ratings

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Analog supply voltage			7.0 [1)]	V
VDD	Digital supply voltage / oscillator			7.0 [1)]	V
VDDIO	Supply voltage, digital I/Os			7.0 [1)]	V
TJ	Operating temperature	-40		125	°C
TS	Storage temperature	-55		150	°C
V(AIN)	Voltage at the analog inputs [NRES, XA, XB, SINP, SINN, COSP, COSN, REFP, REFN]	-0.3		VDDA+0.3	V
V(DIN)	Voltage at the digital inputs [MOSI, SEN, SCK, EDO, TRG, IR(2:0), TM]	-0.3		VDDIO+0.3	V
V(CFG)	Voltage at the configuration inputs [Z4, CFGTPP, CFGFILT, CFGGAIN, MODE]	-0.3		VDDA+0.3	V
ESD	ESD sensitivity (HBM)			2	kV

[1)] t < 250ms, T < 60°C

Table 26 Operating conditions

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Analog supply voltage	4.75 (4.5) [1)]	5.0	5.5	V
VDD	Digital supply voltage / oscillator	4.5	5.0	5.5	V
VDDIO	Supply voltage, digital I/Os	3.0 / 4.5	3.3 / 5.0	3.6 / 5.5	V
I(VDDA)	Current consumption, analog		50	65	mA
I(VDD)	Current consumption, digital		30	35	mA
T	Operating temperature	-40		125	°C

[1)] The control ranges and the interpolation accuracy are limited between 4.5V and 4.75V.

Table 27 Characteristic values of the oscillator

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
FOSZ	Internal clock frequency (CLKI): Frequency	1		25	MHz
VOSZ	External oscillator: Level [XA]	LVCMOS	CMOS	VDD	V
FOSZ(QA)	Internal quartz oscillator: Frequency	1		15	MHz
Z(XA)	Pin XA: impedance (R to VDD, C to VSS)	3.1k | 4pF	4.5k | 4pF	7.5k | 4pF	
VILXA (max)	Pin XA: input voltage L (max)	1.9	2.2		V
VIHXA (min)	Pin XA: input voltage H (min)		2.5	2.9	V
TH/TL	Mark-to-space ratio	40	50	60	%

Table 28 Analog characteristic values

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
Z(AIN)	Input impedance		1GΩ||8pF		
Gain	Gain (as per table 8) @ 1kHz	97	100	103	%
fg	Limit frequency (attenuation 1dB) @ CFG1/LPF = 0		700		kHz
fg(LPF)	Limit frequency (attenuation 1dB) @ CFG1/LPF = 1		100		kHz
CMIR	Common-mode input voltage	0.5	VDDA/2	3.7	V
CMRR	Common-mode rejection ratio (@ f < 1kHz, CFG1/GAIN = 11)	50			dB
V(V0)	Voltage on pin V0/ DC-Voltage on pin SMON/CMON	2.19	2.25	2.31	V
VMON	AC-Voltage on pin SMON/CMON @ nominal amplitude		2.1		V_{pp}
VTH(REFL)	Lower switching point of the reference-point comparator		-1.8		%VINNOM[1)]
VTH(REFH)	Upper switching point of the reference-point comparator		+4.3		%VINNOM[1)]
I(V0)	Output current on pin V0			0.8	mA
CL(V0)	Capacitive load on pin V0			300	pF
I(OUTX)	Output current on pin SMON/CMON			0.05	mA
CL(OUTX)	Capacitive load on pin SMON/CMON			50	pF
φK1	Phase correction in range 1	4.5	5	5.5	°
φK2	Phase correction in range 2	9	10	11	°

[1)] Nominal value of the difference voltage of SINP-SINN or COSP-COSN

Table 29 Digital characteristic values

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VOH	Output voltage H [ECK, EDI, ECS, MISO, A, B, Z, LED]	80			%VDDIO
VOL	Output voltage L [ECK, EDI, ECS, MISO, A, B, Z, NERR, LED]			0.4	V
VO3	Output voltage in state 3 [LED]		VDDA/2		V
VIH	Input voltage H [MOSI, SEN, SCK, EDO, TRG, IR(2:0), TM]	2.0		VDDIO	V
VIL	Input voltage L [MOSI, SEN, SCK, EDO, TRG, IR(2:0), TM]			0.8	V
I(DIG)	Output current, digital @VDDIO=5V (3.3V) [ECS, ECK, EDI, A, B, Z, NERR]			4 (2)	mA
I(MISO)	Output current, digital @VDDIO=5V (3.3V) [MISO]			8 (4)	mA
I(DIGLED)	Output current, digital [LED]			1	mA
VTH(L-O)	Threshold voltage L / open [Z4, CFGTPP, CFGFILT, CFGGAIN, MODE]	7	10	13	%VDDA
VTH(O-V0)	Threshold voltage L / V0 [Z4, CFGTPP, CFGFILT, CFGGAIN, MODE]	33	36	39	%VDDA
VTH(V0-H)	Threshold voltage V0 / H [Z4, CFGTPP, CFGFILT, CFGGAIN, MODE]	81	84	87	%VDDA
V(CFGO)	Terminal voltage if open [Z4, CFGTPP, CFGFILT, CFGGAIN, MODE]	1.10	1.15	1.20	V

Table 30 Characteristic values for interpolation

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{IP}	Input frequency	0		260	kHz
IRATE	Interpolation rate	100		2000	Increments
	Amplitude control	60		120	%VINNOM
	Offset control	-10		10	%VINNOM
EABS	Absolute angle error [1)]		±0.7	±1	Increments
EDIFF	Differential angle error [1)]		±0.4		Increments
tpp	Minimum edge interval A/B/Z	$1/f_{OSZ}$		$128/f_{OSZ}$	ns
t(TRG)	Pulse width of the trigger signal	$3/f_{OSZ}$			ns
td(CNT)	Delay time 'Analog input to counter'	$125/f_{OSZ}$ + 50		$157/f_{OSZ}$ +200	ns
td(ABZ)	Delay time 'Analog input to A/B/Z'	$155/f_{OSZ}$ + 50		$187/f_{OSZ}$ +200	ns

[1)] Clock provided from external oscillator, input voltage range $1V_{pp}$

10 Application Notes

10.1 Application circuit

10.1.1 General notes

- It is imperative to connect defined circuits to the IC inputs.
- All block capacitors (refer table below) are to be connected closely to the pad.
- Connections to VSSA and VSS/VSSIO resp. must be designed as ground areas
- The ground areas for VSSA and VSS/VSSIO must be connected at one point of the PCB.
- The voltage at the digital inputs must not exceed the voltage at VDDIO.
- If a configuration input with 4-value logic remains open, the length of the line on this pin must be ≤ 10cm; otherwise, an additional capacitor of 1nF is to be connected directly at the IC pin.
- Pull-up resistors are required at the pins NRES, NERR and MISO.
- For using the SPI with high data rates, series resistors of 22...33Ω each at MOSI, MISO, SCK and SEN are useful.
- The digital outputs A, B and Z are designed with a maximum load of 4mA (at VDDIO=5V). An external driver-IC is necessary to realize a differential RS422-interface.

10.1.2 Overview

Table 31 Connection of GC-IP2000

Pins	Power domain	I/O	Connection	Connection if unused
2 x VSS		Power	Ground digital	
Exposed Pad		Package	DVSS	DVSS
2 x VSSA		Power	Ground analog	
VSSIO		Power	Ground digital-IO	
VDD	VDD	Power	+5V digital Block capacitor 100nF against VSS	
VDDA	VDDA	Power	+5V analog Block capacitor 100nF against VSSA	
VDDIO	VDDIO	Power	+5V digital or +3.3V digital Block capacitor 100nF against VSSIO	
VPROG	VPROG	Power	Connect to VDD Block capacitor 100nF against VSS	
XA/CLK, XB	VDD	Clock	a) Quartz between XA and XB b) Oscillator-IC to XA, XB to VSS	XB to VSS
RS25, RC25	VDDA	Power	Block capacitor 10nF against VSSA	
RSL, RSH	VDDA	Power	Capacitor 10nF between RSL and RSH Block capacitor 1µF against VSSA each	
RCL, RCH	VDDA	Power	Capacitor 10nF between RCL and RCH Block capacitor 1µF against VSSA each	
V0	VDDA	Power	Block capacitor 100nF against VSSA	
SMON, CMON	VDDA	OUT	Measuring points (Nominal-amplitude 2.1V_{pp})	Left open
SINP, COSP	VDDA	IN	Encoder signals	
REFP	VDDA	IN	Encoder signals	VDDA
SINN, COSN, REFN	VDDA	IN	Encoder signals	V0
LED	VDDA	OUT	LED-control	Left open
CFGTPP, CFGGAIN, Z4/IRBIN/HWA3, MODE	VDDA	IN	Configuration	VSSA
CFGFILT	VDDA	IN	Configuration	Left open
NRES	VDDIO	IN/OUT	Pullup 10kΩ to VDDIO Reset-signal	Pullup 10kΩ to VDDIO
MOSI, SCK	VDDIO	IN	SPI, if necessary via series resistor 22...33Ω	VSS
SEN	VDDIO	IN	SPI, if necessary via series resistor 22...33Ω	Pullup 10kΩ to VDDIO
MISO	VDDIO	OUT	SPI, if necessary via series resistor 22...33Ω Pullup 1kΩ to VDDIO	
ECS, ECK, EDI	VDDIO	OUT	EEPROM	offen
EDO	VDDIO	IN	EEPROM	Pullup 10kΩ to VDDIO
TRG	VDDIO	IN	Trigger	Pullup 10kΩ to VDDIO
IR2/HWA2, IR1/HWA1, IR0/HWA0	VDDIO	IN	Configuration	VSSIO
A, B, Z	VDDIO	OUT	Output, if necessary connect to RS422-driver	Left open
NERR	VDDIO	OUT	Output, if necessary connect to RS422-driver Pullup 10kΩ to VDDIO	Pullup 10kΩ to VDDIO
TM	VDDIO	IN	VSS	VSS
N.C.		N.C.	Must not be connected	Must not be connected

The diagram below shows a minimum application, i.e. without serial SPI interface, as a block diagram. Further application circuits are in the attachment.

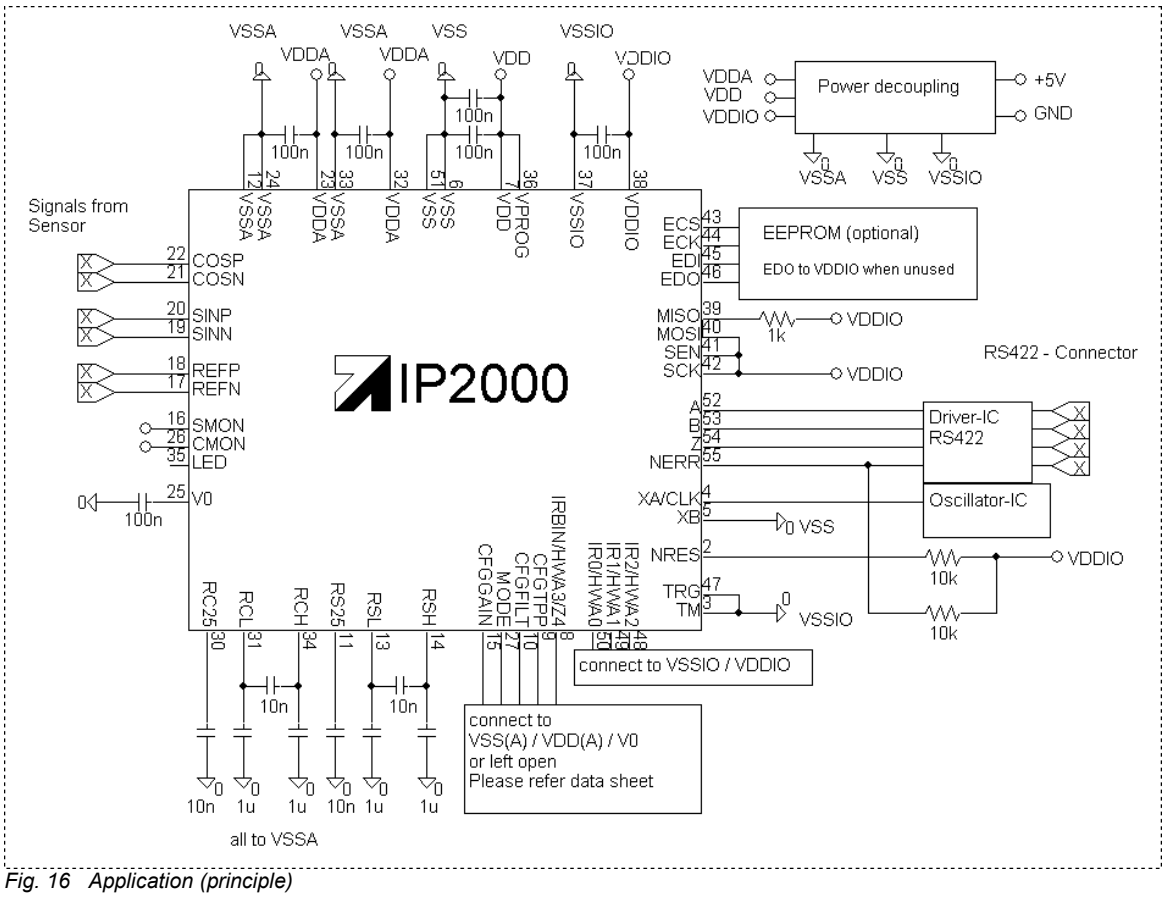


Fig. 16 Application (principle)

10.1.3 Power supply / reference voltages

As the IC GP-IP2000 includes two fast A/D converters, the same design rules applicable to A/D converters must be applied. All block capacitors are to be connected closely to the pad. Please note that the quality of the sensor power supply also influences the measuring accuracy of standard sensors. If necessary, additional LC filters to the sensor power supply and to AVDD must be included.

10.1.4 Digital interface 3.3V

The IC GP-IP2000 is designed to be used in 3.3V controller-systems. The diagram below shows an application example.

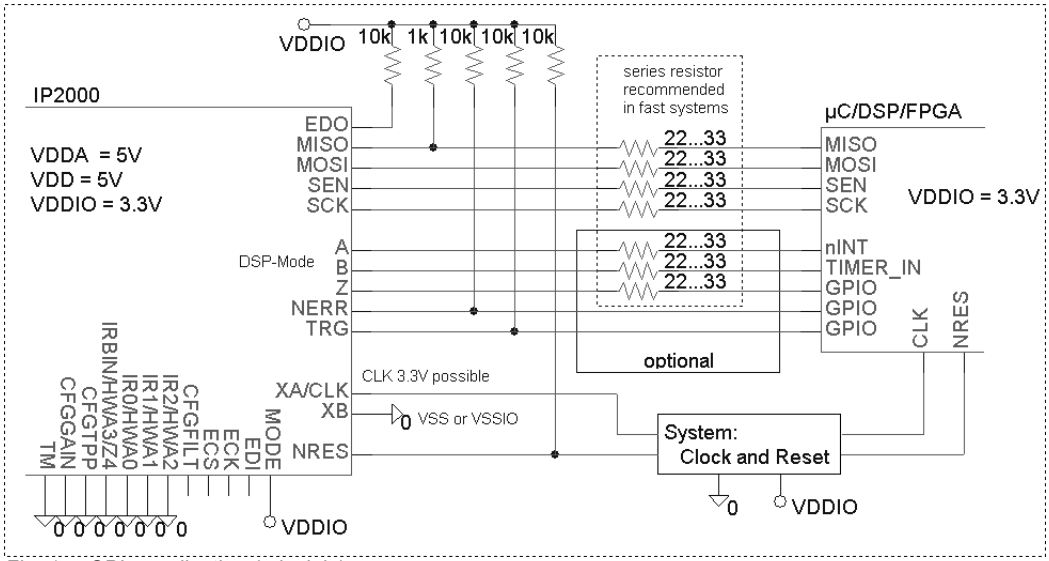


Fig. 17 SPI - application (principle)

10.1.5 Input circuit

The design of the analog input circuit depends on the type of the sensor that is connected. Standard sensors with differential signal outputs are connected directly to the SINP, SINN, COSP and COSN pins. If the sensor signals are transmitted through longer cables, an additional termination resistor between SINP and SINN or between COSP and COSN can be helpful. In this respect, please refer to the application notes of the sensor manufacturer. Single-ended sensors are connected typically to the SINP and COSP inputs. The DC reference levels of the GC-IP2000 and of the sensor must concordant in this case. The V0 signal can be used for this purpose. The current rating at this pin totals 800µA. Short and low-capacity wires should be used. A buffer operational amplifier may be included, if necessary.

Sensor with differential output signals

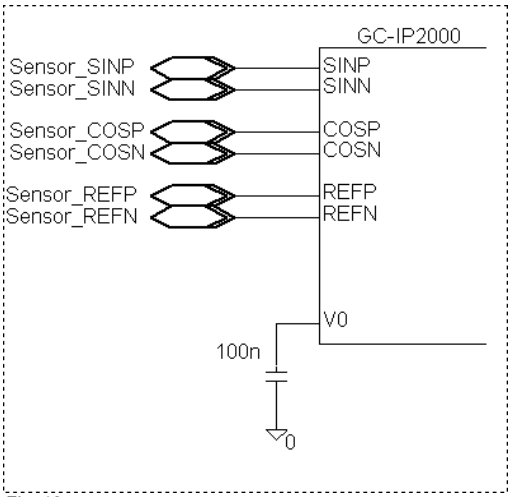


Fig. 18

- The amplitude of the sensor and the gain-factor of the GC-IP2000 are adapted by configuration bits GAIN(1:0).
- Reference level V0 is generated **internally**

Sensor with single-ended output signals (I)

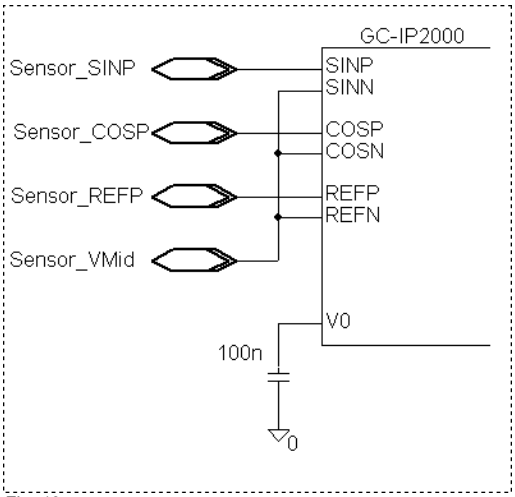


Fig. 19

- The amplitude of the sensor and the gain-factor of the GC-IP2000 are adapted by configuration bits GAIN(1:0).
- Reference level V0 is generated **by sensor**.

Sensor with single-ended output signals (II)

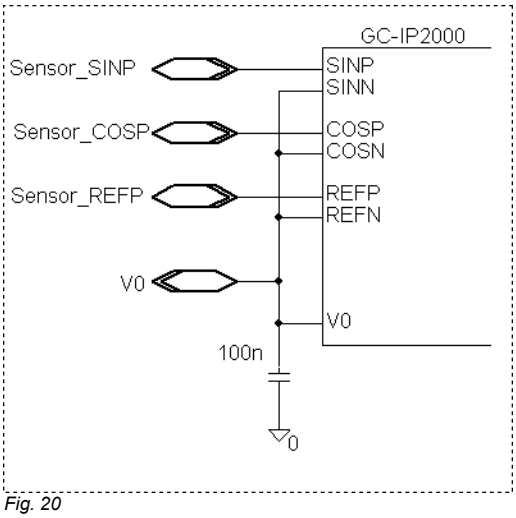


Fig. 20

- The amplitude of the sensor and the gain-factor of the GC-IP2000 are adapted by configuration bits `GAIN(1:0)`.
- Reference level `V0` is generated **by GC-IP2000**.
- The maximum current at Pin `V0` is 800µA

Sensor with a nominal amplitude of $2V_{pp}$

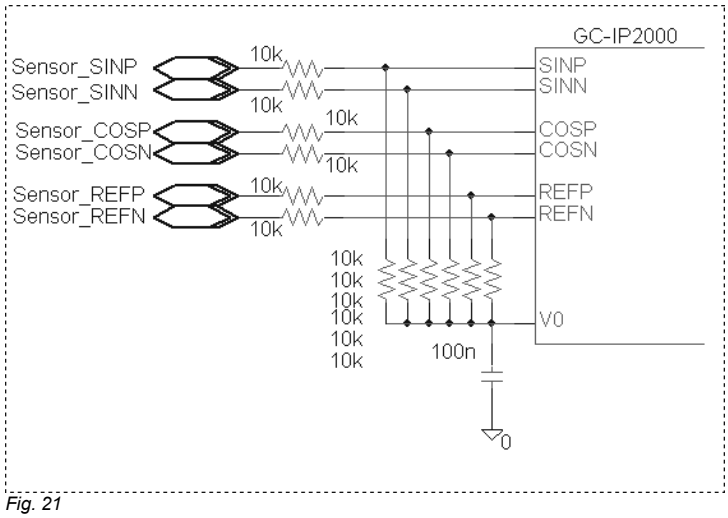


Fig. 21

- The nominal amplitude of the GC-IP2000 has to be set to $1V_{pp}$ by configuration bits `GAIN(1:0)`.
- External resistors between the input signals and pin `V0` are used as voltage divider for the sensor signals. The amplitude of the sensor signals will be divided by 2.

Sensor with current outputs or sensor containing photodiodes

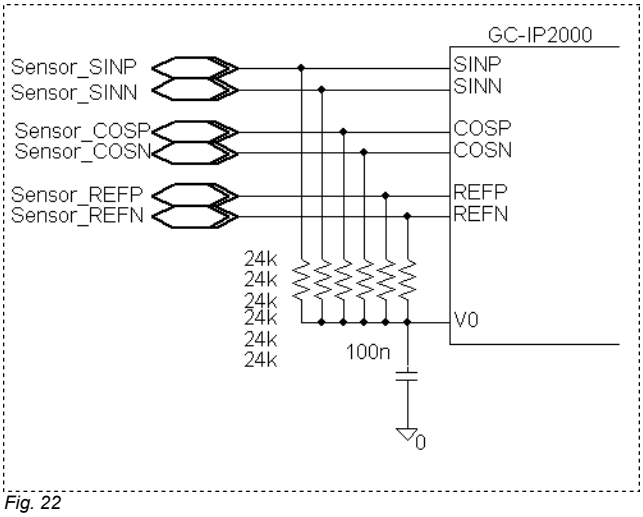


Fig. 22

- The nominal amplitude of the GC-IP2000 has to be set to $500mV_{pp}$, $250mV_{pp}$ or $75mV_{pp}$ by configuration bits `GAIN(1:0)`.
- External resistors between input and `V0` are required.
- Shown resistor value of R=24kΩ is suitable for an amplitiude of $11µA_{pp}$ and the setting of $500mV_{pp}$ as nominal amplitude of GC-IP2000.
- The value of the resistors has to be adjusted to the given sensor: $R = V_{nom} / (2 \cdot I_{nom})$.

Sensor containing antiparallel photodiodes
Adjustment of amplitude equality possible

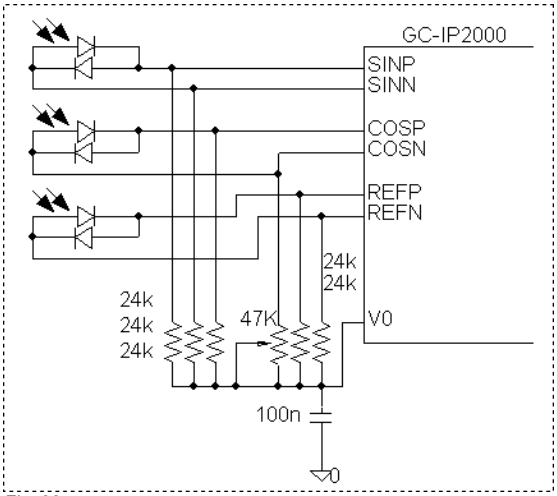


Fig. 23

- The nominal amplitude of the GC-IP2000 has to be set to $500mV_{pp}$, $250mV_{pp}$ or $75mV_{pp}$ by configuration bits `GAIN(1:0)`.
- The amplitude equality is adjusted by changing the amplitude of the cosine signal. The pins `SMON` and `CMON` are used for the measurement.
- Shown resistor value of R=24kΩ is suitable for an amplitiude of $11µA_{pp}$ and the setting of $500mV_{pp}$ as nominal amplitude of GC-IP2000.
- The value of the resistors has to be adjusted to the given sensor:
  $R = V_{nom} / (2 \cdot I_{nom})$ und $P_{Ampl} \approx 1.5 \cdot R$

Sensor containing photodiodes with common catode or common anode
Adjustment of amplitude equality and offset possible

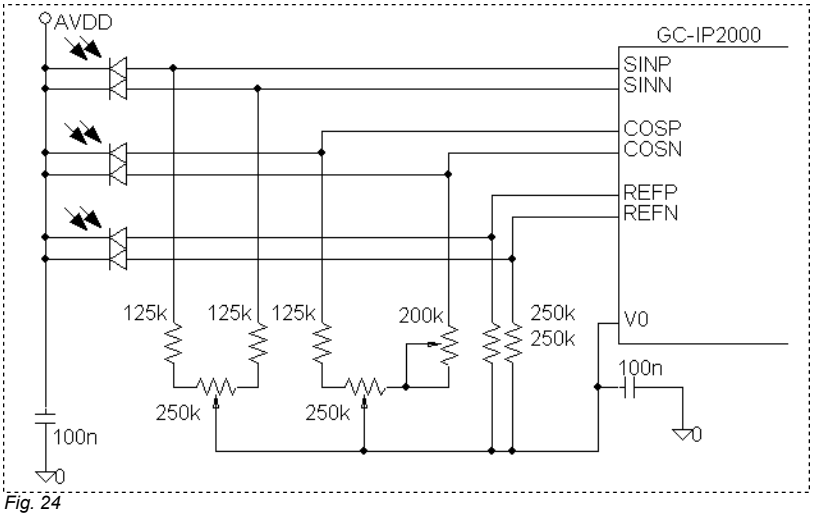


Fig. 24

- The nominal amplitude of the GC-IP2000 has to be set to 500mV$_{pp}$, 250mV$_{pp}$ or 75mV$_{pp}$ by configuration bits `GAIN(1:0)`.
- The amplitude equality is adjusted by changing the amplitude of the cosine signal. Thereafter the offset for both signals can be adjusted. The pins `SMON` and `CMON` are used for the measurement.
- Shown resistor value of R=24kΩ is suitable for an amplitiude of 0.5µA$_{pp}$ and the setting of 250mV$_{pp}$ as nominal amplitude of GC-IP2000.
- The resistor value is given by: $R = V_{nom} / (2 \cdot I_{nom})$. This resistor is partly designed as a potentiometer for the adjustment of the offset: $P_{Offs} \approx R$; $R_{FIX} = R - ½P_{Offs}$; $P_{Ampl} \approx 1.5 \cdot R_{FIX}$

For further information please request the detailed circuit of the evaluationboard „GP-2000“ and the recommended PCB-layout via E-Mail to interpolation@gemac-chemnitz.de.

10.2 Recommended configuration of registers

Basically, the configuration of the IC GC-IP2000 depends on the costumer's application. The following tables are to be understood as advices to the configuration of exemplary applications. If the configuration shall be loaded from EEPROM, the EEPROM must contain the identifier 0x99 at its adress 0x00.

10.2.1 Standard system 1Vpp, square wave output

Ressource	Usage
Analog input	Nominal amplitude $1V_{pp}$
ABZ	Active, ABZ-Output
Sensor monitoring	Active, no latching
SPI	Inactive
Timer / Trigger	Inactive
Automatic Controller	Active, standard
Filter	Active if possible

Register	Register value	Bits		Notes
CFG1	0x403F_1000	IR(3:0)	0000	Necessary: MABZ = 1 GAIN = 00 Mode = 00 RSV = 0 Recommended: MVLOW, MADC, MFAST, MGAIN, MOFF = 1 LVLOW, LADC, LFAST, LABZ, LGAIN, LOFF = 0 LPF = 1 for input frequencies < 100kHz DHE = 1 Depends on application: LEDMODE, HLD, DISZ, Z4, IR, TPP Not used: TRGSLP
		Z4	0	
		DISZ	0	
		MODE(1:0)	00	
		TPP(2:0)	000	
		RSV	0	
		DHE	1	
		TRGSLP	0	
		GAIN(1:0)	00	
		Mxxx / Bit(21:16)	111111	
		HLD	0	
		LEDMODE	0	
		Lxxx / Bit(29:24)	000000	
		LPF	1	
CFG2	0x0000_1000	T(7:0)	00000000	Necessary: Recommended: DISCTL = 0, GAINCTL = 00, OFFSCTL = 00 PHBER = 0 Depends on application: PH Not used: T, VT, SYNC, ASYNC
		VT(1:0)	00	
		SYNC(4:0)	00100	
		ASYNC	0	
		DISCTL	0	
		GAINCTL	00	
		OFFSCTL	00	
		PH(5:0)	000000	
		PHBER	0	
CTRLG	0x0400_0400	CNTRLG_S	0x0400	Recommended: Default value 0x400
		CNTRLG_C	0x0400	
CTRLO	0x0000_0000	CNTRLO_S	0x0000	Recommended: Default value 0x000
		CNTRLO_C	0x0000	
RSV	0x0000			Necessary: all bits 0

EEPROM

ADR	**0x1D**	**0x1C**	**0x1B**	**0x1A**	**0x19**	**0x18**	**0x17**	**0x16**	**0x15**	**0x14**	**0x13**	**0x12**	**0x11**	**0x10**	**0x0F**	**0x0E**	**0x0D**	**0x0C**	**...**	**0x00**
DAT	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x04	0x00	0x00	0x00	0x10	0x00	**0x40**	**0x3F**	**0x10**	**0x00**	-	0x99

Configuration pins (if EEPROM not used)

Pin	Configuration
Mode	VSS
CFGFILT	Left open
CFGGAIN	VSS
CFGTPP	Depends on application
IR(2:0), IRBIN	Depends on application

10.2.2 Standard system 1Vpp, controller output

Resource	Usage
Analog input	Nominal amplitude $1V_{pp}$
ABZ	DSP-Output
Sensor monitoring	Active, latching enabled
SPI	Active
Timer / Trigger	Depends on application
Automatic Controller	Active, standard
Filter	Active if possible

Register	Register value	Bits		Notes
CFG1	0x7737_1040	IR(3:0)	0000	Necessary: MABZ = 0 GAIN = 00 Mode = 01 RSV = 0 Recommended: MVLOW, MADC, MFAST, MGAIN, MOFF = 1 LVLOW, LADC, LFAST, LGAIN, LOFF = 1 LABZ = 0 LPF = 1 for input frequencies < 100kHz Depends on application: LEDMODE, DISZ, IR, TRGSLP Not used: DHE, Z4, TPP, HLD
		Z4	0	
		DISZ	0	
		MODE(1:0)	01	
		TPP(2:0)	000	
		RSV	0	
		DHE	1	
		TRGSLP	0	
		GAIN(1:0)	00	
		Mxxx / Bit(21:16)	110111	
		HLD	0	
		LEDMODE	0	
		Lxxx / Bit(29:24)	110111	
		LPF	1	
CFG2	0x0000_1000	T(7:0)	00000000	Necessary: Recommended: DISCTL = 0, GAINCTL = 00, OFFSCTL = 00 PHBER = 0 SYNC = 00100 ASYNC = 0 Depends on application: PH, T, VT Not used:
		VT(1:0)	00	
		SYNC(4:0)	00100	
		ASYNC	0	
		DISCTL	0	
		GAINCTL	00	
		OFFSCTL	00	
		PH(5:0)	000000	
		PHBER	0	
CTRLG	0x0400_0400	CNTRLG_S	0x0400	Recommended: Default value 0x400
		CNTRLG_C	0x0400	
CTRLO	0x0000_0000	CNTRLO_S	0x0000	Recommended: Default value 0x000
		CNTRLO_C	0x0000	
RSV	0x0000			Necessary: all bits 0

EEPROM

ADR	**0x1D**	**0x1C**	**0x1B**	**0x1A**	**0x19**	**0x18**	**0x17**	**0x16**	**0x15**	**0x14**	**0x13**	**0x12**	**0x11**	**0x10**	**0x0F**	**0x0E**	**0x0D**	**0x0C**	**...**	**0x00**
DAT	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x04	0x00	0x00	0x00	0x10	0x00	**0x77**	**0x37**	**0x10**	**0x40**	-	0x99

Configuration pins (if EEPROM not used)

Pin	Configuration
Mode	VDD
CFGFILT	Left open
CFGGAIN	VSS
CFGTPP	Any
IR(2:0), IRBIN	Depends on application

10.2.3 Standard system 1Vpp, square wave output and controller output

Resource	Usage
Analog input	Nominal amplitude $1V_{pp}$
ABZ	Active, ABZ-Output
Sensor monitoring	Active, latching enabled
SPI	Active
Timer / Trigger	Depends on application
Automatic Controller	Active, standard
Filter	Active if possible

Register	Register value	Bits		Notes
CFG1	0x7F3F_1000	IR(3:0)	0000	Necessary: MABZ = 1 GAIN = 00 Mode = 00 RSV = 0 Recommended: MVLOW, MADC, MFAST, MGAIN, MOFF = 1 LVLOW, LADC, LFAST, LGAIN, LOFF = 1 LABZ = 1 DHE = 1 LPF = 1 for input frequencies < 100kHz Depends on application: LEDMODE, DISZ, IR, TRGSLP, Z4, TPP, HLD Not used:
		Z4	0	
		DISZ	0	
		MODE(1:0)	00	
		TPP(2:0)	000	
		RSV	0	
		DHE	1	
		TRGSLP	0	
		GAIN(1:0)	00	
		Mxxx / Bit(21:16)	111111	
		HLD	0	
		LEDMODE	0	
		Lxxx / Bit(29:24)	111111	
		LPF	1	
CFG2	0x0000_1000	T(7:0)	00000000	Necessary: Recommended: DISCTL = 0, GAINCTL = 00, OFFSCTL = 00 PHBER = 0 SYNC = 00100 ASYNC = 0 Depends on application: PH, T, VT Not used:
		VT(1:0)	00	
		SYNC(4:0)	00100	
		ASYNC	0	
		DISCTL	0	
		GAINCTL	00	
		OFFSCTL	00	
		PH(5:0)	000000	
		PHBER	0	
CTRLG	0x0400_0400	CNTRLG_S	0x0400	Recommended: Default value 0x400
		CNTRLG_C	0x0400	
CTRLO	0x0000_0000	CNTRLO_S	0x0000	Recommended: Default value 0x000
		CNTRLO_C	0x0000	
RSV	0x0000			Necessary: all bits 0

EEPROM

ADR	**0x1D**	**0x1C**	**0x1B**	**0x1A**	**0x19**	**0x18**	**0x17**	**0x16**	**0x15**	**0x14**	**0x13**	**0x12**	**0x11**	**0x10**	**0x0F**	**0x0E**	**0x0D**	**0x0C**	**...**	**0x00**
DAT	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x04	0x00	0x00	0x00	0x10	0x00	**0x7F**	**0x3F**	**0x10**	**0x00**	-	0x99

Configuration pins (if EEPROM not used)

Pin	Configuration
Mode	VSS
CFGFILT	Left open
CFGGAIN	VSS
CFGTPP	Depends on application
IR(2:0), IRBIN	Depends on application

10.2.4 System 75mVpp, square wave output

Resource	Usage
Analog input	Nominal amplitude 75mV$_{pp}$
ABZ	Active, ABZ-Output
Sensor monitoring	Active, no latching
SPI	Inactive
Timer / Trigger	Inactive
Automatic Controller	Active, standard
Filter	Active if possible

Register	Register value	Bits		Notes
CFG1	0x403F_D000	IR(3:0)	0000	Necessary: MABZ = 1 GAIN = 11 Mode = 00 **LPF = 1** RSV = 0 Recommended: MVLOW, MADC, MFAST, MGAIN, MOFF = 1 LVLOW, LADC, LFAST, LABZ, LGAIN, LOFF = 0 DHE = 1 Depends on application: LEDMODE, HLD, DISZ, Z4, IR, TPP Not used: TRGSLP
		Z4	0	
		DISZ	0	
		MODE(1:0)	00	
		TPP(2:0)	000	
		RSV	0	
		DHE	1	
		TRGSLP	0	
		GAIN(1:0)	11	
		Mxxx / Bit(21:16)	111111	
		HLD	0	
		LEDMODE	0	
		Lxxx / Bit(29:24)	000000	
		LPF	**1**	
CFG2	0x0000_1000	T(7:0)	00000000	Necessary: Recommended: DISCTL = 0, GAINCTL = 00, OFFSCTL = 00 PHBER = 0 Depends on application: PH Not used: T, VT, SYNC, ASYNC
		VT(1:0)	00	
		SYNC(4:0)	00100	
		ASYNC	0	
		DISCTL	0	
		GAINCTL	00	
		OFFSCTL	00	
		PH(5:0)	000000	
		PHBER	0	
CTRLG	0x0400_0400	CNTRLG_S	0x0400	Recommended: Default value 0x400
		CNTRLG_C	0x0400	
CTRLO	0x0000_0000	CNTRLO_S	0x0000	Recommended: Default value 0x000
		CNTRLO_C	0x0000	
RSV	0x0000			Necessary: all bits 0

EEPROM

ADR	**0x1D**	**0x1C**	**0x1B**	**0x1A**	**0x19**	**0x18**	**0x17**	**0x16**	**0x15**	**0x14**	**0x13**	**0x12**	**0x11**	**0x10**	**0x0F**	**0x0E**	**0x0D**	**0x0C**	**...**	**0x00**
DAT	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x04	0x00	0x00	0x00	0x10	0x00	**0x40**	**0x3F**	**0xD0**	**0x00**	-	0x99

Configuration pins

Pin	Configuration
Mode	VSS
CFGFILT	Left open
CFGGAIN	Left open
CFGTPP	Depends on application
IR(2:0), IRBIN	Depends on application

To set the bit LPF to 1, it is necessary to use the EEPROM for configuration.

10.3 Propagation delay

10.3.1 Propagation delay analog

The propagation delay of the input signals through the instrument amplifier of the GC-IP2000 is given by the chosen gain factor and the setting of the corner frequency of the noise filter. The following table shows approximate values for some configurations.

Table 32 Propagation delay analog

	1Vpp (nominal)	75mVpp (nominal)
LPF = 0	130ns	200ns
LPF = 1	700ns	750ns

ⓘ *Please note that additional filters at the inputs change the propagation delay. Furthermore it is necessary to pay attention to small tolerances of used components, as otherwise, a relevant phase shift between sine and cosine will occur. This can be corrected by using the phase potentiometer if necessary.*

10.3.2 Propagation delay digital

The propagation delay t_v between sampling and measurement value in the SPI-register MVAL or CNT is 125 system clocks. For using a counter at the outputs A, B and Z this time is 155 system clocks.

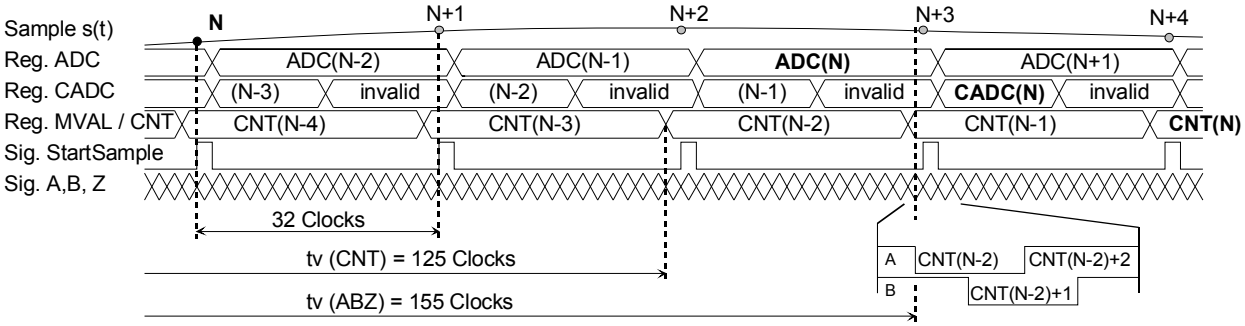


Fig. 25 Propagation delay digital

ⓘ Please note that the **constant** *propagation delay of the IC (as in every digital system) causes a frequency dependent phase shift between the analog input signals and the output signals. ($d\varphi = 2\pi \cdot f \cdot t_v$). The following figures show this behaviour for the output signal Z as an example. Shown are two different input signals. The behaviour of the signals A and B is equivalent.*

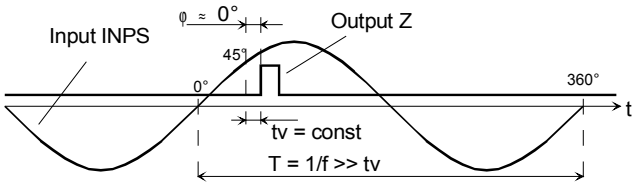


Fig. 26 Constant propagation delay (I)

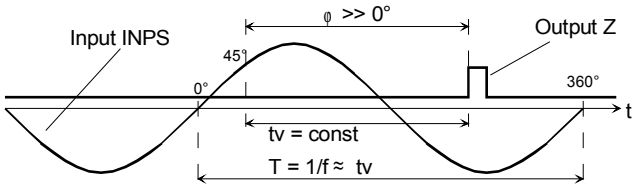


Fig. 27 Constant propagation delay (II)

10.3.3 Discretisation of time

The level at the ABZ-outputs of the GC-IP2000 do not change faster than given by the configured edge interval t_{pp}. However, the time t_{ideal}, computed from input signal, may be outside this time period. The following example is to explain the behaviour of the IC:

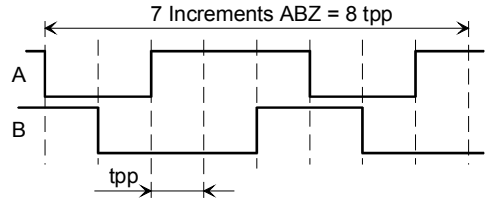


Fig. 28 Discretisation of time

f_{OSZ} = 20MHz; CFGTPP = '000' → t_{pp} = 50ns
f_{INPUT} = 8.75kHz; IRATE = 2000 → $t_{ABZ(ideal)}$ = 57.14ns
$7 \cdot t_{ABZ(ideal)} = 8 \cdot t_{pp}$

10.4 Using of SPI interface

The control of the SPI signals happens by software from a processor or microcontroller, generally. Some important program sequences are shown below.

10.4.1 Initialisation

Table 33 Initialisation via SPI

No.	Program step	Details
1	Hardware initialisation	Signal SEN to H Signal NRES to L Configuration of controller's SPI to 16 Bit, MSB first Configuration of controller's SPI to mode 0: Default: SCK = L Sampling: rising edge SCK, Changing MOSI/MISO falling edge SCK
2	Reset GC-IP2000	Signal NRES to H Wait until signal MISO/nWAIT is at H-level
3	**For Multichannel-SPI only:** Setting of the SPI hardware adress	Writing of command SETHWA to register CMD Low-Level-SPI-Word: 0x9008 (WRA_Broadcast) 0xB020 (WRD_Broadcast)
4	Query GC-IP2000	Reading of register ID/REV Reading of register EEPSTAT, wait until bit EEPBSY = 0 Evaluation of the bit EEPEXIST
5a	Configuration of GC-IP2000, if EEPROM is connected	Configuration of registers which deviate from EEPROM
5b	Configuration of GC-IP2000, in case of if no EEPROM is connected	Configuration of registers CFG1 and CFG2 Configuration of registers CNTRLG and CNTRLO with start values for signal controller
6	Enable trigger holding register	Reading of register MVAL twice
7	Counter reset	Writing of command RESCNT to register CMD
8	Settling of signal controller	Motion of encoder; Settling time between 10 and 120 sine periods: depends on error value and content of bits OFFSCTL(1:0) and GAINCTL(1:0)
9	Motion of encoder over index mark / reference point of scale	Reading of register STAT Evaluation of bit ZSTAT

10.4.2 Measurement

The following sequence is used for software controlled measurement. The timing of measurement is given by the processor:

Table 34 Measurement via SPI, processor controlled

No.	Program step	Details
1	Reading of measurement value	Reading of register MVAL
2	Evaluation of status bits	Check for error: evaluation bit 0 / register MVAL or signal NERR resp. Check for trigger: evaluation bit 1 / register MVAL
3	**In case of error only** Evaluation of status register	Reading of register STAT Evaluation of error reason
4	**In case of error only** Restart measurement	Writing of command RESCNT to the register CMD Motion of encoder over index mark of the scale again

The following sequence is used for interrupt driven measurements. The timing of measurement is given by the GC-IP2000. For this purpose, the bits VT(1:0), T(7:0) and MODE(1:0) must be set accordingly. Please refer Sections 6.7.1 and 6.8, too.

Table 35 Interrupt driven measurement via SPI, timer and trigger active

No.	Program step	Details
1	Wait for interrupt at pin A	Falling edge at signal A = nINT
2	Evaluation of status	Reading of register STAT Check for error, if necessary evaluation of error reason Evaluation of trigger reason
3	Reading of measurement value	Reading of register MVAL
4	**In case of error only** Restart measurement	Writing of command RESCNT to register CMD Pass over the index mark of scale again
5	Reading of all measurement values stored in IC	Repeating of steps 2-4, until signal A goes H

10.4.3 Initialisation of EEPROM

This sequence can be used to adapt the GC-IP2000 to an existing mesurement system. For this purpose an automatic settling of the internal signal control takes place first, thereafter the whole configuration will be copied to the EEPROM. With this, the settling time of the signal control will be shortened considerably at the next start of the system. More information for using the EEPROM is shown in Section 7.2.

Table 36 Initialization of EEPROM

No.	Program step	Details
1	Phase adjust	Adjust phase according to Section 6.7.2.
2	Settling of signal controller	Motion of encoder; Settling time between 10 and 120 sine periods: depends on error value and content of bits OFFSCTL(1:0) and GAINCTL(1:0)
3	Check for errors	Reading of register MVAL , evaluation bit 0 Alternative: evaluation of signal NERR
4	Enable EEPROM	Check BSY bits in register EEPSTAT; if necessary, wait. Writing of the EEPROM-OpCode EWEN (0x03) to register EEPOPC
5	Copy content of all configuration registers to EEPROM	Check BSY bits in register EEPSTAT; if necessary, wait. Writing of command WCFG to register CMD
6	Wait during programming time of EEPROM	
7	Mark EEPROM as GC-IP2000-EEPROM	Check BSY bits in register EEPSTAT; if necessary, wait. Writing of 0x00 to register EEPADR Writing of 0x99 to register EEPDAT Writing of 0x04 to register EEPOPC

10.5 Measurement of absolute positions

The GC-IP2000 is designed to determine covered lengths or angles, basically. To determine an absolute position, the motion of the sensor over an index mark is required. In the bit ZSTAT of the register STAT can be seen if the counter value relates to the index mark of the scale. Additionally, it is possible to determine the phase angle within the sine period by reading the register PHI at any time. The scaling of PHI and CNT is shown in Section 8. The relation between PHI and CNT at interpolation rates of 2048, 2000 and 1600 is shown in the following table f*or instance*.

Table 37 Relation between PHI and CNT

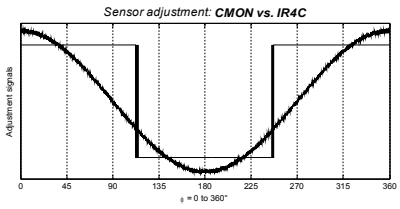
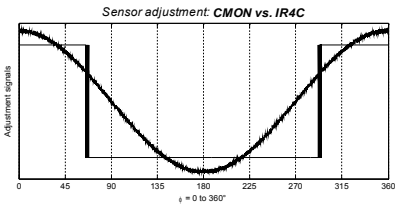
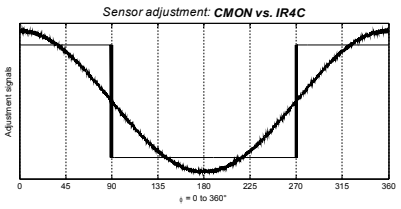
ZSTAT	PHI / CNT
ZSTAT = 0	No relation between PHI and CNT
ZSTAT = 1	PHI = (CNT modulo IRATE) – ($^1/_8$·IRATE); IRATE = 2048, 2000 or 1600 In case of a short-time disturbance at the analog inputs (e.g. switching pulse) this relation is not valid. In this case, the value of PHI shows this disturbance, the register CNT contains the value as before that short-time disturbance. The value of DHI is 0 in that case.

10.6 Sensor adjustment

The IC GC-IP2000 performs an automatic adjustment of amplitude and offset of both signals of the encoder. It is reasonable to correct static errors of the sensor previously to use the full control range for dynamic errors. For this, subsidiary signals at the pins A, B and Z are available in the modes „sensor adjustment 1“ and „sensor adjustment 2“. A description of the adjustment sequence can be found in Section 6.7.2. Additionally, the following figures show typical signal characteristics.

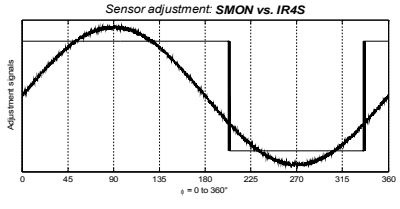
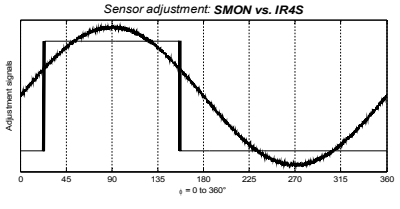
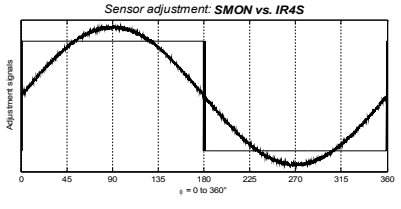
Adjustment offset cosine – signals CMON and IR4C (pin A)

Mode '10' (Sensor adjustment 1), signal controller inactive / correction values in the middle of the setting range

Offset cosine **positive** Duty cycle IR4C > 50%	Offset cosine **negative** Duty cycle IR4C < 50%	Offset cosine **adjusted** Duty cycle IR4C = 50%
		

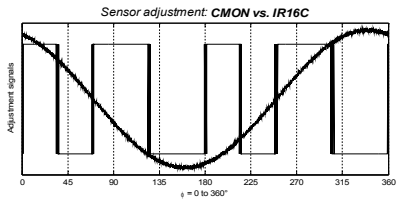
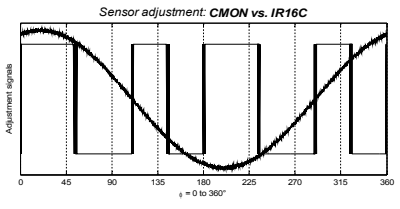
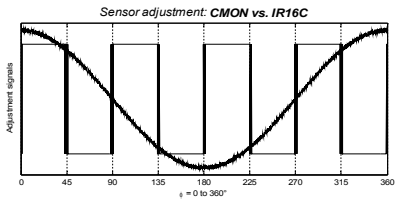
Adjustment offset sine – signals SMON and IR4S (pin B)

Mode '10' (Sensor adjustment 1), signal controller inactive / correction values in the middle of the setting range

Offset sine **positive** Duty cycle IR4S > 50%	Offset sine **negative** Duty cycle IR4S < 50%	Offset sine **adjusted** Duty cycle IR4S = 50%
		

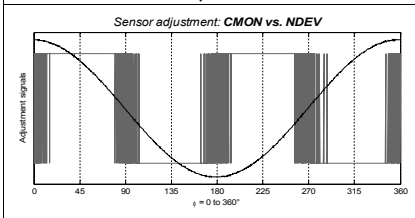
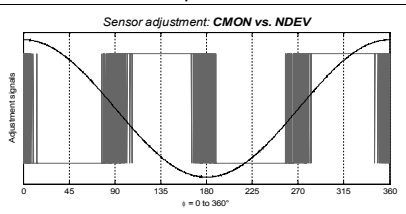
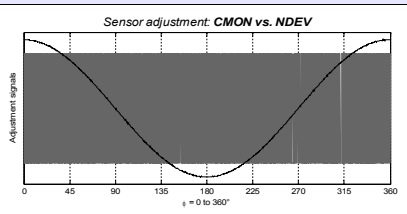
Adjustment phase (coarse) – signals CMON and IR16C (pin B)

Mode '11' (Sensor adjustment 2), signal controller active

Phase betw. cosine and sine **> 90°** Duty cycle IR16C ≠ 50% H-L-edge IR16C at φ < 45°	Phase betw. cosine and sine **< 90°** Duty cycle IR16C ≠ 50% H-L-edge IR16C at φ > 45°	Phase betw. cosine and sine **adjusted** Duty cycle IR16C = 50% H-L-edge IR16C at φ = 45°
		

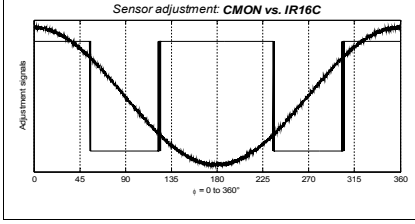
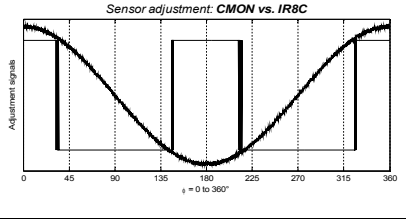
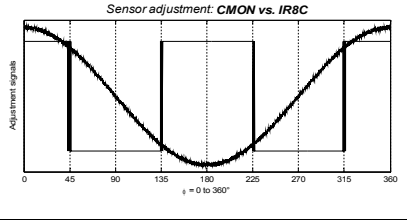
Adjustment phase (fine) – signals CMON and NDEV (pin Z)

Mode '11' (Sensor adjustment 2), signal controller active

Phase betw. cosine and sine **>≈ 90°** Frequency(NDEV) ≈ ½·Frequency(CMON) H-level NDEV at φ = 45°	Phase betw. cosine and sine **<≈ 90°** Frequency(NDEV) ≈ ½·Frequency(CMON) L-level NDEV at φ = 45°	Phase betw. cosine and sine **adjusted** Frequency(NDEV) >> Frequency(CMON)
		

Adjustment amplitude coincidence – signals CMON and IRC8 (pin A)

Mode '11' (Sensor adjustment 2), signal controller inactive / correction values in the middle of the setting range

Ampl. cosine **greater then** ampl. sine Duty cycle IR8C > 50%	Ampl. cosine **lower then** ampl. sine Duty cycle IR8C < 50%	Ampl. cosine and ampl. sine are **equal** Duty cycle IR8C = 50%
		

10.7 Connection of digital encoders

The GC-IP2000 is designed to connect analog encoders, basically. However, a special resistor network and a special configuration allow the use of the internal interpolation counter.

Hardware

Each input will be connected via a differential voltage divider:

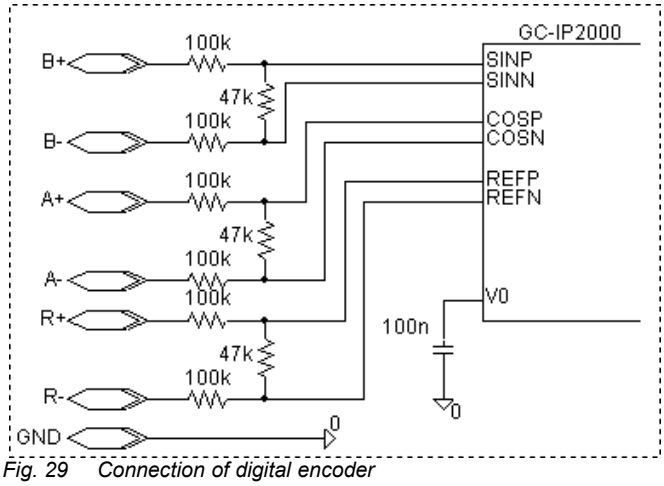


Fig. 29 Connection of digital encoder

Configuration

Register	Register value	Bits	
CFG1	0x0404_0000 (referenz enabled) 0x0404_0020 (referenz disabled)	IR(3:0)	Any
		Z4	Any
		DISZ	0 / 1
		MODE(1:0)	Any
		TPP(2:0)	Any
		RSV	0
		DHE	Any
		TRGSLP	Any
		GAIN(1:0)	**00**
		Mxxx / Bit(21:16)	**000000**
		HLD	0
		LEDMODE	Any
		Lxxx / Bit(29:24)	000000
		LPF	**0**
CFG2	0x0001_1000	T(7:0)	Any
		VT(1:0)	Any
		SYNC(4:0)	Any
		ASYNC	Any
		DISCTL	**1**
		GAINCTL	00
		OFFSCTL	00
		PH(5:0)	000000
		PHBER	0
CTRLG	0x0400_0400	CNTRLG_S	0x0400
		CNTRLG_C	0x0400
CTRLO	0x0000_0000	CNTRLO_S	0x0000
		CNTRLO_C	0x0000
RSV	0x0000		

Counter value

In order to compute the counter value, the interpolation result has to be divided by ¼ of the interpolation rate

Example: interpolation result (MVAL) = 100005, interpolation rate = 2000
→ Counter value = 100005 / 500 = 200.

The maximum input frequency is $f_{MAX} = f_{OSZ} / 32 \cdot (90° - \varphi) / 360°$; φ: phase error between A and B

Example: f_{OSZ} = 20MHz, φ = 5°
→ f_{MAX} = 20MHz / 32 · 85° / 360° = 147kHz