

2.5V-3.3V Low-Skew 1-4 PECL Fanout Buffer

FEATURES

- Four differential 2.5V/3.3V LVPECL output pairs.
- Output Frequency: ≤ 266 MHz.
- Selectable CLK0 or CLK1 inputs for redundant and multiple frequency fanout applications
- Translates single-ended LVCMOS or LVTTTL input to 3.3V or 2.5V LVPECL differential outputs.
- Output Skew: 25ps (typ).
- Part-to-part skew: 85ps (typ).
- Propagation delay: 0.7ns (typ).
- Additive Jitter: 80 fs (typ).
- Operating Supply Voltage: 2.375V ~ 3.63V.
- Operating temperature range from -40°C to 85°C.
- Package availability: 20-pin QFN and 20-pin TSSOP

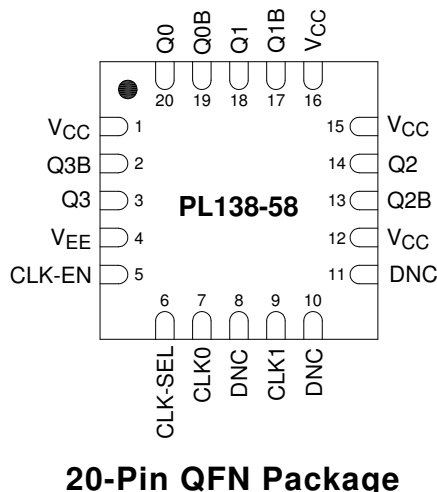
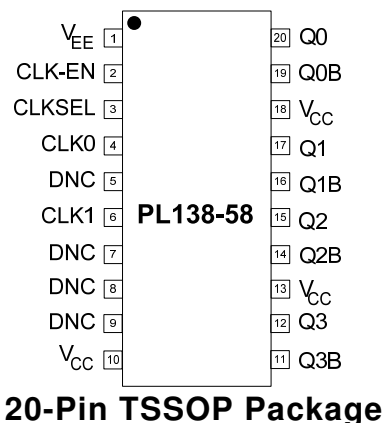
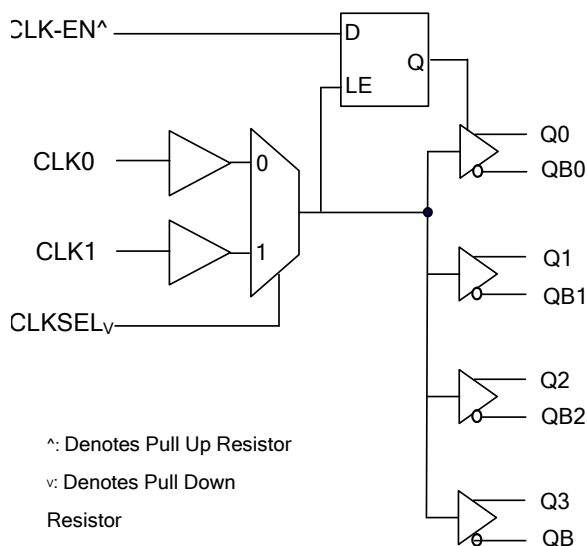
DESCRIPTION

The PL138-58 is a high performance low-cost 1: 4 outputs Differential LVPECL fanout buffer, with very low-skew and LVCMOS/LVTTTL input interface for 3.3V and 2.5V operations.

PL138-58's two single-ended clock inputs are designed to accept a standard LVCMOS or LVTTTL signal levels and produce a high quality set of 2.5V or 3.3V LVPECL outputs with the lowest possible skew, guaranteed for part-to-part or lot-to lot. The clock enable is internally synchronized to assure no runt clock pulses on the output during asynchronous assertion/deassertion of the clock enable pin.

Designed to fit in a small form-factor package, PL138 family offers very low-power consumption, and the lowest additive jitter of any comparable device.

BLOCK DIAGRAM



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PIN DESCRIPTIONS

Name	Package Pin #		Type	Description
	QFN-20	TSSOP-20		
V _{CC}	1, 12, 15, 16	10, 13, 18	P	Power Supply pin connection
QB0 ~ QB3	2, 13, 17, 19	11, 14, 16, 19	O	LVPECL Complementary output
Q0 ~ Q3	3, 14, 18, 20	12, 15, 17, 20	O	LVPECL True output
V _{EE}	4	1	P	Power Supply pin connection
CLK-EN	5	2	I	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, QB outputs are forced high. LVCMOS / LVTTTL interface levels. 50kΩ Internal Pull-Up Resistor.
CLK-SEL	6	3	I	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTTL interface levels. 50kΩ Internal Pull-Down Resistor.
CLK0	7	4	I	LVCMOS, LVTTTL Clock input.
DNC	8, 10, 11	5, 7, 8, 9	-	Do Not Connect.
CLK1	9	6	I	LVCMOS, LVTTTL Clock input.

INPUT CLOCK CONTROL FUNCTION

Inputs			Outputs	
CLK-EN	CLKSEL	Source	Q0:Q3	Q0B:Q3B
0	0	CLK0	Disabled Low	Disabled High
0	1	CLK1	Disabled Low	Disabled High
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

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ELECTRICAL SPECIFICATIONS
Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	-0.5	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		110	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model	2			kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 10\%$; $V_{EE} = 0V$; $T_A = -40^\circ C$ TO $+85^\circ C$

PARAMETER	SYMBOL	-40°C			25°C			80°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output High Voltage*	V_{OH}	2.215	2.320	2.420	2.275	2.350	2.420	2.275	2.35	2.420	V
Output Low Voltage*	V_{OL}	1.470	1.610	1.745	1.490	1.585	1.680	1.490	1.585	1.680	V
Input High Voltage†	V_{IH}	$0.7V_{CC}$		$V_{CC}+0.3$	$0.7V_{CC}$		$V_{CC}+0.3$	$0.7V_{CC}$		$V_{CC}+0.3$	V
Input Low Voltage†	V_{IL}	-0.3		$0.3V_{CC}$	-0.3		$0.3V_{CC}$	-0.3		$0.3V_{CC}$	V
Input High Current	I_{IH}			200			200			200	μA
Input Low Current	I_{IL}	-150			-150			-150			μA

DC CHARACTERISTICS, $V_{CC} = 2.5V \pm 5\%$; $V_{EE} = 0V$; $T_A = -40^\circ C$ TO $+85^\circ C$

PARAMETER	SYMBOL	-40°C			25°C			80°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output High Voltage*	V_{OH}	1.415	1.520	1.620	1.475	1.550	1.620	1.475	1.55	1.620	V
Output Low Voltage*	V_{OL}	0.670	0.810	0.945	0.690	0.785	0.880	0.690	0.785	0.880	V
Input High Voltage†	V_{IH}	$0.7V_{CC}$		$V_{CC}+0.3$	$0.7V_{CC}$		$V_{CC}+0.3$	$0.7V_{CC}$		$V_{CC}+0.3$	V
Input Low Voltage†	V_{IL}	-0.3		$0.3V_{CC}$	-0.3		$0.3V_{CC}$	-0.3		$0.3V_{CC}$	V
Input High Current	I_{IH}			150			150			150	μA
Input Low Current	I_{IL}	-120			-120			-120			μA

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

Input parameters vary with the ratio of $V_I : (V_{CC} - V_{EE})$

* Outputs terminated with 50Ω to $V_{CCO} - 2V$.

† V_{IH}/V_{IL} apply to CLK0, CLK1, CLKEN, CLKSEL.

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AC Electrical Characteristics

$V_{CC} = -3.8V$ to $-2.375V$ or, $V_{CC} = 2.375V$ to $3.8V$; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

PARAMETER		SYMBOL	-40°C			25°C			80°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Frequency		f_{MAX}			266			266			266	MHz
Propagation Delay*		t_{PD}	570	700	800	610	740	840	650	810	940	ps
Output Skew ** †		$tsk(o)$		25	37		25	37		25	37	ps
Part-to-Part Skew *** †		$tsk(pp)$		85	225		85	225		85	225	ps
Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		t_{APJ}		80			80			80		fs
Output Rise/Fall Time	20% to 80%	t_R / t_F			300			300			300	ps

All parameters are measured at $f \leq 266MHz$, unless otherwise noted.

* Measured from the differential input crossing point to the differential output crossing point.

** Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

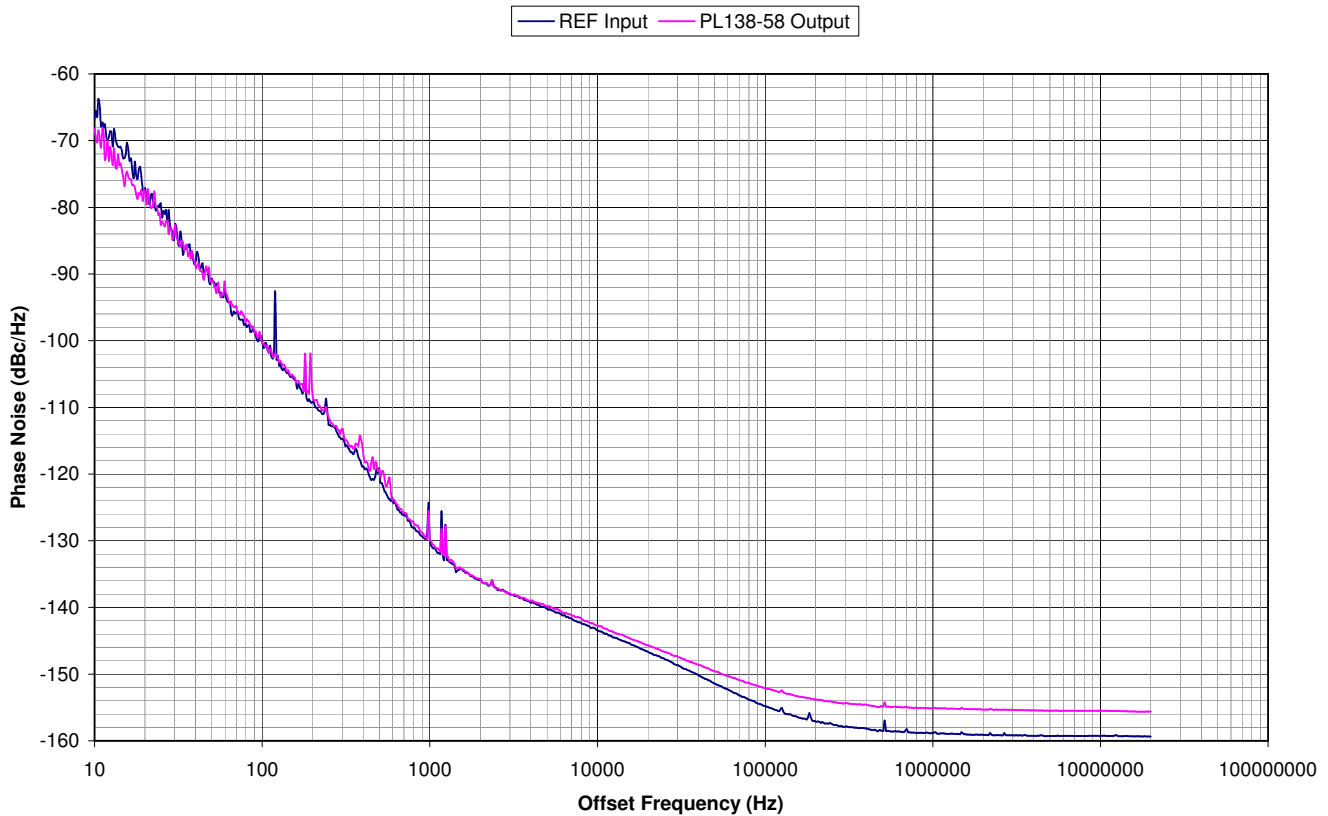
*** Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

† This parameter is defined in accordance with JEDEC Standard 65.

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NOISE CHARACTERISTICS (Commercial and Industrial Temperature Devices)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t _{APJ}	Additive Phase Jitter	V _{DD} =3.3V, Frequency=155.52MHz Offset=12KHz ~ 20MHz		80		fs

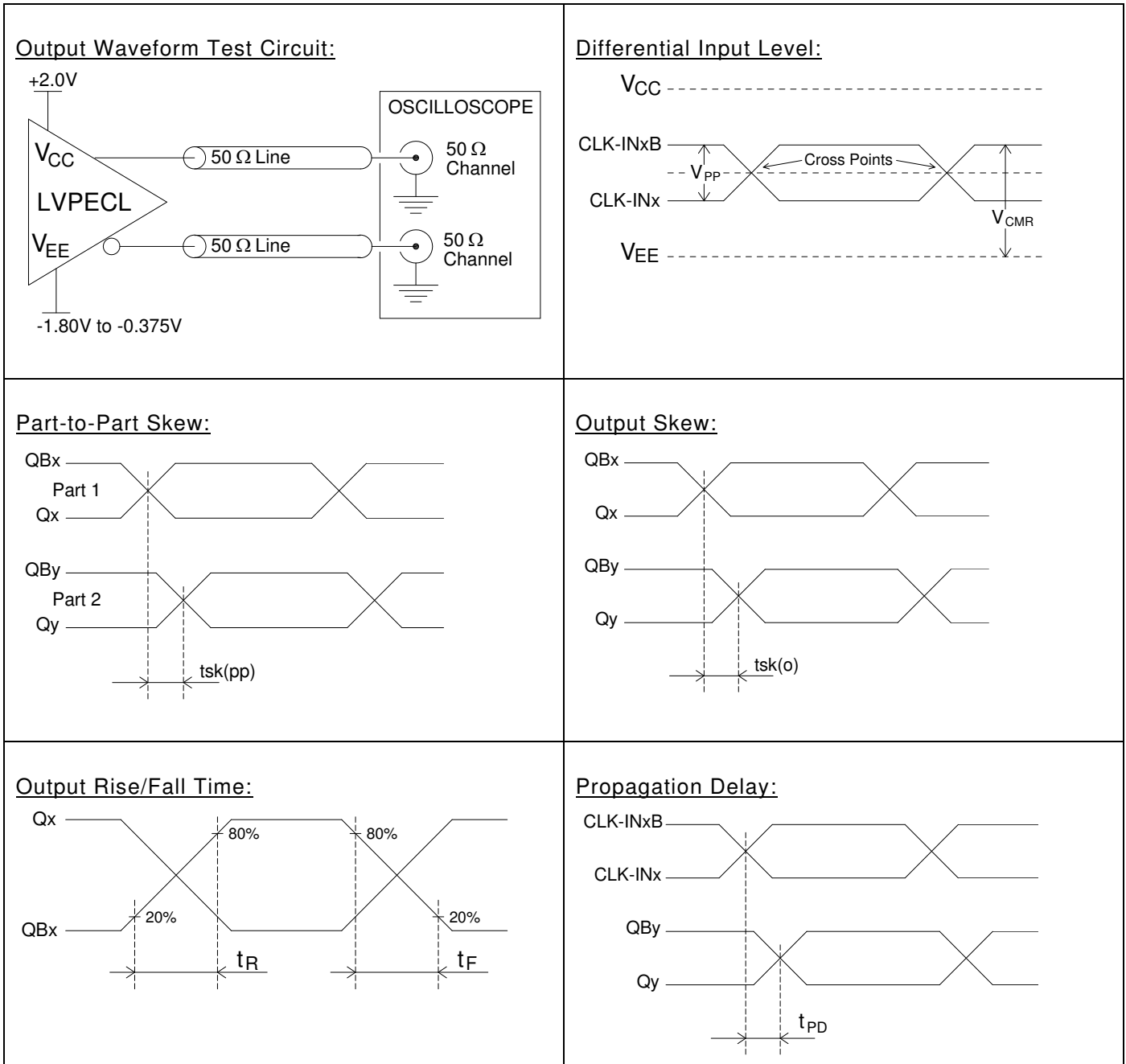


When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called "Additive Phase Jitter". The formula for the Additive Phase Jitter is as follows:

$$\text{Additive Phase Jitter} = \sqrt{(\text{Output Phase Jitter})^2 - (\text{Input Phase Jitter})^2}$$

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PARAMETER MEASUREMENT INFORMATION



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TERMINATION FOR LVPECL OUTPUTS

The required termination for LVPECL is 50Ω to a V_{CC}-2V DC voltage level. Below are two schematics to implement this termination.

LVPECL Termination Schematic #1:	LVPECL Termination Schematic #2:
<p>VCC=3.3V, Ideal values: R1=127Ω , R2=82.5Ω Commercial values (E24): R1=130Ω , R2=82Ω VCC=2.5V, Ideal values: R1=250Ω , R2=62.5Ω Commercial values (E24): R1=240Ω , R2=62Ω</p>	<p>Schematic #2 is an alternative simplified termination. VCC=3.3V, Ideal value: RT=48.7Ω Commercial value: RT=50Ω (E24: 51Ω) VCC=2.5V, Ideal value: RT=18.7Ω Commercial value: RT=18Ω</p>

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POWER CONSIDERATIONS

Driving LVPECL outputs requires an amount of power that can warm up the chip significantly.

The general requirement for the chip is that the junction temperature should not exceed +110°C.

The power consumption can be divided into two parts:

- 1) Core power dissipation
- 2) Output buffers power dissipation

CORE POWER DISSIPATION

The chip core power is equal to $VCC \times IEE$. With a worst case VCC and IEE the power dissipation in the core is $3.63V \times 65mA = 236mW$.

OUTPUT BUFFER POWER DISSIPATION

The output buffers are not exposed to the full VCC-VEE voltage. On the differential output, one line is at logic 1 with a small voltage across the buffer and a large output current. The other line is at logic 0 with a larger voltage across the buffer and a smaller output current. The power dissipation per output buffer is 32mW. Only buffers that are loaded will have power dissipation. With all 4 buffers loaded the worst case output buffer power dissipation will be 128mW.

Total Chip Power Dissipation, worst case, is $236mW + 128mW = 364mW$.

JUNCTION TEMPERATURE

How much the chip is warmed up from the power dissipation depends upon the thermal resistance from the chip to the environment, also known as "junction to ambient". The thermal resistance depends upon the type of package, how the package is assembled to the PCB and if there is additional air flow for improved cooling. For the LQFP package with use of the Thermal Relief pad, the thermal resistance is as follows:

TSSOP 20-pin Package	Air Flow Velocity in Linear Feet per Minute		
	0	200	500
JEDEC Standard Multi Layer PCB	$\theta_{JA} = 73^{\circ}C/W$	$\theta_{JA} = 67^{\circ}C/W$	$\theta_{JA} = 64^{\circ}C/W$

The temperature of the chip (junction) will be higher than the environment (ambient) with an amount equal to $\theta_{JA} \times$ Power. For an ambient temperature of +70°C, all outputs loaded and no air flow, the junction temperature $T_J = 70^{\circ}C + 73 \times 0.364 = 97^{\circ}C$.

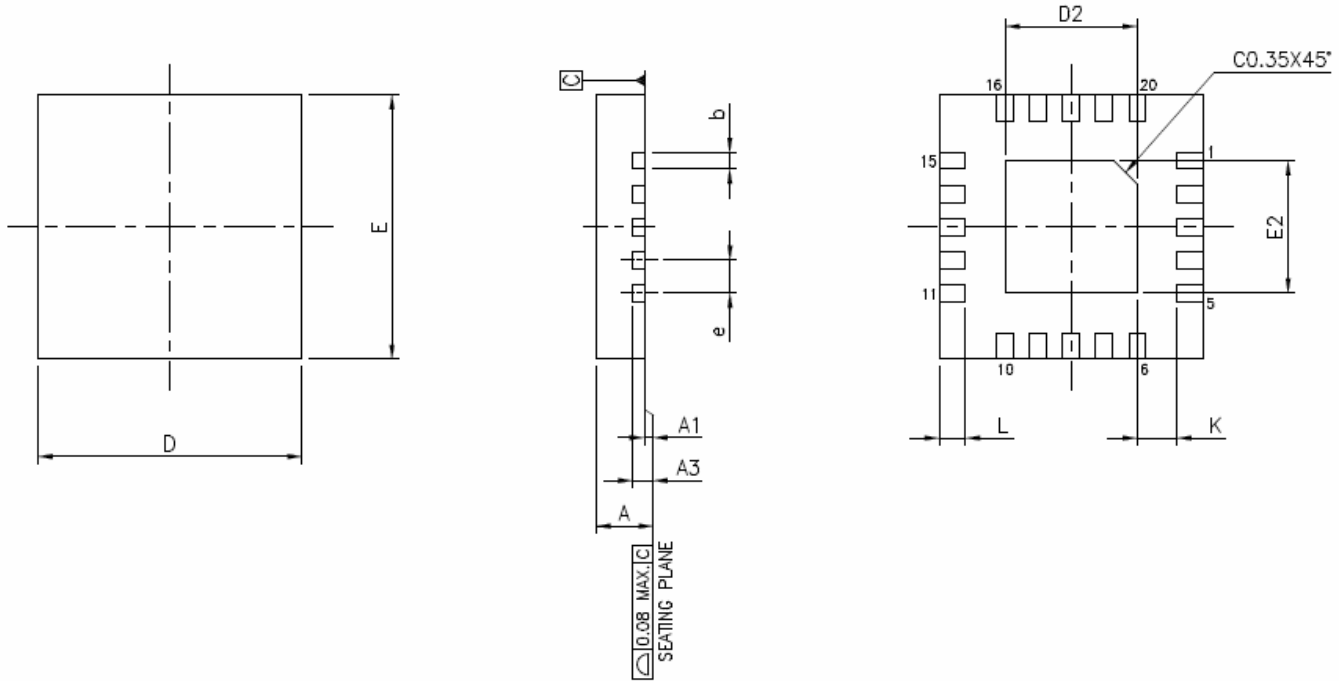
QFN 20-pin Package	Air Flow Velocity in Linear Feet per Minute		
	0	200	500
JEDEC Standard Multi Layer PCB	$\theta_{JA} = 60^{\circ}C/W$	$\theta_{JA} = 53^{\circ}C/W$	$\theta_{JA} = 46^{\circ}C/W$

The temperature of the chip (junction) will be higher than the environment (ambient) with an amount equal to $\theta_{JA} \times$ Power. For an ambient temperature of +85°C, all outputs loaded and no air flow, the junction temperature $T_J = 85^{\circ}C + 60 \times 0.364 = 107^{\circ}C$.

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PACKAGE DRAWING (GREEN PACKAGE COMPLIANT)

QFN 20L 4 X 4 mm



JEDEC OUTLINE	PACKAGE TYPE					
	MO-220			MO-220		
PKG CODE	WQFN(X420)			VQFN(Y420)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30
D	4.00 BSC			4.00 BSC		
E	4.00 BSC			4.00 BSC		
e	0.50 BSC			0.50 BSC		
K	0.20	—	—	0.20	—	—

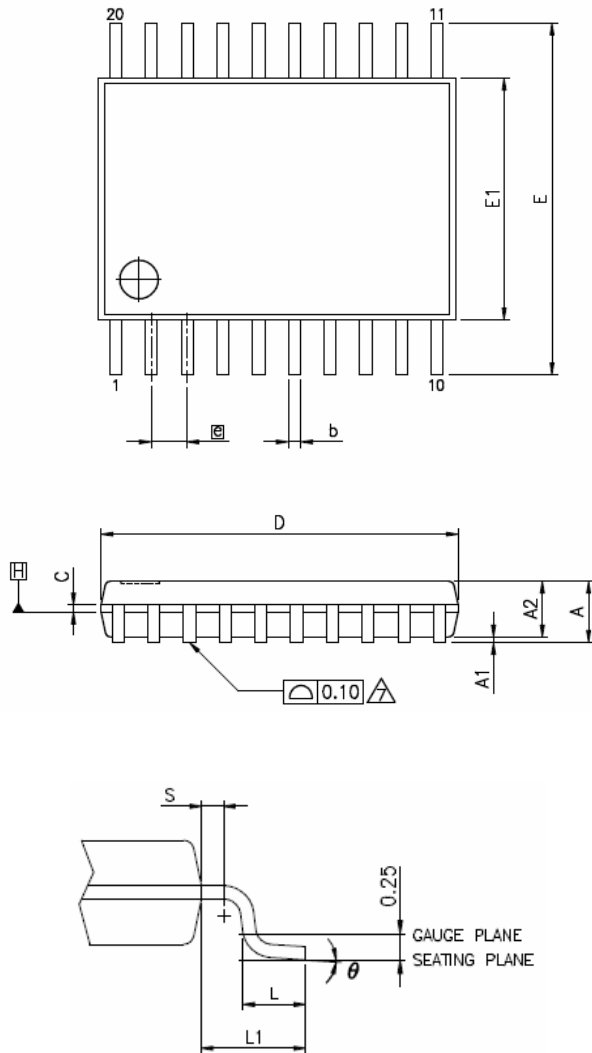
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION *b* APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION *b* SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	E2			D2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
114X114 MIL	1.90	2.00	2.05	1.90	2.00	2.05	0.30	0.40	0.50	V	V	W(V)GGD-1
102X102 MIL	2.00	2.10	2.15	2.00	2.10	2.15	0.45	0.55	0.65	X	V	W(V)GGD-1
110X110 MIL	2.40	2.50	2.55	2.40	2.50	2.55	0.35	0.45	0.55	V	X	W(V)GGD-11

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TSSOP173 20L



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.90	1.05
b	0.19	-	0.30
C	0.09	-	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	-	-
θ	0°	-	8°

NOTES:

- JEDEC OUTLINE :
STANDARD : MO-153 AC REV.F
THERMALLY ENHANCED : MO-153 ACT REV.F
- DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
- DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
- DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
- DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE \square .

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ORDERING INFORMATION (GREEN PACKAGE)

For part ordering, please contact our Sales Department:

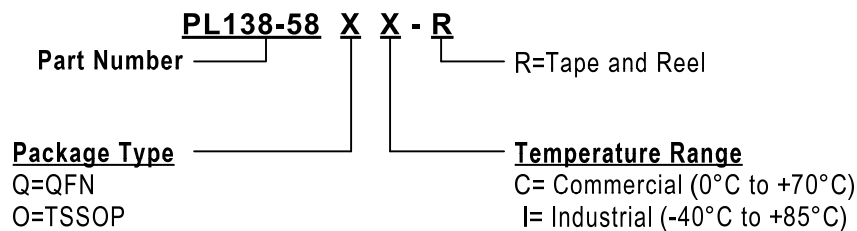
2880 Zanker Road, San Jose, CA 95134 USA

Tel (408) 571-1668 Fax (408) 571-1688

PART NUMBER

The order number for this device is a combination of the following:

Part number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option
PL138-58QC	P138 58 LLLLL	20-Pin QFN (Tube)
PL138-58OC	P138-58 OC LLLLL	20-Pin TSSOP (Tube)

*Note: LLLLL designates lot number

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Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf