0.5kHz-125MHz, MHz to KHz Programmable Clock™

FEATURES

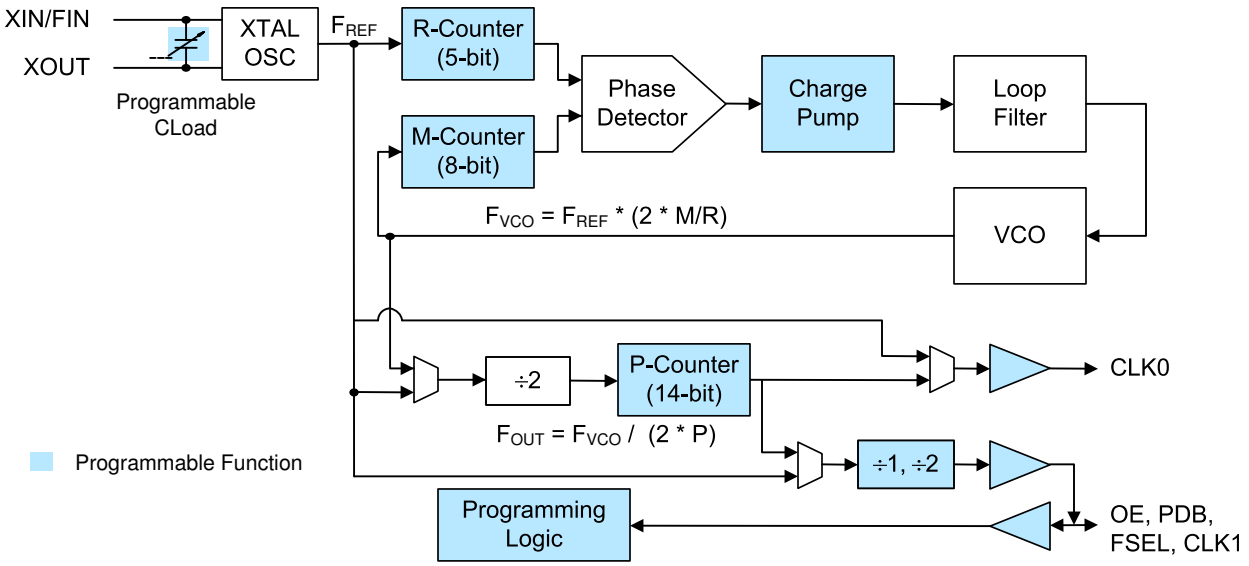
- Designed for Very Low-Power applications
- Accepts Crystal or Reference Clock inputs
- Input Frequency:
  - o Fundamental crystal: 10MHz to 50MHz
  - o Reference Input: 1MHz to 125MHz
- Accepts >0.1V reference signal input voltage
- Output Frequency 0.5kHz to 125MHz CMOS.
  - o 65MHz @ 1.8V operation
  - o 90MHz @ 2.5V operation
  - o 125MHz @ 3.3V operation
- One programmable I/O pin can be configured as OE, PDB, FSEL or CLK1
- Low current consumption:
  - o <1.0mA with 27MHz & 32kHz outputs
  - o < 5µA when PDB is activated
- Single 1.8V ~ 3.3V, ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin DFN, SOT23, and SC70 GREEN/RoHS compliant packages.

DESCRIPTION

The PL611s-18 is a low-cost general purpose frequency synthesizer and a member of PhaseLink's PicoPLL family, the worlds smallest programmable clocks. PhaseLink's PL611s-18 offers the versatility of using a single Crystal (MHz) or Reference Clock input and producing up to two (kHz/MHz) system clocks, or a combination of Reference and low frequency outputs. The PL611s-18 is designed for low-power applications with very stringent space requirements and consumes ~1.0mA, while producing 2 distinct outputs of 27MHz and 32kHz. The power down feature of PL611s-18, when activated, allows the IC to consume less than 5µA of power.

The PL611s-18 fits in a small DFN, SC70, or SOT23 package. Cascading of the PL611s-18 with other PhaseLink programmable clocks allow generating system level clocking requirements, thereby reducing the overall system implementation cost. In addition, one programmable I/O pin can be configured as Output Enable (OE), Frequency switching (FSEL), Power Down (PDB) input, or CLK1 (CLK0, FREF, FREF/2) output.

BLOCK DIAGRAM

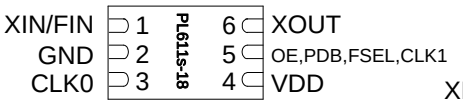


0.5kHz-125MHz, MHz to KHz Programmable Clock™

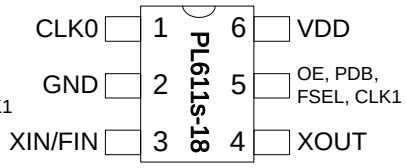
KEY PROGRAMMING PARAMETERS

CLK Output Frequency	Output Drive Strength	Programmable Input/Output
FOUT = FREF * M / (R * P) Where M=8 bit R= 5 bit P= 14 bit CLK0 = FOUT, FREF or FREF / (2*P) CLK1 = FREF, FREF/2, CLK0 or CLK0/2	Three optional drive strengths to choose from: • Low: 4mA • Std: 8mA (default) • High: 16mA	One output pin can be configured as: • OE - input • FSEL - input • PDB – input • CLK1 – output • Programmable CLoad

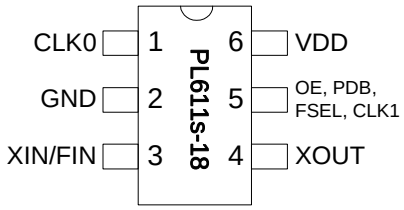
PACKAGE PIN CONFIGURATION AND ASSIGNMENT



DFN-6L
(2.0mmx1.3mmx0.6mm)



SC70-6L
(2.3mmx2.25mmx1.0mm)



SOT23-6L
(3.0mmx3.0mmx1.35mm)

Name	Pin Assignment			Type	Description
	DFN Pin #	SC70 Pin#	SOT Pin#		
XIN, FIN	1	3	3	I	Crystal or Reference input pin.
GND	2	2	2	P	GND connection
CLK0	3	1	1	O	Programmable Clock Output
VDD	4	6	6	P	VDD connection
OE, PDB, FSEL, CLK1	5	5	5	I/O	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB), Frequency Select input (FSEL) or CLK1 output. This pin has an internal 60KΩ pull up resistor on OE, PDB and FSEL.
XOUT	6	4	4	O	Crystal Output pin. Do Not Connect if FIN is used.

State	OE	PDB	FSEL
0	Tri-state CLK	Power Down Mode	Bank 0
1 (default)	Operating mode	Operating mode	Bank 1

FUNCTIONAL DESCRIPTION

PL611s-18 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-18 accepts a crystal input of 10MHz to 50MHz or a reference clock input of 1MHz to 125MHz and is capable of producing two outputs up to 125MHz. This flexible design allows the PL611s-18 to deliver any PLL generated frequency, FREF (Crystal or Ref Clk) frequency or FREF /(2*P) to CLK0 and/or CLK1. Some of the design features of the PL611s-18 are mentioned below:

PLL Programming

The PLL in the PL611s-18 is fully programmable. The PLL is equipped with a 5-bit input frequency divider (R-Counter), and an 8-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 14-bit post VCO divider (P-Counter). The output frequency is determined by the following formula [FOUT = FREF * M / (R * P)].

Clock Output (CLK0)

CLK0 is the main clock output. The PL611s-18 can also be programmed to provide a second clock output, CLK1, on the programmable I/O pin (see OE/PDB/FSEL/CLK1 pin description below). The output of CLK0 can be configured as the PLL output (F_{VCO}/(2*P)), FREF (Ref Clk Frequency) output, or FREF/(2*P) output. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The maximum output frequency is 125MHz.

Clock Output (CLK1)

The CLK1 feature allows the PL611s-18 to have an additional clock output. This output can be programmed to one of the following:

FREF
FREF / 2
CLK0
CLK0 / 2

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 60kΩ pull up resistor giving a default condition of logic “1”. Pulling the OE pin low “0” will tri-state the output buffers.

Power-Down Control (PDB)

The Power Down (PDB) feature allows the user to put the PL611s-18 into “Sleep Mode”. When activated (logic ‘0’), PDB ‘Disables the PLL, the oscillator circuitry, counters, and all other active circuitry and tri-state the output buffers. In Power Down mode the IC consumes <5µA of power. The PDB pin incorporates a pull up resistor giving a default condition of logic “1”.

Frequency Select (FSEL)

The Frequency Select (FSEL) feature allows the PL611s-18 to switch between two pre-programmed outputs allowing the device “On the Fly” frequency switching. The FSEL pin incorporates a 60kΩ pull up resistor giving a default condition of logic “1”.

Programmable CLoad

The PL611s-18 is equipped with programmable S-Caps to allow the Cload to be tuned from 8pF to 12pF.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic	I_{DD}	@ V_{DD} =3.3V, 27MHz Xtal input, F_{VCO}=81MHz, CLK0=32.768kHz, CLK1=27MHz, load=15pF		3.95		mA
Supply Current, Dynamic	I_{DD}	@ V_{DD} =2.5V, 27MHz Xtal input, F_{VCO}=81MHz, CLK0=32.768kHz, CLK1=27MHz, load=10pF		2.35		mA
Supply Current, Dynamic	I_{DD}	@ V_{DD} =1.8V, 27MHz Xtal input, F_{VCO}=81MHz, CLK0=32.768kHz, CLK1=27MHz, load=5pF		1.30		mA
PLL Off: Supply Current, Dynamic	I_{DD}	@ V_{DD} =3.3V, 27MHz Xtal input, CLK0=32.768kHz, CLK1=27MHz, load=15pF		2.75		mA
PLL Off: Supply Current, Dynamic	I_{DD}	@ V_{DD} =2.5V, , 27MHz Xtal input, CLK0=32.768kHz, CLK1=27MHz, load=10pF		1.3		mA
PLL Off: Supply Current, Dynamic	I_{DD}	@ V_{DD} =1.8V, , 27MHz Xtal input, CLK0=32.768kHz, CLK1=27MHz, load=5pF		0.9		mA
Supply Current, Dynamic	I_{DD}	When PDB=0			5	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Standard Drive	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Std Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

AC SPECIFICATIONS

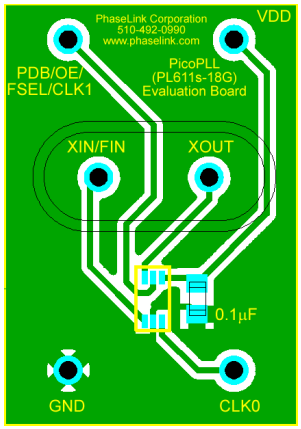
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency	Fundamental Crystal	10		50	MHz
Input (FIN) Frequency	@ V_{DD} =3.3V	1		125	MHz
	@ V_{DD} =2.5V			90	
	@ V_{DD} =1.8V			65	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V $\leq$50MHz, 2.5V $\leq$40MHz, 1.8V $\leq$15MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			125	MHz
	@ V_{DD} =2.5V			90	MHz
	@ V_{DD} =1.8V			65	MHz
Settling Time	At power-up (after V_{DD} increases over 1.62V)			2	ms
Output Enable Time	OE Function; Ta=25º C, 15pF Load. Add one clock period for a useable output.			10	ns
	PDB Function; Ta=25º C, 15pF Load			2	ms
VDD Sensitivity	Frequency vs. V_{DD} +/-10%	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V_{DD}, Std. Drive, 3.3V		2.0	3.0	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, Std. Drive, 3.3V		2.0	3.0	ns
Duty Cycle	V_{DD} /2	45	50	55	%
Period Jitter,Pk-to-Pk* (10,000 samples measured)	With capacitive decoupling between V_{DD} and GND.		70		ps

* Note: Jitter performance depends on the programming parameters.

CRYSTAL SPECIFICATIONS

PARAMETERS		SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		50	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)		$C_{L\ (xtal)}$	8		12	pF
Maximum Sustainable Drive Level					100	µW
Operating Drive Level				30		µW
Metal Can Crystal	Shunt Capacitance	C0			5.5	pF
	ESR Max	ESR			50	Ω
Small SMD Crystal	Shunt Capacitance	C0			2.5	pF
	ESR Max	ESR			80	Ω

PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION



DFN-6L Evaluation Board

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces(> 1 inch) as “striplines” or “microstrips” with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

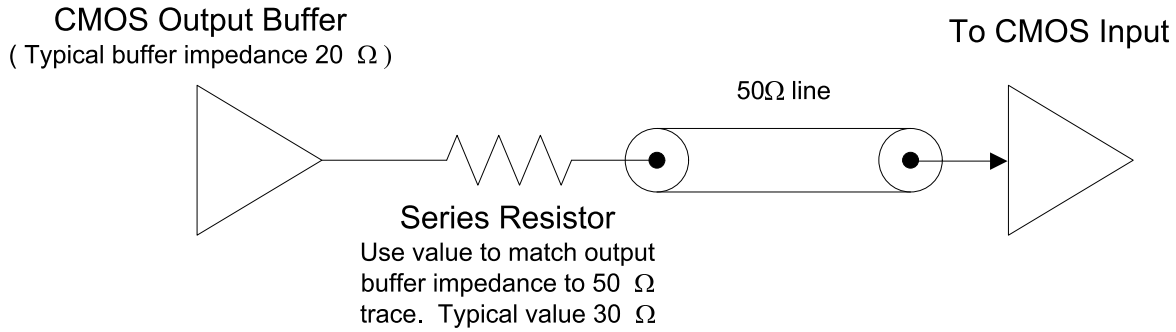
- Multiple VDD pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1µF for designs using crystals < 50MHz and 0.01µF for designs using crystals > 50MHz.

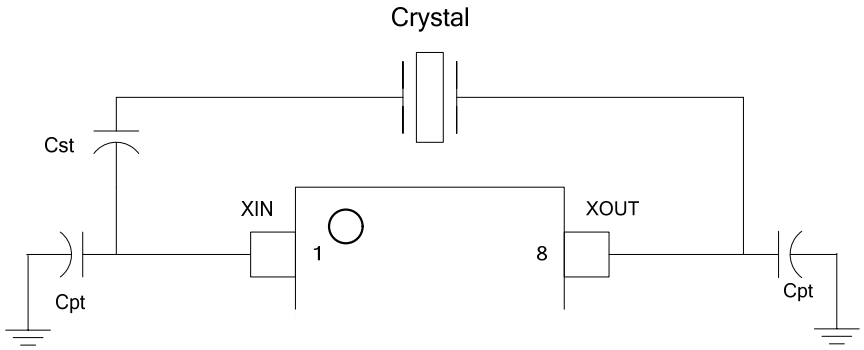
Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Crystal Tuning Circuit

Series and parallel capacitors used to fine tune the crystal load to the circuit load.



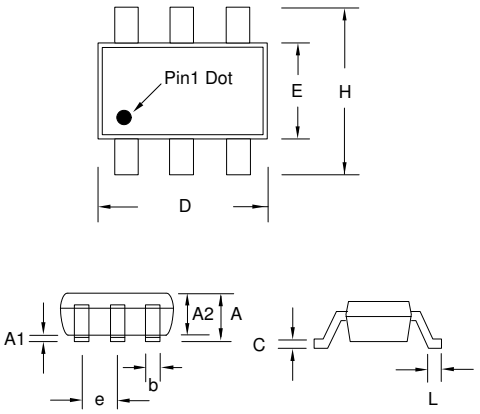
CST – Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator.

CPT – Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

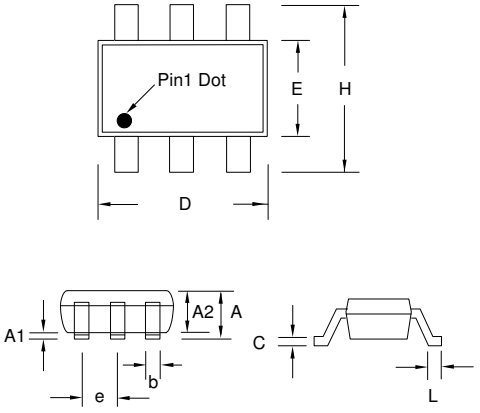
SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	



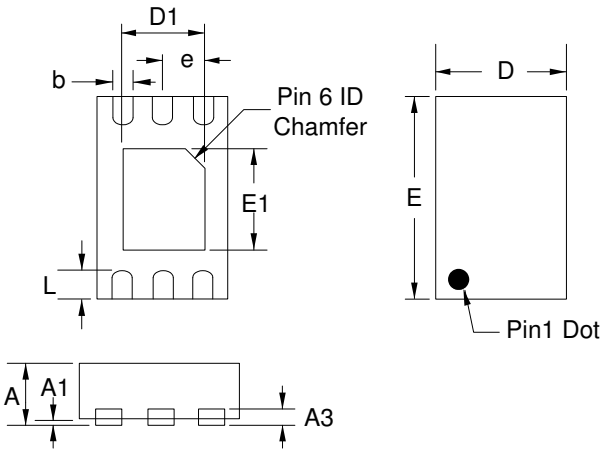
SC70-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.09
A2	0.80	0.91
b	0.15	0.30
c	0.08	0.25
D	1.85	2.25
E	1.15	1.35
H	2.00	2.30
L	0.21	0.41
e	0.65BSC	



DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30

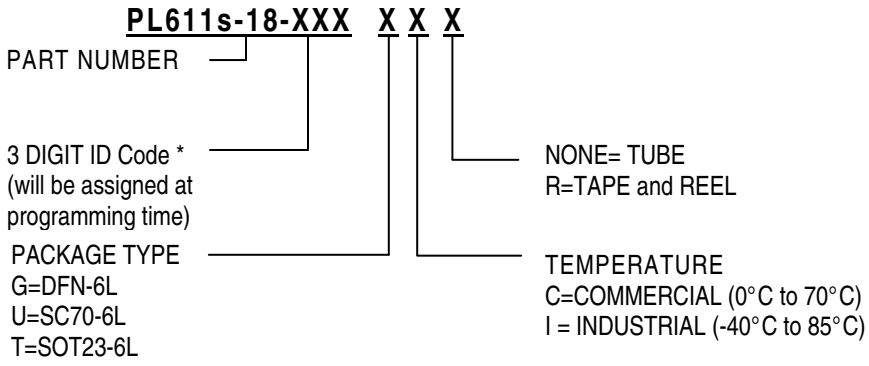


ORDERING INFORMATION (GREEN PACKAGE)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.

Part /Order Number	Marking†	Package Option
PL611s-18-XXXGC-R	XXX	6-Pin DFN (Tape and Reel)
PL611s-18-XXXUC-R	XXX	6-Pin SC70 (Tape and Reel)
PL611s-18-XXXTC-R	18XXX	6-Pin SOT23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that, at times, could be independent of the part number.
Please consult your PhaseLink sales representative for marking information.

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf