

**1.8V-3.3V PicoPLL™, World's Smallest Programmable Clock**

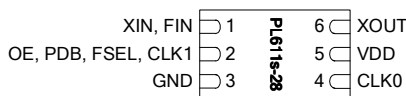
**FEATURES**

- Designed for Very Low-Power applications
- Input Frequency:
  - Fundamental Crystal: 10MHz to 50MHz
  - Reference Input: 1MHz to 200MHz
- Accepts >0.1V reference signal input voltage
- Output Frequency:
  - ≤65MHz @ 1.8V operation
  - ≤90MHz @ 2.5V operation
  - ≤125MHz @ 3.3V operation
- Disabled outputs programmable as HiZ or Active Low.
- Low current consumption:
  - < 1.2mA @ 27MHz
  - < 5µA when PDB is activated
- Single 1.8V to 3.3V, ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin DFN, SOT23, and SC70 GREEN/RoHS compliant packages.

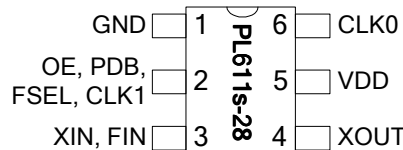
**DESCRIPTION**

The PL611s-28 consumes very low-power while producing high performance clock outputs of up to 125MHz. Designed for low-power applications with very stringent space requirement, PL611s-28 consumes about 1.2mA, while producing 2 distinct outputs of 27MHz and 13.5MHz. Designed to fit in a small SOT23, SC70, or DFN package for high performance applications, the PL611s-28 offers the best phase noise and jitter performance, and power consumption of its rivals. The power down feature of PL611s-28, when activated, allows the IC to consume less than 5µA of power, while its programming flexibility allows generating any output, using a low-cost crystal or reference input. In addition, one programmable I/O pin can be configured as Output Enable (OE), Frequency switching (FSEL), Power Down (PDB) input, or CLK1 (FOUT, FREF, FREF/2) output.

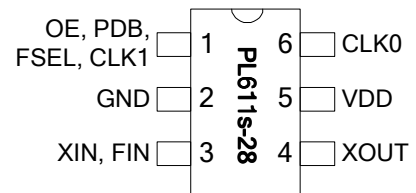
**PACKAGE PIN CONFIGURATION**



**DFN-6L**  
(2.0 x 1.3 x 0.6mm)

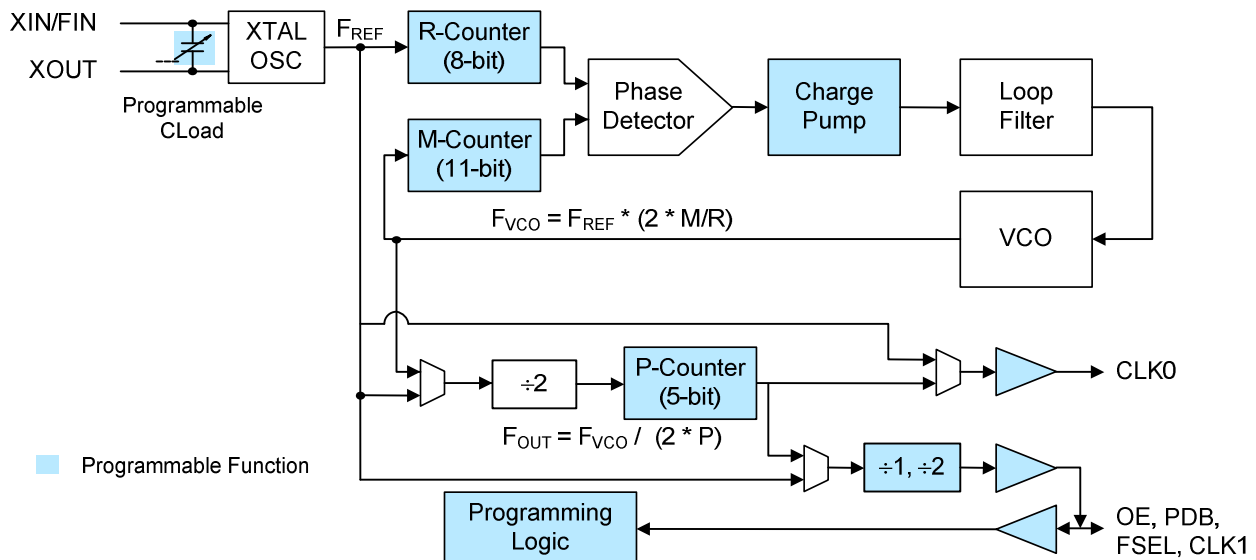


**SC70-6L**  
(2.3 x 2.25 x 1.0mm)



**SOT23-6L**  
(3.0 x 3.0 x 1.35mm)

**BLOCK DIAGRAM**



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### KEY PROGRAMMING PARAMETERS

CLK[0:1] Output Frequency	Output Drive Strength	Programmable Input/Output
$F_{OUT} = F_{REF} * M / (R * P)$ Where M = 11 bit R = 8 bit P = 5 bit $CLK0 = F_{OUT}, F_{REF}$ or $F_{REF} / (2 * P)$ $CLK1 = F_{REF}, F_{REF}/2, CLK0$ or $CLK0/2$	Three optional drive strengths to choose from: <ul style="list-style-type: none"> <li>• Low: 4mA</li> <li>• Std: 8mA (default)</li> <li>• High: 16mA</li> </ul>	One output pin can be configured as: <ul style="list-style-type: none"> <li>• OE - input</li> <li>• PDB - input</li> <li>• FSEL – input</li> <li>• Clock - output</li> <li>• HiZ or Active Low disabled state</li> </ul>

### PACKAGE PIN ASSIGNMENT

Name	Pin Assignment			Type	Description												
	SOT Pin #	SC70 Pin#	DFN Pin#														
OE, PDB, FSEL, CLK1	1	2	2	I/O	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down (PDB) input, On-the-Fly Frequency Switching Selector (FSEL) input or CLK1 clock output. This pin has an internal 60KΩ pull up resistor (OE, PDB & FSEL Only). <table border="1" data-bbox="662 1108 1479 1272"> <thead> <tr> <th>State</th> <th>OE</th> <th>PDB</th> <th>FSEL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable CLK</td> <td>Power Down Mode</td> <td>Bank 1</td> </tr> <tr> <td>1 (default)</td> <td>Normal mode</td> <td>Normal mode</td> <td>Bank 2</td> </tr> </tbody> </table>	State	OE	PDB	FSEL	0	Disable CLK	Power Down Mode	Bank 1	1 (default)	Normal mode	Normal mode	Bank 2
State	OE	PDB	FSEL														
0	Disable CLK	Power Down Mode	Bank 1														
1 (default)	Normal mode	Normal mode	Bank 2														
GND	2	1	3	P	GND connection												
XIN, FIN	3	3	1	I	Crystal or Reference input pin												
XOUT	4	4	6	O	Crystal Output pin Do Not Connect (DNC) when FIN is present												
VDD	5	5	5	P	VDD connection												
CLK0	6	6	4	O	Programmable Clock Output												

**1.8V-3.3V PicoPLL™, World's Smallest Programmable Clock****FUNCTIONAL DESCRIPTION**

The PL611s-28 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-28 accepts a fundamental input crystal of 10MHz to 50MHz or reference clock input of 1MHz to 200MHz and is capable of producing two outputs up to 125MHz. This flexible design allows the PL611s-28 to deliver any PLL generated frequency,  $F_{REF}$  (Crystal or Ref Clk) frequency or  $F_{REF}/(2*P)$  to CLK0 and/or CLK1. Some of the design features of the PL611s-28 are mentioned below:

**PLL Programming**

The PLL in the PL611s-28 is fully programmable. The PLL is equipped with an 8-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 5-bit post VCO divider (P-Counter). The output frequency is determined by the following formula [ $F_{OUT} = F_{REF} * M / (R * P)$ ].

**Clock Output (CLK0)**

CLK0 is the main clock output. The output of CLK0 can be configured as the PLL output ( $F_{VCO}/(2*P)$ ),  $F_{REF}$  (Crystal or Ref Clk Frequency) output, or  $F_{REF}/(2*P)$  output.

**Clock Output (CLK1)**

The CLK1 feature allows the PL611s-28 to have an additional clock output. This output can be programmed to one of the following:

- $F_{REF}$  - Reference (Crystal or Ref Clk) Frequency
- $F_{REF} / 2$
- CLK0
- CLK0 / 2

The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA) for each clock, independently.

**Output Enable (OE)**

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 60k $\Omega$  pull up resistor giving a default condition of logic "1".

**Power-Down Control (PDB)**

The Power Down (PDB) feature allows the user to put the PL611s-28 into "Sleep Mode". When activated (logic '0'), PDB 'Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <5 $\mu$ A of power. The PDB pin incorporates a 60k $\Omega$  pull up resistor giving a default condition of logic "1".

**Frequency Select (FSEL)**

The Frequency Select (FSEL) feature allows the PL611s-28 to switch between two pre-programmed outputs allowing the device "On the Fly" frequency switching. The FSEL pin incorporates a 60k $\Omega$  pull up resistor giving a default condition of logic "1".

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## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage Range	$V_{DD}$	-0.5	4.6	V
Input Voltage Range	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage Range	$V_O$	-0.5	$V_{DD}+0.5$	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. \*Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

### DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic	$I_{DD}$	$V_{DD} = 3.3V, 27MHz,$ load=15pF		3.7		mA
		$V_{DD} = 2.5V, 27MHz,$ load=10pF		2.3		
		$V_{DD} = 1.8V, 27MHz,$ load=5pF		1.3		
PLL Off: Supply Current, Dynamic	$I_{DD}$	$V_{DD} = 3.3V, 27MHz,$ load=15pF		3.4		mA
		$V_{DD} = 2.5V, 27MHz,$ load=10pF		1.9		
		$V_{DD} = 1.8V, 27MHz,$ load=5pF		1		
Supply Current, Dynamic	$I_{DD}$	When PDB=0			5	μA
Operating Voltage	$V_{DD}$		1.62		3.63	V
Power Supply Ramp	$t_{PU}$	Time for $V_{DD}$ to reach 90% $V_{DD}$ . Power ramp must be monotonic.			100	ms
Output Low Voltage	$V_{OL}$	$I_{OL} = +4mA$ Standard Drive			0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = -4mA$ Standard Drive	$V_{DD} - 0.4$			V
Output Current, Low Drive	$I_{OSD}$	$V_{OL} = 0.4V, V_{OH} = 2.4V$	4			mA
Output Current, Standard Drive	$I_{OSD}$	$V_{OL} = 0.4V, V_{OH} = 2.4V$	8			mA
Output Current, High Drive	$I_{OHD}$	$V_{OL} = 0.4V, V_{OH} = 2.4V$	16			mA

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### AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Input Frequency (XIN)	Fundamental Crystal	10		50	MHz
Input (FIN) Frequency	@ V <sub>DD</sub> =3.3V	1		200	MHz
	@ V <sub>DD</sub> =2.5V			166	
	@ V <sub>DD</sub> =1.8V			133	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V <sub>DD</sub>	V <sub>pp</sub>
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz, 1.8V ≤15MHz	0.1		V <sub>DD</sub>	V <sub>pp</sub>
Output Frequency	@ V <sub>DD</sub> =3.3V	1		125	MHz
	@ V <sub>DD</sub> =2.5V			90	MHz
	@ V <sub>DD</sub> =1.8V			65	MHz
Settling Time	At power-up (after V <sub>DD</sub> increases over 1.62V)			2	ms
Output Enable Time	OE Function; Ta=25° C, 15pF Load. Add one clock period to this measurement for a usable clock output.			10	ns
	PDB Function; Ta=25° C, 15pF Load			2	ms
VDD Sensitivity	Frequency vs. V <sub>DD</sub> +/-10%	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V <sub>DD</sub> , High Drive, 3.3V		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V <sub>DD</sub> , High Drive, 3.3V		1.2	1.7	ns
Duty Cycle	V <sub>DD</sub> / 2	45	50	55	%
Period Jitter,Pk-to-Pk* (10,000 samples measured)	With capacitive decoupling between V <sub>DD</sub> and GND		70		ps

\* Note: Jitter performance depends on the programming parameters.

### CRYSTAL SPECIFICATIONS

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
Fundamental Crystal Resonator Frequency	F <sub>XIN</sub>	10		50	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range)	C <sub>L(xtal)</sub>	8		12	pF
Maximum Sustainable Drive Level				100	μW
Operating Drive Level			30		μW
Metal Can Crystal	Shunt Capacitance	C <sub>0</sub>		5.5	pF
	ESR Max	ESR		50	Ω
Small SMD Crystal	Shunt Capacitance	C <sub>0</sub>		2.5	pF
	ESR Max	ESR		80	Ω

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**LAYOUT RECOMMENDATIONS**

The following guidelines are to assist you with a performance optimized PCB design:

**Signal Integrity and Termination Considerations**

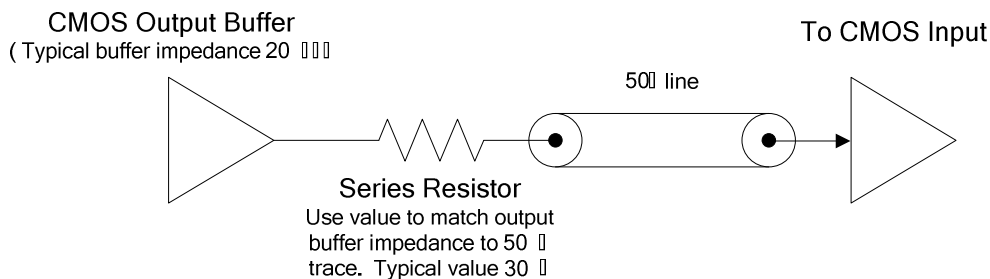
- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections ( looks like ringing ).
- Design long traces ( > 1 inch ) as "striplines" or "microstrips" with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

**Decoupling and Power Supply Considerations**

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Multiple VDD pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1µF for designs using frequencies < 50MHz and 0.01µF for designs using frequencies > 50MHz.

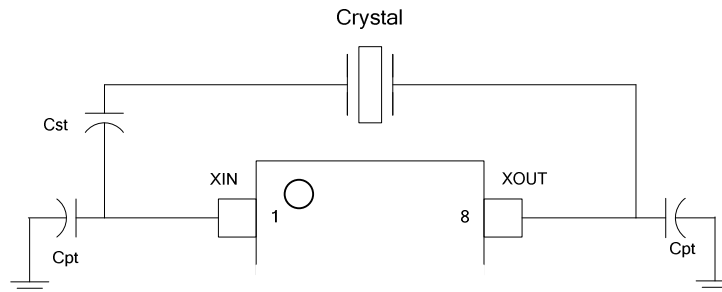
**Typical CMOS termination**

Place Series Resistor as close as possible to CMOS output



**Crystal Tuning Circuit**

Series and parallel capacitors used to fine tune the crystal load to the circuit load.



**CST** - Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator.

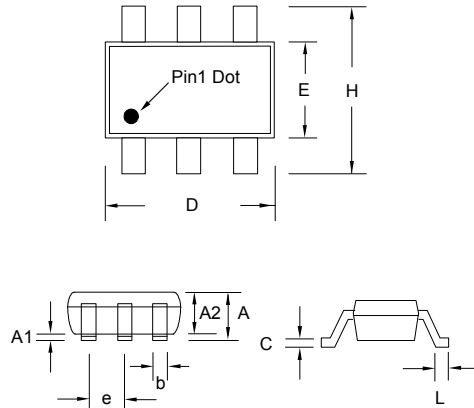
**CPT** - Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

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**PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)**

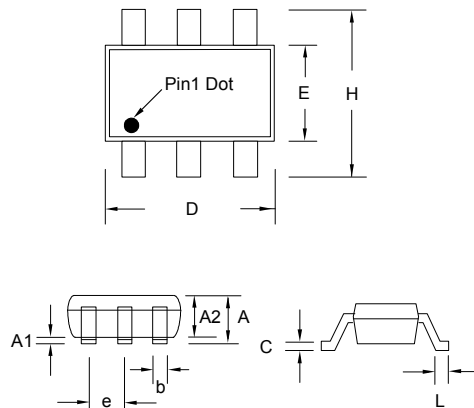
**SOT23-6L**

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.00
L	0.35	0.55
e	0.95 BSC	



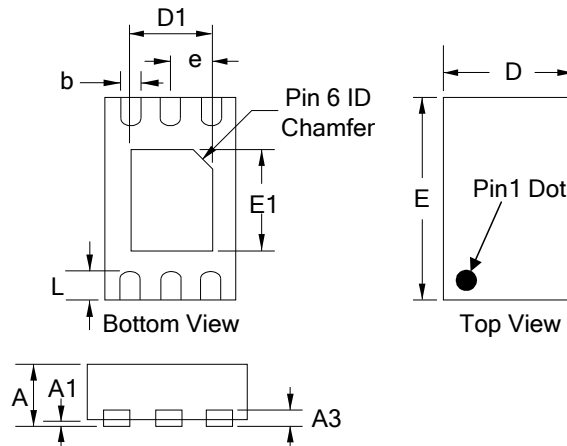
**SC70-6L**

Symbol	Dimension in MM	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.09
A2	0.80	0.91
b	0.15	0.30
c	0.08	0.25
D	1.85	2.25
E	1.15	1.35
H	2.00	2.30
L	0.21	0.41
e	0.65BSC	



**DFN-6L**

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30



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**ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)**

*For part ordering, please contact our Sales Department:*

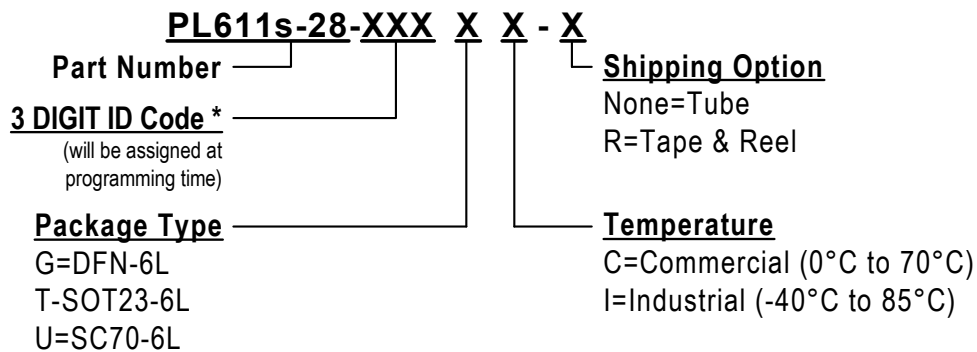
2880 Zanker Road, San Jose, CA 95134, USA

Tel: (408) 571-1668 Fax: (408) 571-1688

**PART NUMBER**

The order number for this device is a combination of the following:

Part number, Package type and Operating temperature range



\* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.

Part/Order Number	Marking†	Package Option
PL611s-28-XXXGC-R	XXX LLL	6-Pin DFN (Tape and Reel)
PL611s-28-XXXUC-R	XXX LLL	6-Pin SC70 (Tape and Reel)
PL611s-28-XXXTC-R	28XXX LLL	6-Pin SOT23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that, at times, could be independent of the part number. Please consult your PhaseLink sales representative for marking information.

\* LLL designates lot number

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Solder reflow profile available at [www.phaselink.com/QA/solderingGreen.pdf](http://www.phaselink.com/QA/solderingGreen.pdf)