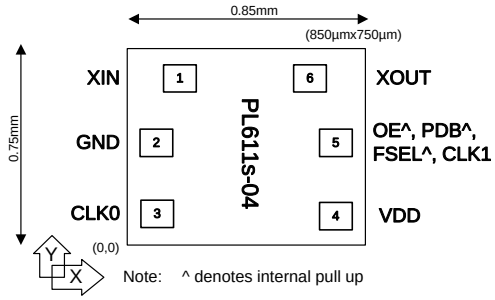
1.8V-3.3V PicoPLL™ Programmable Quick Turn Clock™

FEATURES

- Advanced One Time Programmable PLL design.
- Programmable PLL or Direct Oscillation operation.
- Very low Jitter (30-70ps Pk-Pk typical)
- Output Frequency range
  - o ≤110MHz @ 1.8V operation
  - o ≤166MHz @ 2.5V operation
  - o ≤200MHz @ 3.3V operation
- Input Frequency: Fundamental crystal
  - o 10MHz to 50MHz.
- 8bit Switch Capacitor for crystal CLoad tuning
  - o 8pF to 12pF
- Low current consumption, <10µA when PDB is activated.
- One programmable I/O pin can be configured as Output Enable (OE) input, Power Down (PDB) input, Frequency Select (FSEL) input or 2nd clock output.
- Single 1.8V, 2.5V, or 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 12 mil to 6 mil thickness

PAD CONFIGURATION



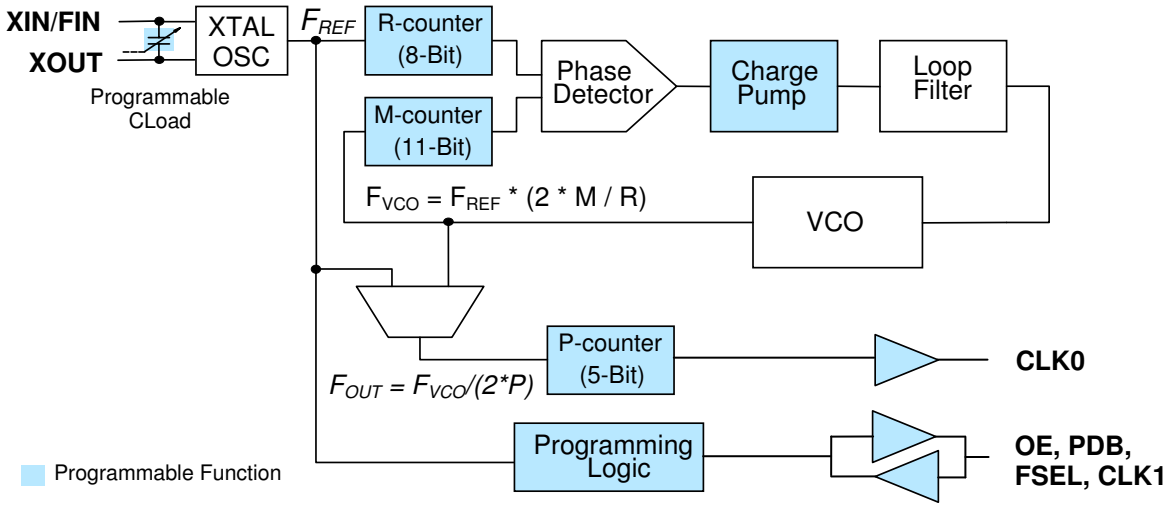
DIE SPECIFICATION

Parameter	Value
Chip size	0.75 x 0.85mm
Chip thickness	Optional (See Ordering Information)
PAD size	90µm
Chip Base	GND level

DESCRIPTION

The PL611s-04 is a high performance low-cost general purpose frequency synthesizer and a member of PhaseLink's PicoPLL™ Factory Programmable 'Quick Turn Clock (QTC)'. Designed to fit in a small 2.5mmx2.0mm oscillator module for high performance applications, the PL611s offers the best phase noise and jitter performance, smallest die size, and power consumption of any comparable device. The power down feature of PL611s, when activated, allows the IC to consume less than 10µA of power, while its programming flexibility allows generating any output, using a low-cost crystal input.

BLOCK DIAGRAM



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KEY PROGRAMMING PARAMETERS

Output Frequency	Output Drive Strength	Crystal Load	Programmable Input/Output	Charge-Pump Current
CLK0 PLL Mode : CLK0 = F_{IN} * M / (R * P) Where: • M=11 bit • R= 8 bit • P= 5 bit P is an Odd/Even Divider Direct Oscillation Mode: CLK0 = F_{IN} or F_{IN} /(2*P) **CLK1** = F_{IN}, F_{IN}/2, CLK0 or CLK0/2	Three optional drives to choose from. They are: • Low: 4mA • Std: 8mA (default) • High: 16mA	Programmable CLoad Tuning • 8pF to 12pF • ±50ppm typical	One pad can be configured as: • OE – input • PDB – input • FSEL – input • CLK1 – output	Charge pump current • 4 levels; programmable

PAD ASSIGNMENT AND DESCRIPTION (PL611s-04)

Name	Pad Assignment*			Type	Description
	Pad #	X (µm)	Y (µm)		
XIN	1	125	665	I	Crystal Input pad
GND	2	85	375	P	GND connection
CLK0	3	85	115	O	Programmable Clock Output
VDD	4	765	115	P	VDD connection
OE, PDB, FSEL, CLK1	5	765	375	B	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB), Frequency Select (FSEL) input or CLK1 clock output.
XOUT	6	725	665	O	Crystal Output pad

State	OE	PDB	FSEL
0	Tri-state CLK0	Power Down Mode Tri-state CLK0	Bank 0
1 (default)	Operating mode	Operating mode	Bank 1

* Note: The X/Y coordinates indicate pad centers.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency (XIN)	Fundamental Crystal	10		50	MHz
Output Frequency	@ V_{DD} = 3.3V			200	MHz
	@ V_{DD} = 2.5V			166	
	@ V_{DD} = 1.8V			110	
Settling Time	At power-up (after $V_{DD} \geq$ 1.62V)			2	ms
Output Enable Time (See MTC-1)	OE Function; Ta=25º C, 15pF Load. Add one clock period to this measurement for a usable clock output.			10	ns
	PDB Function; Ta=25º C, 15pF Load			2	ms
Output Disable Time (See MTC-1)	Ta=25º C, 15pF Load			100	ns
VDD Sensitivity	Frequency vs. V_{DD} +/-10%	-2		2	ppm
Output Rise Time (See MTC-1)	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1	1.2	ns
Output Fall Time (See MTC-1)	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1	1.2	ns
Duty Cycle (See MTC-1)	@2.5V and 3.3V over entire frequency range, $V_{DD}/2$	45	50	55	%
	@1.8V, $\leq$ 75MHz F_{OUT}, $V_{DD}/2$	45	50	55	
	@1.8V, 75MHz < $F_{OUT} \leq$110MHz	40		60	
Period Jitter, Pk-to-Pk* (10,000 samples measured) (See MTC-3)	With capacitive decoupling between V_{DD} and GND.		70		ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

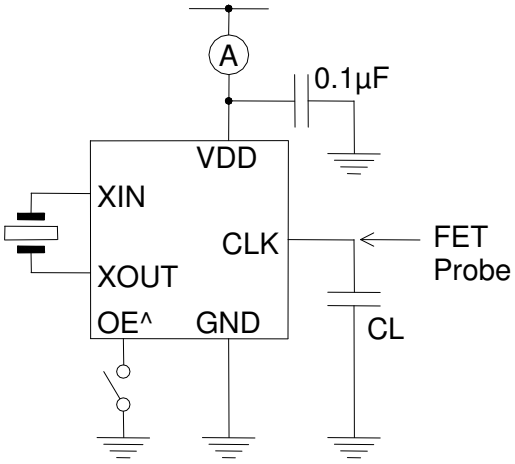
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, Loaded Output	I_{DD}	@ V_{DD} =3.3V, 30MHz, load=15pF		6.0		mA
Supply Current, Dynamic, Loaded Output	I_{DD}	@ V_{DD} =2.5V, 30MHz, load=15pF		3.9		mA
Supply Current, Dynamic, Loaded Output	I_{DD}	@ V_{DD} =1.8V, 30MHz, load=5pF		2.1		mA
PLL Off: Supply Current, Dynamic, Loaded Output	I_{DD}	@ V_{DD} =3.3V, 30MHz, load=15pF		2.0		mA
PLL Off: Supply Current, Dynamic, Loaded Output	I_{DD}	@ V_{DD} =2.5V, 30MHz, load=15pF		1.6		mA
PLL Off: Supply Current, Dynamic, Loaded Output	I_{DD}	@ V_{DD} =1.8V, 30MHz, load=5pF		0.8		mA
Stand By Current, Loaded Outputs (See MTC-1)	I_{DD}	When PDB=0			<10	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Standard Drive	V_{DD} – 0.4			V
Output Current, Low Drive (See MCT-2)	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V Operation	4			mA
Output Current, Standard Drive (See MCT-2)	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V Operation	8			mA
Output Current, High Drive (See MCT-2)	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V, 3.3V Operation	16			mA

CRYSTAL SPECIFICATIONS

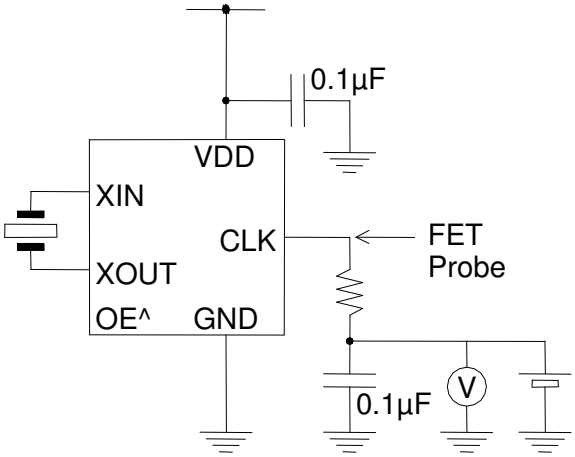
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	F_{XIN}	10		50	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L\ (xtal)}$	8		12	pF
Maximum Sustainable Drive Level				100	µW
Operating Drive Level			30		µW
Crystal Shunt Capacitance	C0			4	pF
Effective Series Resistance, Fundamental, 10 - 50MHz (See MCT-4)	ESR			30	Ω

MEASUREMENT TEST CIRCUITS (MTC)

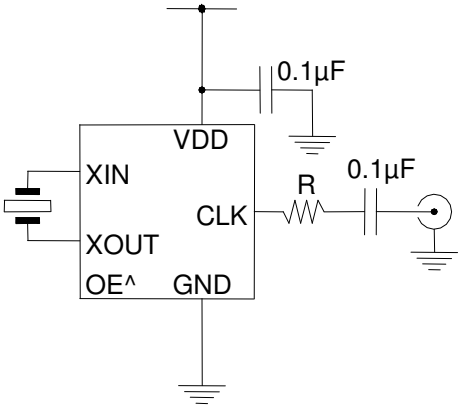
MTC-1: Rise Time, Fall Time, Duty Cycle, VOL, VOH, I_{dd}, Power Down Current, Output Enable/Disable



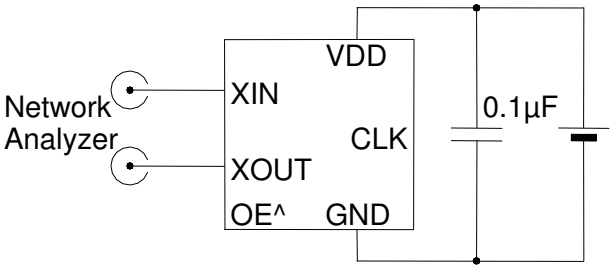
MTC-2: Output Drive Current and Output Impedance



MTC-3: Jitter and Phase Noise

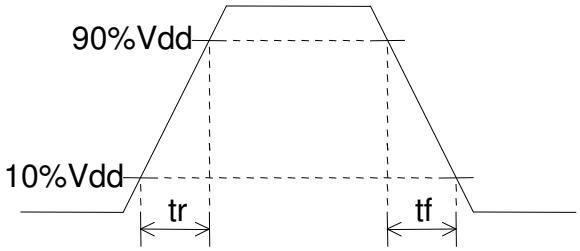


MTC-4: Negative Resistance

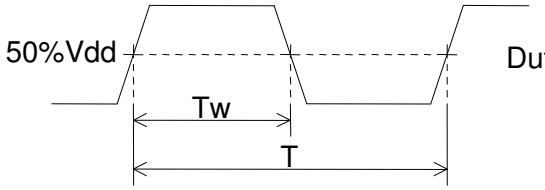


WAVEFORM SWITCHING CHARACTERISTICS

Rise and Fall times:

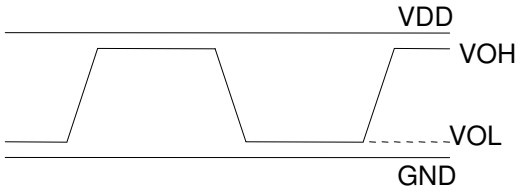


Duty Cycle:



$$\text{Duty Cycle} = 100\% \times \frac{Tw}{T}$$

VOH, VOL:



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ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL611s-04 X X X

Part Number

Temperature Range
C=Commercial (0°C to 70°C)

Package Type
D = Die
E = Die (with Non-Conductive Backcoating)
V = Wafer (with Non-Conductive Backcoating)
W = Wafer

Thickness
6 = 6 Mil (Available in Die only)
8 = 8 Mil
A = 10 Mil
Blank = 12 Mil

Part / Order Number	Marking	Package Option	Temperature
PL611s-04DxC	P611s-04DxC	Die (Waffle Pack)	0°C to +70°C
PL611s-04ExC	P611s-04ExC	Die (Waffle Pack)	0°C to +70°C
PL611s-04VxC	P611s-04VxC	Wafer	0°C to +70°C
PL611s-04WxC	P611s-04WxC	Wafer	0°C to +70°C