1.8V-3.3V PicoPLL™, World's Smallest Programmable Clock

FEATURES

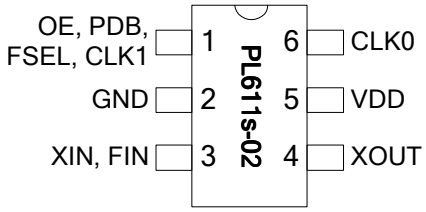
- Lowest-power, smallest Programmable PLL
- Very low Jitter and Phase Noise
- Output Frequency up to:
  - 110MHz @ 1.8V operation
  - 166MHz @ 2.5V operation
  - 200MHz @ 3.3V operation
- Input Frequency:
  - Fundamental Crystal: 10MHz to 50MHz
  - Reference Clock: 1MHz to 200MHz
- Accepts ≥0.1V reference signal input voltage
- One I/O pin can be configured as Output Enable (OE), Frequency switching (FSEL), Power Down (PDB) input, or CLK1 output.
- <10µA current consumption with PDB active.
- Single 1.8V to 3.3V, ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin DFN and SOT23 GREEN/RoHS compliant packages.

DESCRIPTION

The PL611s-02 is a low-power, small form factor, high performance OTP-base programmable frequency synthesizer and a member of PhaseLink's PicoPLL Factory Programmable 'Quick Turn Clocks. Designed to fit in a small DFN or SOT23 package for a broad range of applications, the PL611s-02 offers the best phase noise and jitter performance, and power consumption of its rivals. . In addition, one programmable I/O pin can be configured as Output Enable (OE), Frequency switching (FSEL), Power Down (PDB) input, or CLK1 (FOUT, FREF, FREF/2) output. The power down feature of PL611s-02, when activated, allows the IC to consume less than 10µA of power, while its programming flexibility allows generating any output, up to 200MHz using a low-cost crystal or reference input.

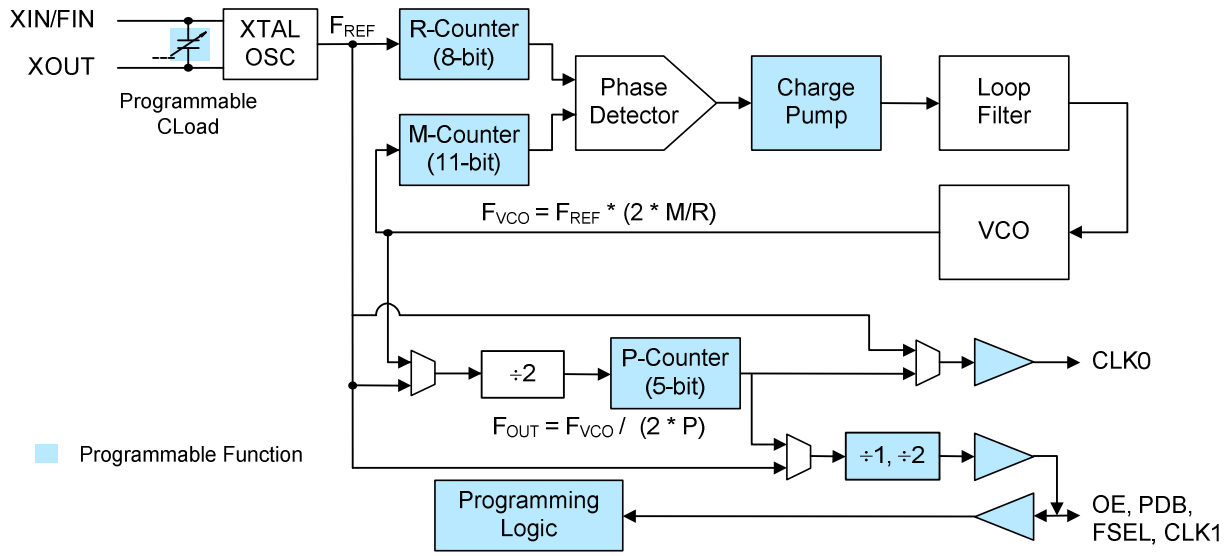
PACKAGE PIN CONFIGURATION

DFN-6L
(2.0 x 1.3 x 0.6mm)



SOT23-6L
(3.0 x 3.0 x 1.35mm)

BLOCK DIAGRAM



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KEY PROGRAMMING PARAMETERS

CLK[0:1] Output Frequency	Output Drive Strength	Programmable Input/Output
$F_{OUT} = F_{REF} * M / (R * P)$ Where M = 11 bit R = 8 bit P = 5 bit CLK0 = F_{OUT}, F_{REF} or $F_{REF} / (2*P)$ CLK1 = F_{REF}, $F_{REF}/2$, CLK0 or CLK0/2	Three optional drive strengths to choose from: • Low: 4mA • Std: 8mA (default) • High: 16mA	One output pin can be configured as: • OE - input • PDB - input • FSEL - input • CLK1 – output

PACKAGE PIN ASSIGNMENT

Name	Pin Assignment SOT23 Pin #	Pin Assignment DFN Pin#	Type	Description
OE, PDB, FSEL, CLK1	1	2	I/O	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB), On-the-Fly Frequency Switching Selector (FSEL), or CLK1 clock output This pin has an internal 60KΩ pull up resistor for OE, PDB & FSEL.
GND	2	3	P	GND connection
XIN, FIN	3	1	I	Crystal or Reference Clock input pin
XOUT	4	6	O	Crystal Output pin Do Not Connect (DNC) when FIN is present
VDD	5	5	P	VDD connection
CLK0	6	4	O	Programmable Clock Output

State	OE	PDB	FSEL
0	Tri-State CLK	Power Down Mode	Bank 1
1 (default)	Normal mode	Normal mode	Bank 2

FUNCTIONAL DESCRIPTION

PL611s-02 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-02 accepts a fundamental input crystal of 10MHz to 50MHz or reference clock input of 1MHz to 200MHz and is capable of producing two outputs up to 200MHz. This flexible design allows the PL611s-02 to deliver any PLL generated frequency, FREF (Crystal or Ref Clk) frequency or FREF /(2*P) to CLK0 and/or CLK1. Some of the design features of the PL611s-02 are mentioned below:

PLL Programming

The PLL in the PL611s-02 is fully programmable. The PLL is equipped with an 8-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 5-bit post VCO divider (P-Counter). The output frequency is determined by the following formula [FOUT = FREF * M / (R * P)].

Clock Output (CLK0)

CLK0 is the main clock output. The output of CLK0 can be configured as the PLL output (FVCO/(2*P)), FREF (Crystal or Ref Clk) output, or FREF/(2*P) output. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The maximum output frequency is determined by the Power Supply Voltage; 200MHz at 3.3V, 166MHz at 2.5V and 110MHz at 1.8V.

Clock Output (CLK1)

The CLK1 feature allows the PL611s-02 to have an additional clock output programmed to one of the following:

FREF - Reference (Crystal or Ref Clk) Frequency
FREF / 2
CLK0
CLK0 / 2

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 60kΩ pull up resistor giving a default condition of logic "1".

Power-Down Control (PDB)

The Power Down (PDB) feature allows the user to put the PL611s-02 into "Sleep Mode". When activated (logic '0'), PDB 'Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10µA of power. The PDB pin incorporates a 60kΩ pull up resistor giving a default condition of logic "1".

Frequency Select (FSEL)

The Frequency Select (FSEL) feature allows the PL611s-02 to switch between two pre-programmed outputs allowing the device "On the Fly" frequency switching. The FSEL pin incorporates a 60kΩ pull up resistor giving a default condition of logic "1".

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic	I_{DD}	V_{DD} =3.3V,30MHz, load=15pF		6.0		mA
Supply Current, Dynamic	I_{DD}	V_{DD} =2.5V,30MHz, load=15pF		3.9		mA
Supply Current, Dynamic	I_{DD}	V_{DD} =1.8V,30MHz, load=15pF		2.1		mA
PLL Off: Supply Current, Dynamic	I_{DD}	V_{DD} =3.3V,30MHz, load=15pF		2.0		mA
PLL Off: Supply Current, Dynamic	I_{DD}	V_{DD} =2.5V,30MHz, load=15pF		1.6		mA
PLL Off: Supply Current, Dynamic	I_{DD}	V_{DD} =1.8V,30MHz, load=5pF		0.8		mA
Supply Current, Dynamic	I_{DD}	When PDB=0			<10	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Power Supply Ramp	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.	.001		100	ms
Output Low Voltage	V_{OL}	I_{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Standard Drive	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Input Frequency (XIN)	Fundamental Crystal	10		50	MHz
Input (FIN) Frequency	@ V_{DD} =3.3V	1		200	MHz
	@ V_{DD} =2.5V			166	
	@ V_{DD} =1.8V			110	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz, 1.8V ≤15MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			200	MHz
	@ V_{DD} =2.5V			166	MHz
	@ V_{DD} =1.8V			110	MHz
Settling Time	At power-up (after V_{DD} increases over 1.62V)			2	ms
Output Enable Time	OE Function; Ta=25° C, 15pF Load. Add one clock period to this measurement for a usable clock output.			10	ns
	PDB Function; Ta=25° C, 15pF Load			2	ms
VDD Sensitivity	Frequency vs. V_{DD} +/-10%	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Duty Cycle (See MTC-1)	@2.5V and 3.3V over entire frequency range, $V_{DD}/2$	45	50	55	%
	@1.8V, ≤ 75MHz F_{OUT}, $V_{DD}/2$	45	50	55	
	@1.8V, 75MHz < F_{OUT} ≤110MHz	40		60	
Period Jitter, Pk-to-Pk* (10,000 samples measured)	With capacitive decoupling between V_{DD} and GND		70		ps

* Note: Jitter performance depends on the programming parameters.

CRYSTAL SPECIFICATIONS

PARAMETERS		SYMBOL	MIN	TYP	MAX	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		50	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range)		$C_{L\ (xtal)}$	8		12	pF
Maximum Sustainable Drive Level					100	µW
Operating Drive Level				30		µW
Metal Can Crystal	Shunt Capacitance	C0			5.5	pF
	ESR Max	ESR			50	Ω
Small SMD Crystal	Shunt Capacitance	C0			2.5	pF
	ESR Max	ESR			80	Ω

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (> 1 inch) as "striplines" or "microstrips" with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

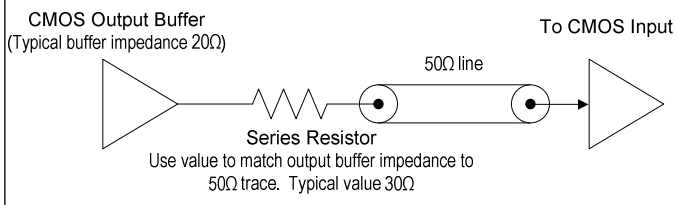
- Multiple VDD pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1µF for designs using frequencies < 50MHz and 0.01µF for designs using frequencies > 50MHz.

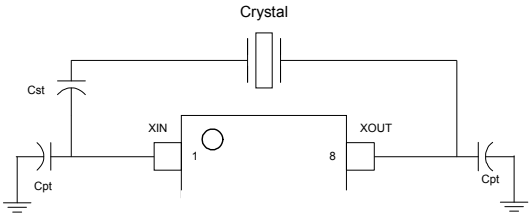
Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Crystal Tuning Circuit

Series and parallel capacitors used to fine tune the crystal load to the circuit load.

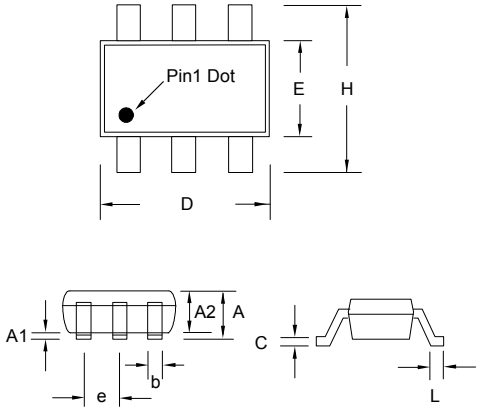


CST – Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator.
CPT – Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

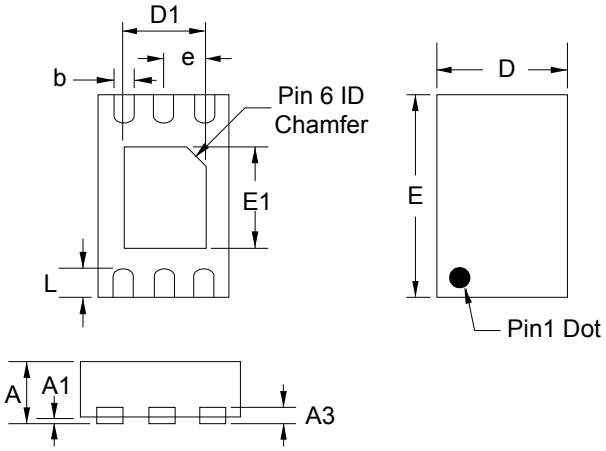
SOT23-6 L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	



DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL611s-02-XXX X X - X

- **Part Number**
- **3 DIGIT ID Code *** (will be assigned at programming time)
- **Package Type**
  - G=DFN-6L
  - T-SOT23-6L
- **Temperature**
  - C=Commercial (0°C to 70°C)
  - I=Industrial (-40°C to 85°C)
- **Shipping Option**
  - None=Tube
  - R=Tape & Reel

* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.

Part/Order Number	Marking†	Package Option
PL611s-02-XXXGC-R	XXX LLL	6-Pin DFN (Tape and Reel)
PL611s-02-XXXTC-R	02XXX LLL	6-Pin SOT23 (Tape and Reel)

* Note: LLL and LLLLL designates lot number

† Note: 'XXX' designates marking identifier that, at times, could be independent of the part number.
Please consult your PhaseLink sales representative for marking information.

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf