

1.8V to 3.3V, 1MHz to 130MHz XO IC

FEATURES

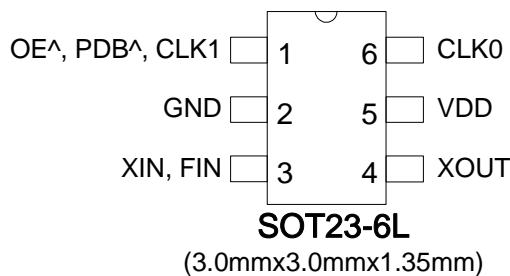
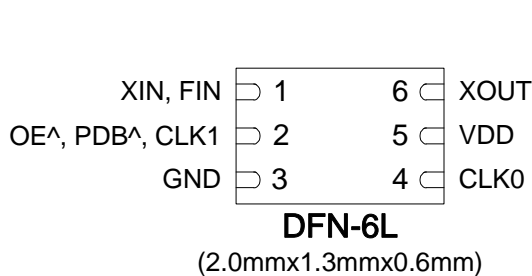
- Wide frequency coverage, programmable, advanced oscillator design
- Programmable “Odd/Even” Divider up to ÷63
- Direct oscillation operation with optional programmable features:
 - Output Drive Strength (4, 8, or 16mA)
 - 6-bit Odd/Even Output Divider
- Input Frequency:
 - Fundamental Crystal: 5MHz to 130MHz
 - Reference Clock: 1MHz to 130MHz
- Supports CMOS or Sine Wave input clock
- Output Frequency: 20kHz to 130MHz
- Very low Jitter and Phase Noise
- Low current consumption
- Single 1.8V ~ 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin DFN or SOT23 GREEN/RoHS compliant packaging

DESCRIPTION

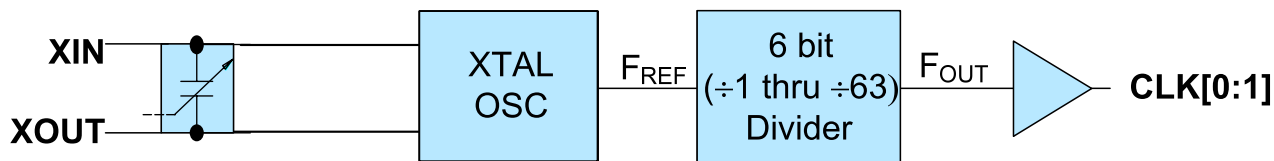
The PL610 is a high performance general purpose oscillator IC for outputs up to 130MHz. Designed to fit in a small 2 x 1.3mm DFN or 3 x 3mm SOT23 package, the PL610 offers the best phase noise and jitter performance and lowest power consumption of any comparable IC.

In addition, there is a ‘6’ bit optional programmable Odd/Even divider (default= 1), and ‘3’ programmable output drive strengths (4mA, 8mA (default), 16mA) to choose from. The full feature set of the PL610 makes it the most versatile XO for any application.

PACKAGE PIN CONFIGURATION



BLOCK DIAGRAM



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KEY PROGRAMMING PARAMETERS (Optional)

CLK[0:1] Output Frequency	Output Drive Strength	Programmable Input/Output
$F_{OUT} = F_{REF} / P^*$ (*: P is an Odd/Even Divider) Where P = 6 bit $CLK0 = F_{REF}, F_{REF}/2 \text{ or } F_{REF} / P$ $CLK1 = F_{REF}, F_{REF}/2 \text{ or } CLK0$	Three optional drive strengths to choose from: <ul style="list-style-type: none"> • Low: 4mA • Std: 8mA (default) • High: 16mA 	One output pin can be configured as: <ul style="list-style-type: none"> • OE - input • PDB - input • CLK1 – output

PACKAGE PIN AND DIE PAD ASSIGNMENT

Name	Pin Assignment		Type	Description									
	DFN-6L	SOT23-6L											
XIN, FIN	1	3	I	Crystal or Reference Clock input pin									
OE, PDB, CLK1	2	1	I/O	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB) input or CLK1 clock output. This pin has an internal 60KΩ pull up resistor for OE and 10MΩ pull up resistor for PDB. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>State</th> <th>OE</th> <th>PDB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Tri-state CLK</td> <td>Power Down Mode</td> </tr> <tr> <td>1 (default)</td> <td>Normal mode</td> <td>Normal mode</td> </tr> </tbody> </table>	State	OE	PDB	0	Tri-state CLK	Power Down Mode	1 (default)	Normal mode	Normal mode
State	OE	PDB											
0	Tri-state CLK	Power Down Mode											
1 (default)	Normal mode	Normal mode											
GND	3	2	P	GND connection									
CLK0	4	6	O	Programmable Clock Output									
VDD	5	5	P	VDD connection									
XOUT	6	4	O	Crystal Output pin									
				Do Not Connect (DNC) when FIN is present									

FUNCTIONAL DESCRIPTION

PL610-01 is a highly featured, very flexible, advanced XO design for high performance, low-power, small form-factor applications. The PL610-01 accepts a fundamental input crystal of 5MHz to 130MHz or a reference clock input of 1MHz to 130MHz and is capable of producing two outputs up to 130MHz. This flexible design allows the PL610-01 to deliver any frequency, FREF (Crystal or Ref Clk) frequency, FREF / 2 or FREF / P to CLK0 and/or CLK1. Some of the design features of the PL610-01 are mentioned below:

Clock Output (CLK0)

CLK0 is the main clock output. The output from CLK0 can be FREF (Crystal or Ref Clk), FREF/2 or FREF/P output. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA).

Programmable I/O (OE/PDB/CLK1)

The PL610-01 provides one programmable I/O pin which can be configured as one of the following functions:

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 60kΩ pull up resistor giving a default condition of logic "1".

Power-Down Control (PDB)

The Power Down (PDB) feature allows the user to put the PL610-01 into "Sleep Mode". When activated (logic '0'), PDB 'Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10μA of power. The PDB pin incorporates a 10MΩ pull up resistor giving a default condition of logic "1".

Clock Output (CLK1)

The CLK1 feature allows the PL610-01 to have an additional clock output programmed to one of the following:

FREF - Reference (Crystal or Ref Clk)
Frequency
FREF / 2
CLK0

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LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

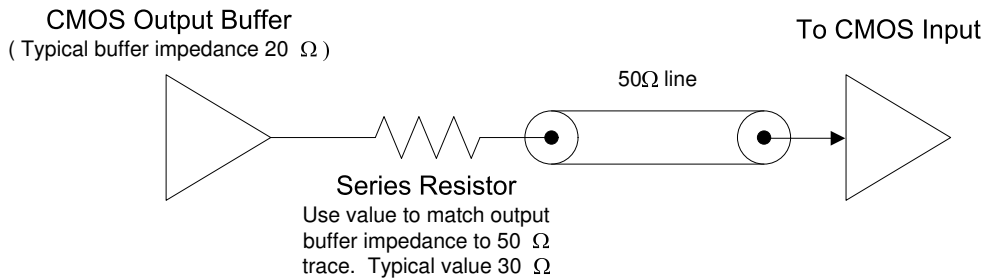
- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Multiple VDD pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1µF for designs using crystals < 50MHz and 0.01µF for designs using crystals > 50MHz.

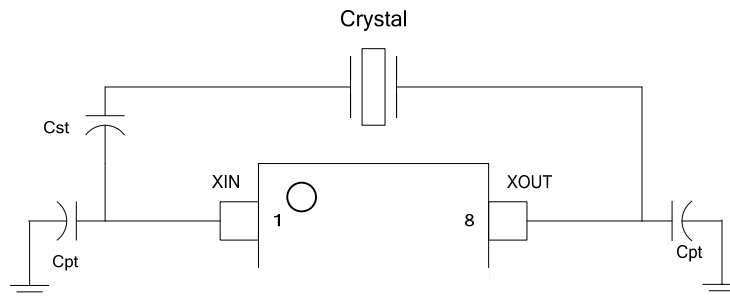
Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Crystal Tuning Circuit

Series and parallel capacitors used to fine tune the crystal load to the circuit load.



CST - Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator.

CPT - Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_i	-0.5	$V_{DD}+0.5$	V
Output Voltage Range	V_o	-0.5	$V_{DD}+0.5$	V
Storage Temperature	T_s	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency	Fundamental Crystal	5		130	MHz
Input (FIN) Frequency	@ $V_{DD} = 3.3V$	1		130	MHz
	@ $V_{DD} = 2.5V$				
	@ $V_{DD} = 1.8V$				
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V \leq 50MHz, 2.5V \leq 40MHz, 1.8V \leq 15MHz	0.1		V_{DD}	Vpp
Output Frequency	@ $V_{DD} = 1.8V-3.3V$	20kHz		130	MHz
VDD Sensitivity	Frequency vs. $V_{DD} \pm 10\%$	-2		2	ppm
Output Rise Time (See MTC-1)	15pF Load, 10/90% V_{DD} , High Drive, 3.3V		1	1.2	ns
Output Fall Time (See MTC-1)	15pF Load, 90/10% V_{DD} , High Drive, 3.3V		1	1.2	ns
Duty Cycle* (See MTC-1)		45	50	55	%

* For 1.8V operation, the 50% \pm 5% duty cycle is guaranteed for frequencies \leq 40MHz.

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DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic, with Loaded CMOS Output	I _{DD}	@V _{dd} =3.3V, 25MHz, load=15pF		3.4		mA
		@V _{dd} =2.5V, 25MHz, load=10pF		2.1		mA
		@V _{dd} =1.8V, 25MHz, load=5pF		0.9		mA
		@V _{dd} =1.8V, 2.0MHz, load=5pF		0.65		mA
Operating Voltage	V _{DD}		1.62		3.63	V
Output Low Voltage	V _{OL}	I _{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4mA Standard Drive	V _{DD} - 0.4			V
Output Current, Low Drive (See MCT-2)	I _{OLD}	V _{OL} = 0.4V, V _{OH} = 2.4V	4			mA
Output Current, Standard Drive (See MCT-2)	I _{OSD}	V _{OL} = 0.4V, V _{OH} = 2.4V	8			mA
Output Current, High Drive (See MCT-2)	I _{OHD}	V _{OL} = 0.4V, V _{OH} = 2.4V	16			mA

CRYSTAL SPECIFICATIONS (5MHz-60MHz)

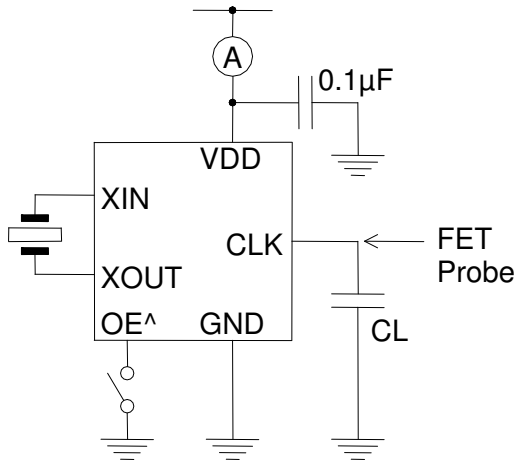
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	F _{XIN}	5		60	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	C _{L (xtal)}	8		12	pF
Maximum Sustainable Drive Level				100	μW
Operating Drive Level			25		μW
Crystal Shunt Capacitance	C ₀			3	pF
Effective Series Resistance, Fundamental, 5 - 60MHz (See MTC-1)	ESR			50	Ω

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CRYSTAL SPECIFICATIONS (60MHz-130MHz)

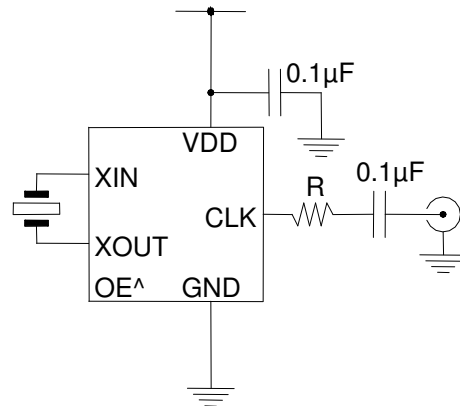
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	F_{XIN}	60		130	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L(xtal)}$	5		8	pF
Maximum Sustainable Drive Level				100	μW
Operating Drive Level			25		μW
Crystal Shunt Capacitance	C_0			2.5	pF
Effective Series Resistance, Fundamental, 60-130MHz (See MTC-1)	ESR			30	Ω

MEASUREMENT TEST CIRCUITS (MTC)

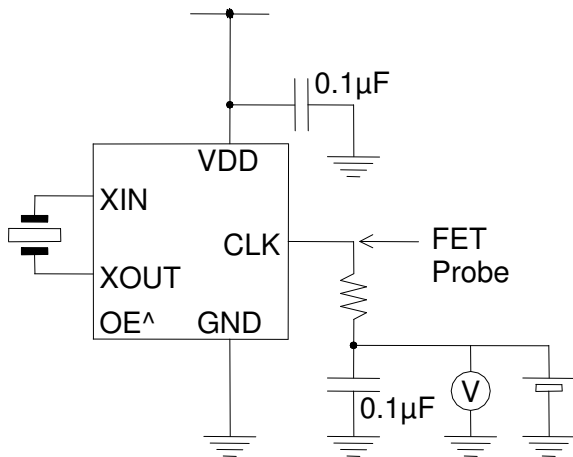
MTC-1: Rise Time, Fall Time, Duty Cycle, VOL, VOH, I_{dd}, Power Down Current, Output Enable/Disable



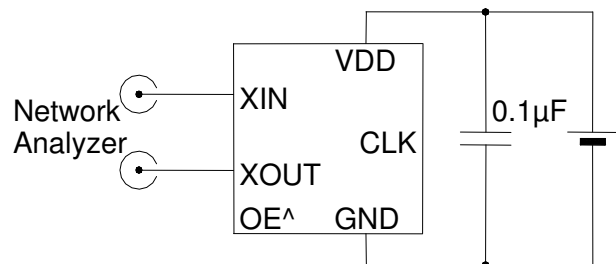
MTC-3: Jitter and Phase Noise



MTC-2: Output Drive Current and Output Impedance

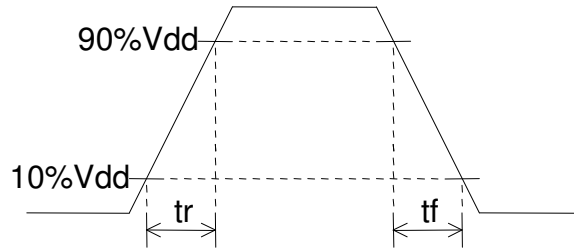


MTC-4: Negative Resistance

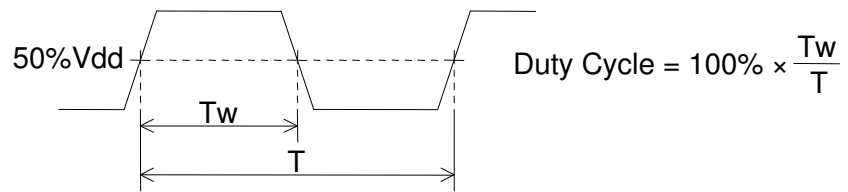


WAVEFORM SWITCHING CHARACTERISTICS

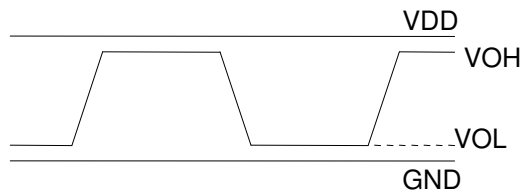
Rise and Fall times:



Duty Cycle:



VOH, VOL:

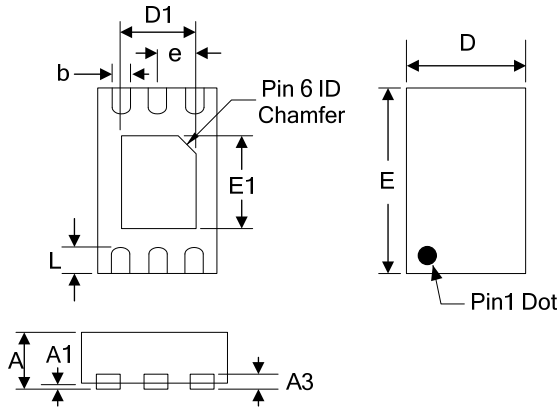


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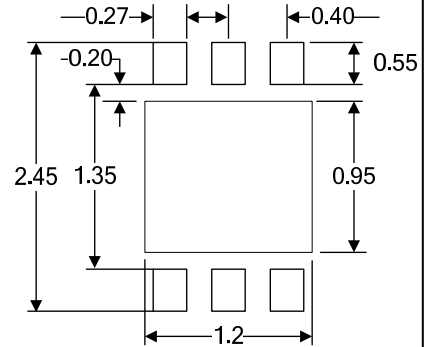
PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

DFN-6L

Symbol	Dimension (MM)	
	Min.	Max.
A	0.5	0.6
A1	0	0.05
A3	0.152 REF	
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.2	0.3

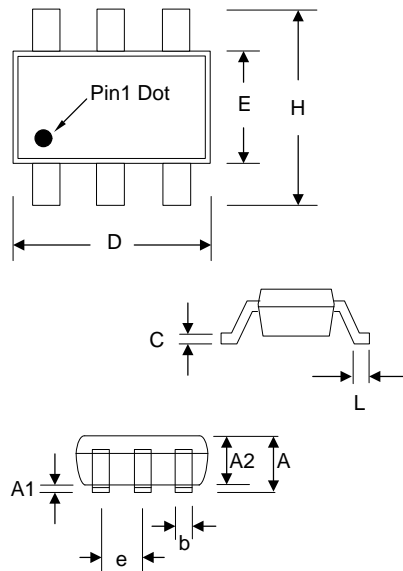


Recommended Land Pattern (MM)

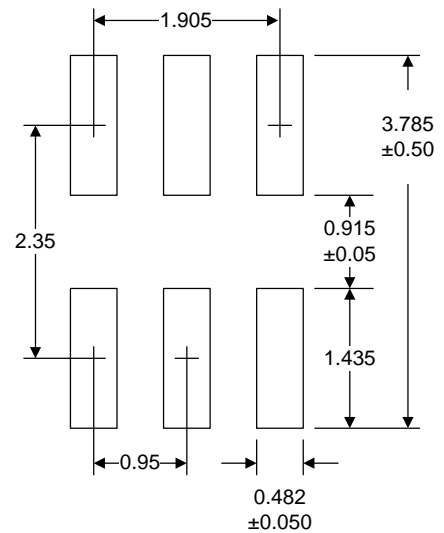


SOT23-6L

Symbol	Dimension (MM)	
	Min	Max
A	1.05	1.45
A1	0.05	0.15
A2	1.00	1.30
b	0.35	0.50
c	0.127 Typical	
D	2.80	3.00
E	1.50	1.70
H	2.60	3.00
L	0.35	0.55
e	0.95 Typical	



Recommended Land Pattern (MM)



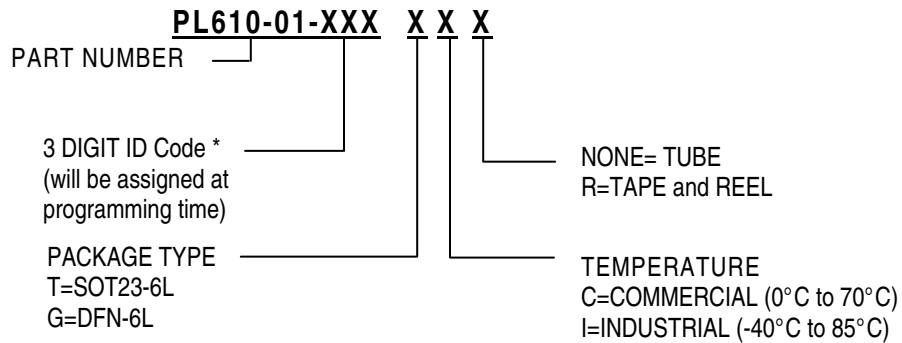
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ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



Part/Order Number	Marking†	Package Option
PL610-01-XXXGC-R	XXX LLL	6-Pin DFN (Tape and Reel)
PL610-01-XXXTC-R	E1XXX LLL	6-Pin SOT-23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that could be independent of the part number.

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