1.8V-3.3V Single IC XO with Frequency Tuning (5MHz to 130MHz)

FEATURES

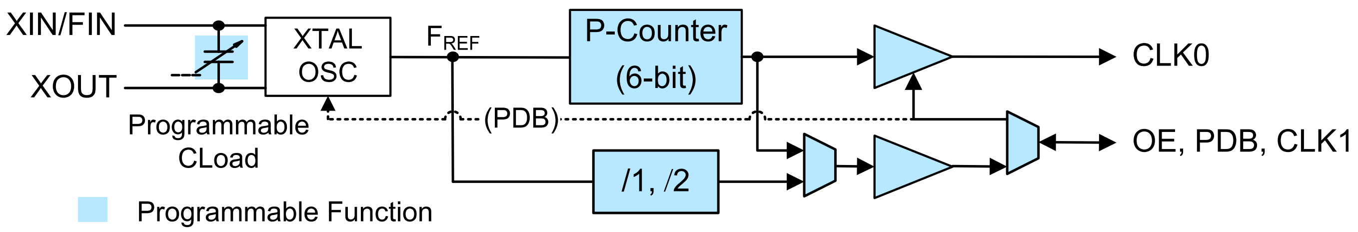
- Single die, wide frequency coverage, programmable advanced oscillator design.
- Single IC to cover up to 130MHz output frequency.
- Direct oscillation operation with optional programmable features:
    - ±50ppm Frequency Tuning
    - Output Drive Setting (4, 8, or 16mA)
    - 6-bit Odd/Even Output Divider (≤ ÷63)
- Input Frequency: Fundamental crystal:
    - 5MHz to 60MHz (Default)
    - 60MHz to 130MHz (programming option)
- Output Frequency: LVCMOS
    - 80kHz to 130MHz
- Wire Bond and Flip Chip options to choose from.
- Very low Jitter and Phase Noise
- Low current consumption
- Single 1.8V, 2.5V, or 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C

DESCRIPTION

The PL610 is a high performance general purpose clock that uses a single die to cover outputs up to 130MHz, eliminating the need for multiple ICs to cover a wide frequency range. Designed to fit in a small 2.0 x 1.6mm, or larger substrates, the PL610 offers the best phase noise and jitter performance, smallest die size, and lowest power consumption of any comparable IC.

The optional 'frequency fine tuning' feature of PL610 allows for frequency adjustment after encapsulation of the module, up to ±50ppm. In addition, there is a '6' bit optional programmable Odd/Even divider (default= ⁒1), and '3' programmable output drive strengths (4mA, 8mA (default), 16mA) to choose from. The full feature set of PL610 makes it the most versatile XO for any application.

BLOCK DIAGRAM



KEY PROGRAMMING PARAMETERS

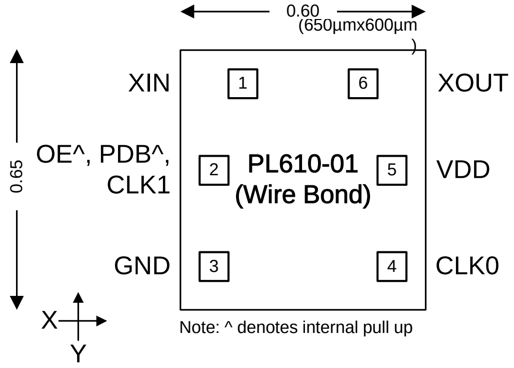
CLK[0:1] Output Frequency	Crystal Load	Output Drive Strength	Output Dividers
CLK0 = F_{REF}, $F_{REF}/2$ or F_{REF} / P Where P = 6-bit Optional CLK1 = F_{REF}, $F_{REF}/2$ or CLK0	Optional 'Frequency Tuning' after encapsulation, up to: ±50ppm Tuning Range Single bit CL adjustment for Hi/Low frequency input	Three optional drive strengths to choose from: • Low: 4mA • Std: 8mA (default) • High: 16mA	Optional 6-bit Odd/Even output divider: • ⁒1 (default) to ⁒63

DIE SPECIFICATION

Chip Size	Chip Thickness	Pad Size	Chip Base
0.65x 0.60mm	Optional	90µm	GND level

PAD ASSIGNMENT AND SPECIFICATION

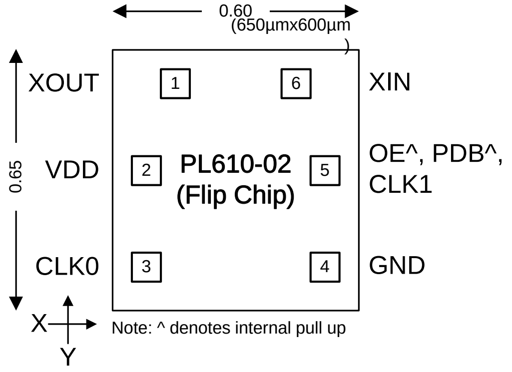
PL610-01



Note: ^ denotes internal pull up

Pad #	Pad Name	Pad Center	
		X	Y
1	XIN	-177	231
2	OE, PDB, CLK1	-215	41
3	GND	-215	-186
4	CLK0	215	-186
5	VDD	215	41
6	XOUT	177	231

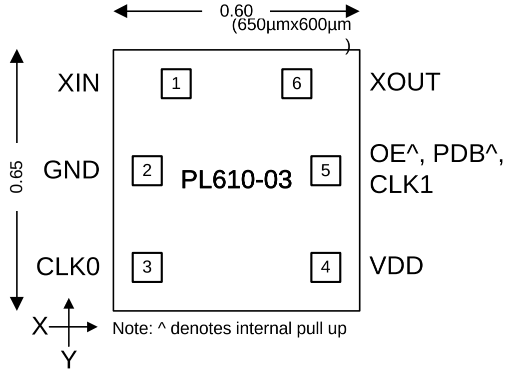
PL610-02



Note: ^ denotes internal pull up

Pad #	Pad Name	Pad Center	
		X	Y
1	XOUT	-177	231
2	VDD	-215	41
3	CLK0	-215	-186
4	GND	215	-186
5	OE, PDB, CLK1	215	41
6	XIN	177	231

PL610-03



Note: ^ denotes internal pull up

Pad #	Pad Name	Pad Center	
		X	Y
1	XIN	-177	231
2	GND	-215	41
3	CLK0	-215	-186
4	VDD	215	-186
5	OE, PDB, CLK1	215	41
6	XOUT	177	231

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PAD FUNCTION DESCRIPTION

Pad Name	Description
CLK0	Programmable Clock Output.
GND	GND connection
OE^, PDB^, CLK1	Programmable as: Output Enable (OE) – Enables/Disables CLK0 output buffer Power Down (PDB) – Enables/Disables CLK0 output buffer and crystal oscillator circuitry CLK1 – Second Clock Output
VDD	VDD connection
XIN	Crystal input pad
XOUT	Crystal Output pad

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. * Operating Temperature is guaranteed by design for all parts but tested for COMMERCIAL grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency (XIN)	Fundamental Crystal, Low Frequency	5		60	MHz
	Fundamental Crystal, High Frequency	60		130	
Output Frequency	@ V_{DD} = 1.8V to 3.3V, ±10%	.080		130	MHz
VDD Sensitivity	Frequency vs. V_{DD}+/-10%	-2		2	ppm
Output Rise Time (See MTC-1)	15pF Load, 10/90%V_{DD}, High Drive, 3.3V		1	1.2	ns
Output Fall Time (See MTC-1)	15pF Load, 90/10%V_{DD}, High Drive, 3.3V		1	1.2	ns
Duty Cycle* (See MTC-1)		45	50	55	%

* For 1.8V operation, the 50% ±5% duty cycle is guaranteed for frequencies ≤40MHz.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, Loaded LVCMOS Output	I_{DD}	@ V_{DD}=3.3V, 40MHz, load=15pF		3.7		mA
		@ V_{DD}=2.5V, 40MHz, load=15pF		2.75		
		@ V_{DD}=1.8V, 40MHz, load=15pF		2.0		
		@ V_{DD}=3.3V, 26MHz, load=15pF		2.5		
		@ V_{DD}=2.5V, 26MHz, load=15pF		1.8		
		@ V_{DD}=1.8V, 26MHz, load=15pF		1.3		
Supply Current, Dynamic, Unloaded LVCMOS Output		@ V_{DD}=3.3V, 40MHz, no load		1.65		mA
		@ V_{DD}=2.5V, 40MHz, no load		1.2		
		@ V_{DD}=1.8V, 40MHz, no load		0.9		
		@ V_{DD}=3.3V, 26MHz, no load		1.2		
		@ V_{DD}=2.5V, 26MHz, no load		0.8		
		@ V_{DD}=1.8V, 26MHz, no load		0.58		
Operating Voltage	V_{DD}		1.62		3.63	V
Power Supply Ramp	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.	.001		100	ms
Output Low Voltage	V_{OL}	I_{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Standard Drive	V_{DD} – 0.4			V
Output Current, Low Drive *	I_{OLD}	V_{OL} = 0.4V, V_{OH} = 2.4V	±4			mA
Output Current, Std Drive*	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	±8			
Output Current, High Drive*	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	±16			

***Note: See MCT-2 below**

CRYSTAL SPECIFICATIONS (5MHz to 60MHz)

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	F_{XIN}	5		60	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L\ (xtal)}$	8		12	pF
Maximum Sustainable Drive Level				100	µW
Operating Drive Level			25		µW
Crystal Shunt Capacitance	C0			3	pF
Effective Series Resistance, 5MHz to 60MHz, (See MTC-1)	ESR			50	Ω

CRYSTAL SPECIFICATIONS (60MHz to 130MHz)

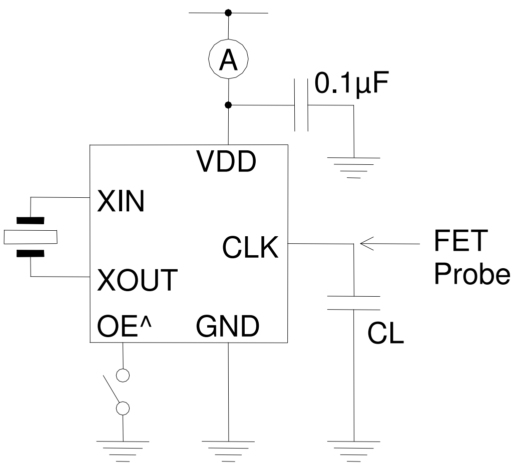
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	F_{XIN}	60		130	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L\ (xtal)}$	5		8	pF
Maximum Sustainable Drive Level				100	µW
Operating Drive Level			25		µW
Crystal Shunt Capacitance	C0			2.5	pF
Effective Series Resistance, 60MHz to 130MHz, (See MTC-1)	ESR			30	Ω

PHASE NOISE SPECIFICATIONS (See MCT-3)

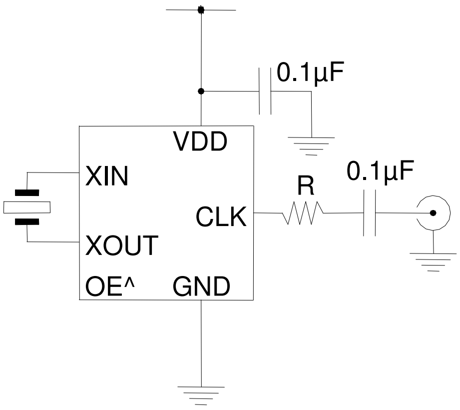
PARAMETERS	FREQ.	@1Hz	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	@1M	UNITS
Phase Noise relative to carrier (typical)	40.0MHz	-67	-98	-127	-142	-151	-155	-155	dBc/Hz
	26.0MHz	-65	-96	-124	-145	-150	-155	-155	

MEASUREMENT TEST CIRCUITS (MTC)

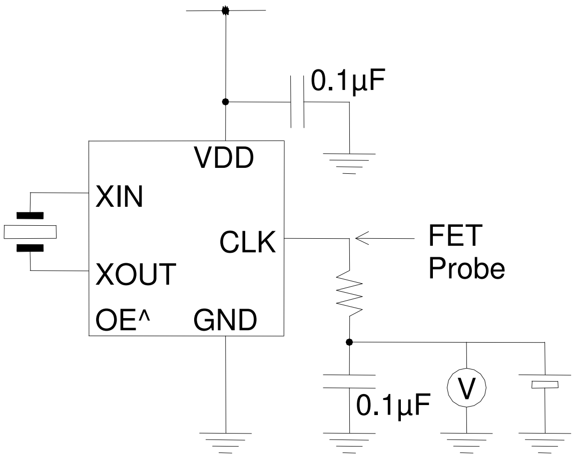
MTC-1: Rise Time, Fall Time, Duty Cycle, VOL, VOH, I_{dd}, Power Down Current, Output Enable/Disable



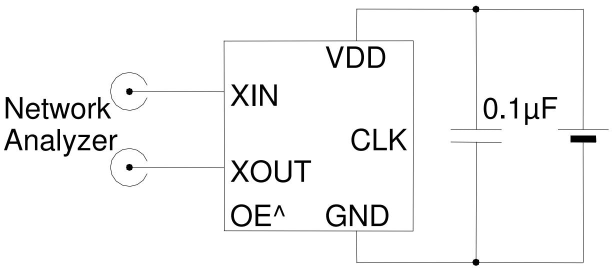
MTC-3: Jitter and Phase Noise



MTC-2: Output Drive Current and Output Impedance

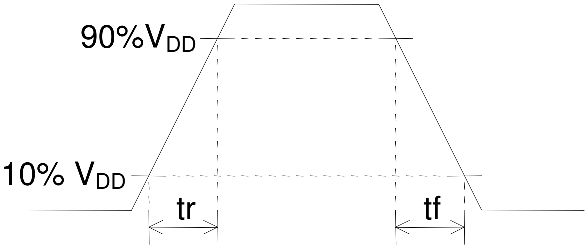


MTC-4: Negative Resistance

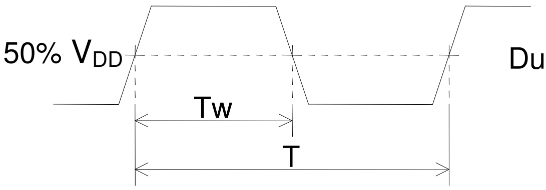


WAVEFORM SWITCHING CHARACTERISTICS

Rise and Fall times:

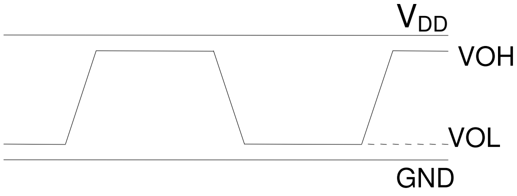


Duty Cycle:



$$\text{Duty Cycle} = 100\% \times \frac{Tw}{T}$$

VOH, VOL:



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL610-0x X X X

Part Number — PL610-0x

Temperature Range
C=Commercial (0°C to 70°C)

Package Type
D = Die
E = Die (with Non-Conductive Backcoating)
V = Wafer (with Non-Conductive Backcoating)
W = Wafer

Thickness
6 = 6 Mil (Available in Die only)
8 = 8 Mil
A = 10 Mil
Blank = 12 Mil

Part / Order Number	Marking	Package Option	Temperature
PL610-01DxC		Die (Waffle Pack)	0°C to +70°C
PL610-01ExC		Die (Waffle Pack)	0°C to +70°C
PL610-01VxC		Wafer	0°C to +70°C
PL610-01WxC		Wafer	0°C to +70°C
PL610-02DxC		Die (Waffle Pack)	0°C to +70°C
PL610-02ExC		Die (Waffle Pack)	0°C to +70°C
PL610-02VxC		Wafer	0°C to +70°C
PL610-02WxC		Wafer	0°C to +70°C
PL610-03DxC		Die (Waffle Pack)	0°C to +70°C
PL610-03ExC		Die (Waffle Pack)	0°C to +70°C
PL610-03VxC		Wafer	0°C to +70°C
PL610-03WxC		Wafer	0°C to +70°C