

### DESCRIPTION

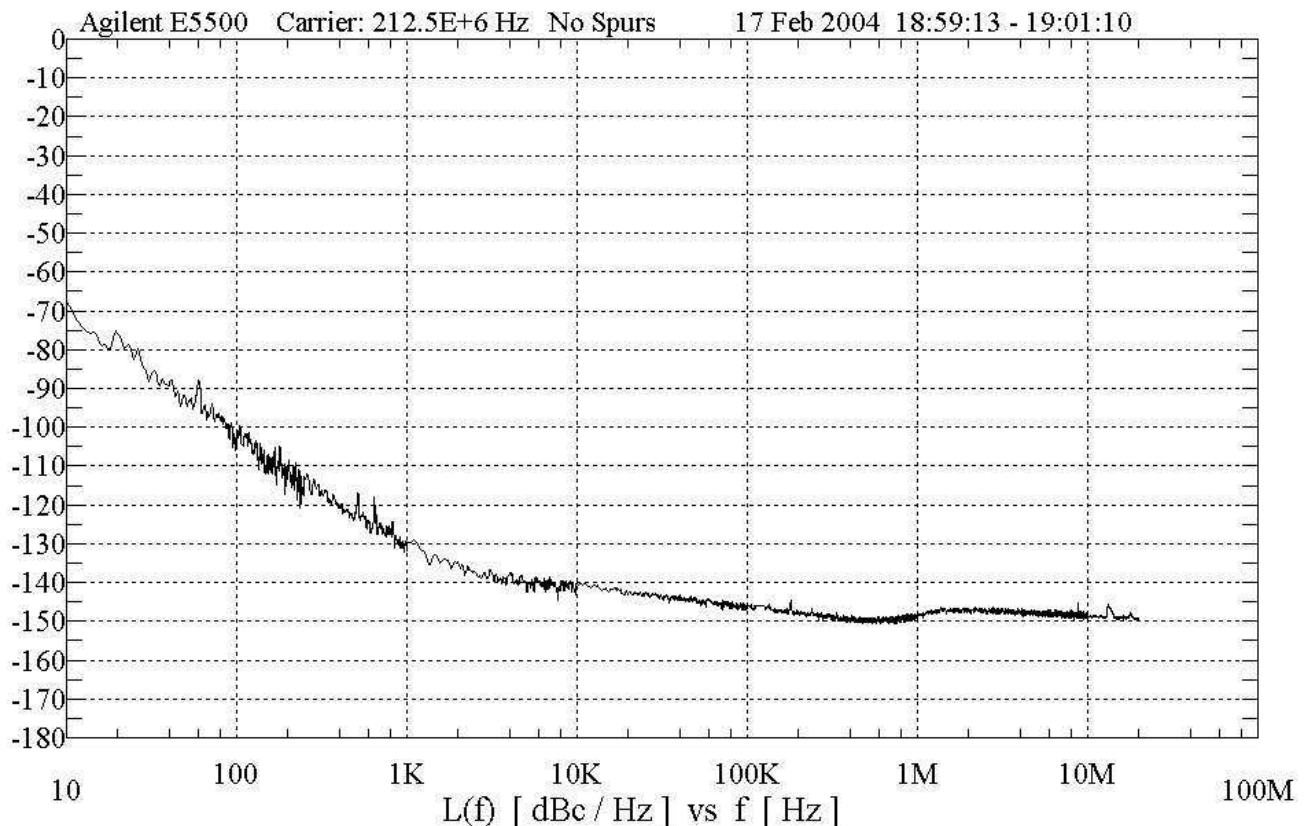
PhaseLink's Analog Frequency Multipliers™ (AFMs) are the industry's first "Balanced Oscillator" utilizing analog multiplication of the fundamental frequency (at double or quadruple frequency), combined with an attenuation of the fundamental of the reference crystal, without using a phase-locked loop (PLL), in CMOS technology.

PhaseLink's patent pending PL663-xx family of AFM products can achieve up to 800 MHz differential LVPECL, LVDS, or single-ended LVCMOS output with little jitter or phase noise deterioration.

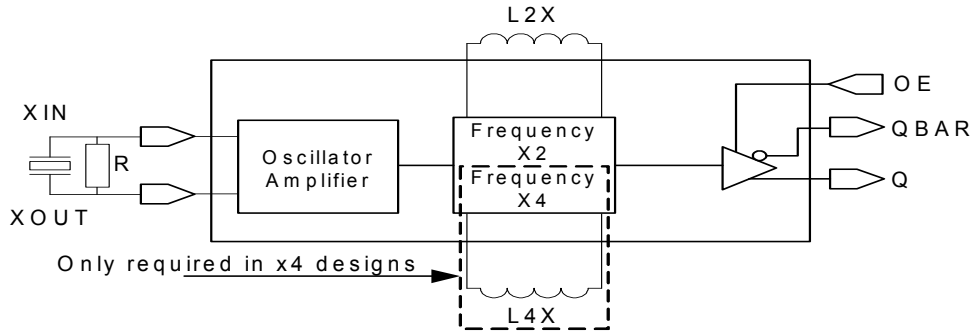
PL663-xx family of products utilizes a low-power CMOS technology and is housed in GREEN/ RoHS compliant 16-pin TSSOP and 3x3 QFN packages.

### FEATURES

- Non-PLL frequency multiplication
- Input frequency from 30-200 MHz
- Output frequency from 60-800 MHz
- Low phase noise and jitter (equivalent to fundamental at the output frequency)
- Ultra-low jitter
  - RMS phase jitter < 0.25 ps (12 kHz to 20 MHz)
  - RMS period jitter < 2.5 ps typ.
- Low phase noise
  - -145 dBc/Hz @ 100 kHz offset from 155.52 MHz
  - -150 dBc/Hz @ 10 MHz offset from 155.52 MHz
- Low input frequency eliminates the need for expensive crystals
- Differential LVPECL/LVDS, or single-ended LVCMOS output
- Single 2.5V or 3.3V +/- 10% power supply
- Optional industrial temperature range (-40°C to +85°C)
- Available in 16-pin GREEN/RoHS compliant TSSOP, and 16-pin 3x3 QFN packages.

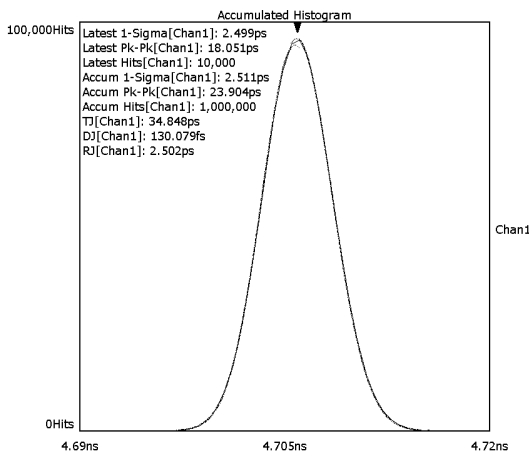


**Figure 1: 2X AFM Phase Noise at 212.5 MHz (106.25 MHz 3<sup>rd</sup> overtone crystal)**

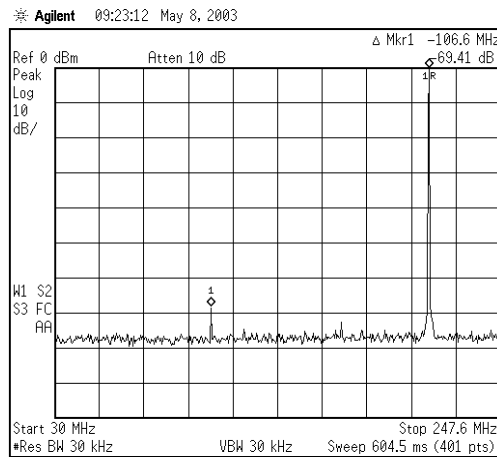


**Figure 2: Block Diagram of AFM XO**

Figure 3 shows the period jitter histogram of the 2x Analog Frequency Multiplier at 212.5 MHz, while Figure 4 shows the very low levels of sub-harmonics that correspond to the exceptional performance (i.e. low jitter).



**Figure 3: Period Jitter Histogram at 212.5MHz Analog Frequency Multiplier (2x), with 106.25 MHz crystal**



**Figure 4: Spectrum Analysis at 212.5MHz Analog Frequency Multiplier (2x), with sub-harmonics below -69dBc**

### OE LOGIC SELECTION

OUTPUT	OESEL	OE	Output State
LVPECL	0 (Default)	0 (Default)	Enabled
		1	Tri-state
	1	0	Tri-state
		1 (Default)	Enabled
LVDS or LVCMOS	0 (Default)	0	Tri-state
		1 (Default)	Enabled
	1	0 (Default)	Enabled
		1	Tri-state

OESEL and OE: Connect to V<sub>DD</sub> to set to "1", connect to GND to set to "0". [The 'Default' state is set by internal pull up/down resistor.]

### PRODUCT SELECTOR GUIDE

### FREQUENCY VERSUS PHASE NOISE PERFORMANCE

Part Number	Input Frequency Range (MHz)	Analog Multiplication Factor	Output Frequency Range (MHz)	Output Type	Phase Noise at Frequency Offset From Carrier (dBc/Hz)							
					Carrier Freq. (MHz)	10Hz	100Hz	1KHz	10KHz	100KHz	1MHz	10MHz
PL663-07	30 - 80	2	60 to 160	LVC MOS	156.25	-75	-105	-130	-140	-145	-150	-150
PL663-08	30 - 80	2	60 to 160	LVPECL	156.25	-75	-105	-130	-140	-145	-150	-150
PL663-17	75 - 140	2	150 to 280	LVC MOS	212.5	-70	-100	-130	-140	-145	-148	-148
PL663-18	75 - 140	2	150 to 280	LVPECL	212.5	-70	-100	-130	-140	-145	-148	-148
PL663-19	75 - 140	2	150 to 280	LVDS	212.5	-70	-100	-130	-140	-145	-148	-148
PL663-28	140 - 160	2	280 to 320	LVPECL	311.04	-60	-92	-122	-140	-142	-146	-146
PL663-29	100 - 160	2	200 to 320	LVDS	311.04	-60	-92	-122	-140	-142	-146	-148

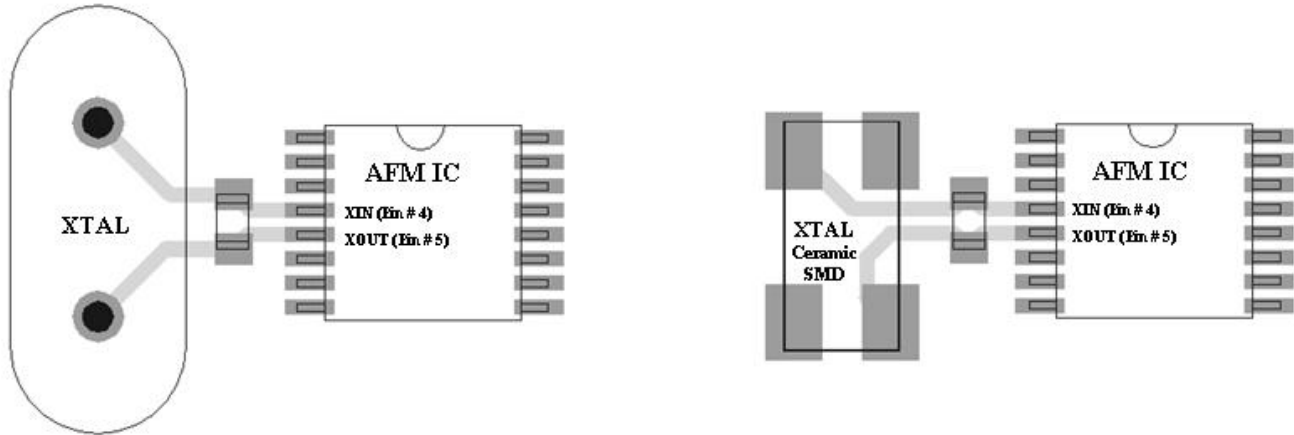
### FREQUENCY VERSUS JITTER, AND SUB-HARMONIC PERFORMANCE

Part Number	Output Freq. (MHz)	RMS Period Jitter (ps)			Peak to Peak Period Jitter (ps)			RMS Accumulated (L.T.) Jitter (ps)			Phase Jitter (12 KHz-20MHz) (ps)			Spectral Specifications / Sub-harmonic Content (dBc) Frequency (MHz)						
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Carrier Freq. MHz (Fc)	@ -75% (Fc)	@ -50% (Fc)	@ -25% (Fc)	@ +25% (Fc)	@ +50% (Fc)	@ +75% (Fc)
		PL663-07	156.25		2	3		18	20			3		0.24		156.25		-70		
PL663-08	156.25		2	3		18	20			3		0.24		156.25		-70			-75	
PL663-17	212.50		2.5	4		18	20			4		0.19		212.50		-70			-75	
PL663-18	212.50		2.5	4		18	20			4		0.19		212.50		-70			-75	
PL663-19	212.50		2.5	4		18	20			4		0.19		212.50		-70			-75	
PL663-28	311.04		2.5	4		18	20			4		0.16		311.04		-65			-70	
PL663-29	311.04		2.5	4		18	20			4		0.16		311.04		-65			-70	

**Note:** Wavecrest data 10,000 hits. No Filtering was used in Jitter Calculations.  
 Agilent E5500 was used for phase jitter measurements.  
 Spectral specifications were obtained using Agilent E7401A.

### BOARD LAYOUT CONSIDERATIONS AND CRYSTAL SPECIFICATIONS

#### BOARD LAYOUT CONSIDERATIONS



To minimize parasitic effects and improve performance, do the following:

- Place the crystal as close as possible to the IC.
- Make the board traces that are connected to the crystal pins symmetrical. The board trace symmetry is very important, as it reduces the negative parasitic effects to produce clean frequency multiplication with low jitter.

#### CRYSTAL SPECIFICATIONS

Part Number	Crystal Resonator Frequency ( $F_{XIN}$ )	Mode	CL (xtal)	ESR( $R_E$ )	$C_0$
			Typical	Max.	Max.
PL663-07 PL663-08	30 to 80MHz	Fundamental or 3rd overtone	5 pF	30 $\Omega$	4.5 pF
PL663-17 PL663-18 PL663-19	75 to 140MHz	Fundamental or 3rd overtone	5 pF	60 $\Omega$	4.0 pF
PL663-28 PL663-29	140 to 200MHz	Fundamental or 3rd overtone	5 pF	60 $\Omega$	4.0 pF

**Note:** Non-specified parameters can be chosen as standard values from crystal suppliers.  
CL ratings larger than 5pF require a crystal frequency adjustment.  
Request detailed crystal specifications from PhaseLink.

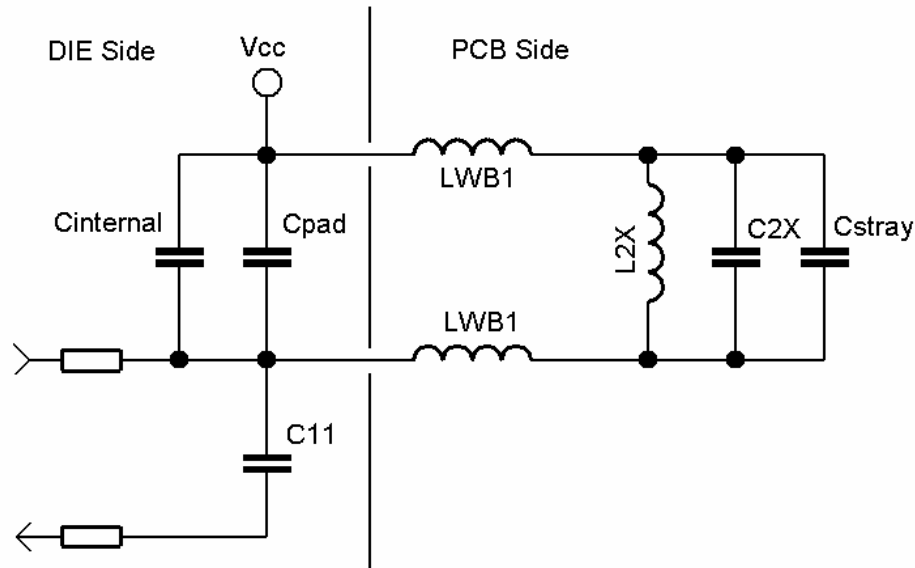
### EXTERNAL COMPONENT VALUES

#### INDUCTOR VALUE OPTIMIZATION

The required inductor value(s) for the best performance depends on the operating frequency, and the board layout specifications. The listed values in this datasheet are based on the calculated parasitic values from PhaseLink's evaluation board design. These inductor values provide the user with a starting point to determine the optimum inductor values. Additional fine-tuning may be required to determine the optimal solution.

To assist with the inductor value optimization, PhaseLink has developed the "AFM Tuning Assistant" software. You can download this software from PhaseLink's web site ([www.phaselink.com](http://www.phaselink.com)). The software consists of two worksheets. The first worksheet (named L2) is used to fine-tune the 'L2' inductor value, and the second worksheet (named L4) is used for fine tuning of the 'L4' (used in 4x AFMs only) inductor value.

For those designs using PhaseLink's recommended board layout, you can use the "AFM Tuning Assistant" to determine the optimum values for the required inductors. This software is developed based on the parasitic information from PhaseLink's board layout and can be used to determine the required inductor and parallel capacitor (see LWB1 and Cstray parameters) values. For those employing a different board layout in their design, we recommend to use the parasitic information of their board layout to calculate the optimized inductor values. Please use the following fine tuning procedure:



**Figure 5: Diagram Representation of the Related System Inductance and Capacitance**

#### DIE SIDE

- Cinternal = Based on AFM Device
- Cpad = 2.0 pF, Bond pad and its ESD circuitry
- C11 = 0.4 pF, The following amplifier stage

#### PCB side

- LWB1 = 2 nH, (2 places), Stray inductance
- Cstray = 1.0 pF, Stray capacitance
- L2X = 2x inductor
- C2X = range (0.1 to 2.7), Fine tune inductor if used

- There are two default variables that normally will not need to be modified. These are Cpad, and C11 and are found in cells B22 and B27 of 'AFM Tuning Assistant', respectively.
- LWB1 is the combined stray inductance in the layout. The DIE wire bond is ~ 0.6 nH and in the case of a leaded part an additional 1.0 nH is added. Your layout inductance must be added to these. There are 2 of these and they are assumed to be approximately symmetrical so you only need to enter this inductance once in cell B23.
- Enter the stray parasitic capacitance into cell B26. An additional 0.5 pF must be added to this value if a leaded part is used.
- Enter the appropriate value for Cinternal into B21 based on the device used (see column D). Use the 'AFM Tuning Assistant' software to calculate L2X (and C2X if used) for your resonance frequency.

Internal Capacitor Selection by Device	
Device Number	Cinternal (pF)
	<b>2X</b>
PL663-0X	46.500
PL663-1X	14.625
PL663-2X	14.625

### EXTERNAL COMPONENT VALUES – 3<sup>RD</sup> OVERTONE RESISTOR SELECTIONS (R3rd)

This resistor is only required when a third overtone crystal is used. The chart below indicates the calculated and the nearest “E12” resistor values versus frequency.

PL663-07/08			PL663-17/18/19			PL663-28/29		
Freq. (MHz)	R3rd (Ω)	E12 Pick KΩ	Freq. (MHz)	R3rd (Ω)	E12 Pick KΩ	Freq. (MHz)	R3rd (Ω)	E24 Pick KΩ
30	9,917	10	75	2,125	2.2	140.0	915	0.91
32	9,297	10	77.5	2,056	2.2	142.0	902	0.91
34	8,750	8.2	80	1,992	2.2	144.0	890	0.91
36	8,264	8.2	82.5	1,932	1.8	146.0	878	0.91
38	7,829	8.2	85	1,875	1.8	148.0	866	0.91
40	7,438	6.8	87.5	1,821	1.8	150.0	854	0.82
42	7,083	6.8	90	1,771	1.8	152.0	843	0.82
44	6,761	6.8	92.5	1,723	1.8	154.0	832	0.82
46	6,467	6.8	95	1,678	1.8	156.0	821	0.82
48	6,198	6.8	97.5	1,635	1.5	158.0	811	0.82
50	5,950	5.6	100	1,594	1.5	160.0	801	0.82
52	5,721	5.6	102.5	1,555	1.5	162.0	790	0.82
54	5,509	5.6	105	1,518	1.5	164.0	780	0.75
56	5,313	5.6	107.5	1,483	1.5	166.0	770	0.75
58	5,129	4.7	110	1,449	1.5	168.0	759	0.75
60	4,958	4.7	112.5	1,417	1.5	170.0	749	0.75
62	4,798	4.7	115	1,386	1.5	172.0	740	0.75
64	4,648	4.7	117.5	1,356	1.5	174.0	730	0.75
66	4,508	4.7	120	1,328	1.2	176.0	720	0.75
68	4,375	4.7	122.5	1,301	1.2	178.0	711	0.68
70	4,250	3.9	125	1,275	1.2	180.0	701	0.68
72	4,132	3.9	127.5	1,250	1.2	182.0	692	0.68
74	4,020	3.9	130	1,226	1.2	184.0	683	0.68
76	3,914	3.9	132.5	1,203	1.2	186.0	674	0.68
78	3,814	3.9	135	1,181	1.2	188.0	665	0.68
80	3,719	3.9	137.5	1,159	1.2	190.0	656	0.68
			140	1,138	1.2	192.0	647	0.62
						194.0	639	0.62
						196.0	630	0.62
						198.0	622	0.62
						200.0	614	0.62

### ELECTRICAL SPECIFICATIONS

#### ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, DC	$V_I$	GND-0.5	$V_{DD}+0.5$	V
Output Voltage, DC	$V_O$	GND-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-55	+150	°C
Industrial Ambient Operating Temperature	$T_{A\_I}$	-40	+85	°C
Commercial Ambient Operating Temperature	$T_{A\_C}$	0	+70	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C

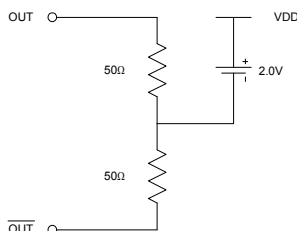
Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

**\*Note:** For performance reasons, some pins on this device do not meet PhaseLink's standard ESD protection. Therefore, the ESD protection on this device is classified as Class I HBM and Class A MM. Handling precaution is recommended.

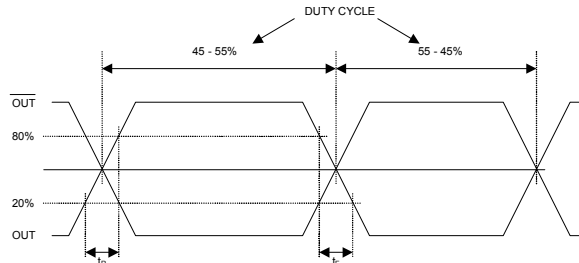
#### LVPECL ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (loaded outputs)	$I_{DD}$	$F_{out} = 212.5 \text{ MHz}$ , 15pF Load	58	65	75	mA
Operating Supply Voltage	$V_{DD}$		2.25		3.63	V
Output Clock Duty Cycle		@ $V_{DD} - 1.3V$	45	50	55	%
Short Circuit Current				$\pm 50$		mA
Output High Voltage	$V_{OH}$	$R_L = 50 \Omega$ to $V_{DD} - 2V$	$V_{DD} - 1.025$			V
Output Low Voltage	$V_{OL}$	$R_L = 50 \Omega$ to $V_{DD} - 2V$			$V_{DD} - 1.620$	V
Clock Rise Time	$t_r$	@20/80%		0.25	0.45	ns
Clock Fall Time	$t_f$	@80/20%		0.25	0.45	ns

PECL Levels Test Circuit



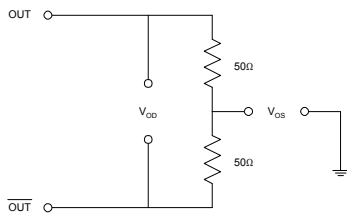
PECL Transition Time Waveform



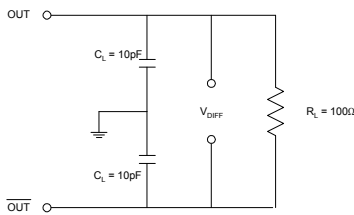
### LVDS ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (with loaded outputs)	$I_{DD}$	$F_{out} = 212.5\text{MHz}$ , 15pF Load		55	60	mA
Operating Supply Voltage	$V_{DD}$		2.25		3.63	V
Output Clock Duty Cycle		@ 1.25V	45	50	55	%
Output Differential Voltage	$V_{OD}$	$R_L = 100\ \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$		$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA
Differential Clock Rise Time	$t_r$	$R_L = 100\ \Omega$ $C_L = 10\ \text{pF}$ (see figure)	0.2	0.5	0.7	ns
Differential Clock Fall Time	$t_f$		0.2	0.5	0.7	ns

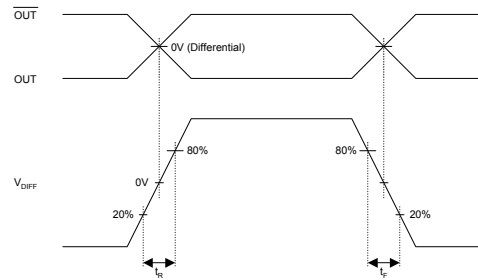
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



### LVC MOS ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, Loaded Outputs	$I_{DD}$	At 100MHz, load=10pF		32	40	mA
Operating Supply Voltage	$V_{DD}$		2.25		3.63	V
Output High Voltage (LVTTTL)	$V_{OH3.3}$	$I_{OH} = -8.5mA$ , 3.3V Supplies	2.4			V
Output Low Voltage (LVTTTL)	$V_{OL3.3}$	$I_{OL} = 8.5mA$ , 3.3V Supplies			0.4	V
Output High Voltage (LVC MOS)	$V_{OHC3.3}$	$I_{OH} = -4mA$ , 3.3V Supplies	$V_{DD} - 0.4$			V
Output High Voltage	$V_{OH2.5}$	$I_{OH} = 1mA$ , 2.5V Supplies	$V_{DD} - 0.2$			V
Output Low Voltage	$V_{OL2.5}$	$I_{OL} = 1mA$ , 2.5V Supplies			0.2	V
Output Drive Current	$I_{OSD}$	$V_{OL} = 0.4V$ , $V_{OH} = 2.4V$ (per output)		8.5		mA
Output Clock Rise/Fall Time	$T_r/T_f$	10% / 90% $V_{DD}$ with 10 pF load		1.2	1.6	ns
Output Clock Duty Cycle		Measured @ 50% $V_{DD}$	45	50	55	%

### BOARD DESIGN AND LAYOUT CONSIDERATIONS

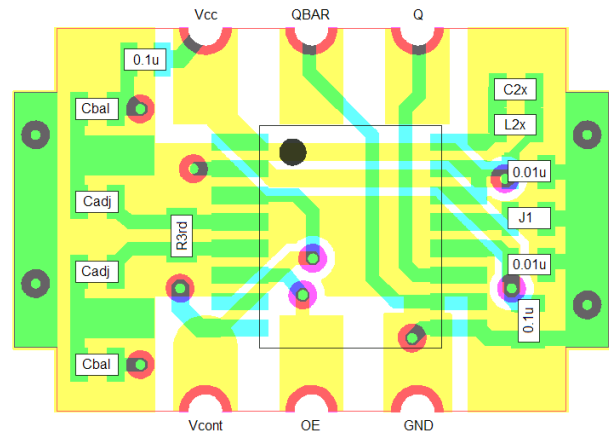
**L2X:** Reduce the PCB trace inductance to a minimum by placing L2X as physically close to their respective pins as possible. Also be sure to bypass each  $V_{DD}$  connection especially taking care to place a 0.01  $\mu\text{F}$  bypass at the  $V_{DD}$  side of L2X (see recommended layout).

**Crystal Connections:** Be sure to keep the ground plane under the crystal connections continuous so that the stray capacitance is consistent on both crystal connections. Also be sure to keep the crystal connections symmetrical with respect to one another and the crystal connection pins of the IC. If you chose to use a series capacitance and/or inductor to fine tune the crystal frequency, be sure to put symmetrical pads for this cap on both crystal pins (see Cadj in recommended layout), even if one of the capacitors will be a 0.01  $\mu\text{F}$  and the other is used to tune the frequency. To further maintain a symmetrical balance on a crystal that may have more internal Cstray on one pin or the other, place capacitor pads (Cbal) on each crystal lead to ground (see recommended layout). R3rd is only required if a 3<sup>rd</sup> overtone crystal is used.

**$V_{DD}$  and GND:** Bypass VDDANA and VDDBUF with separate bypass capacitors and if a  $V_{DD}$  plane is

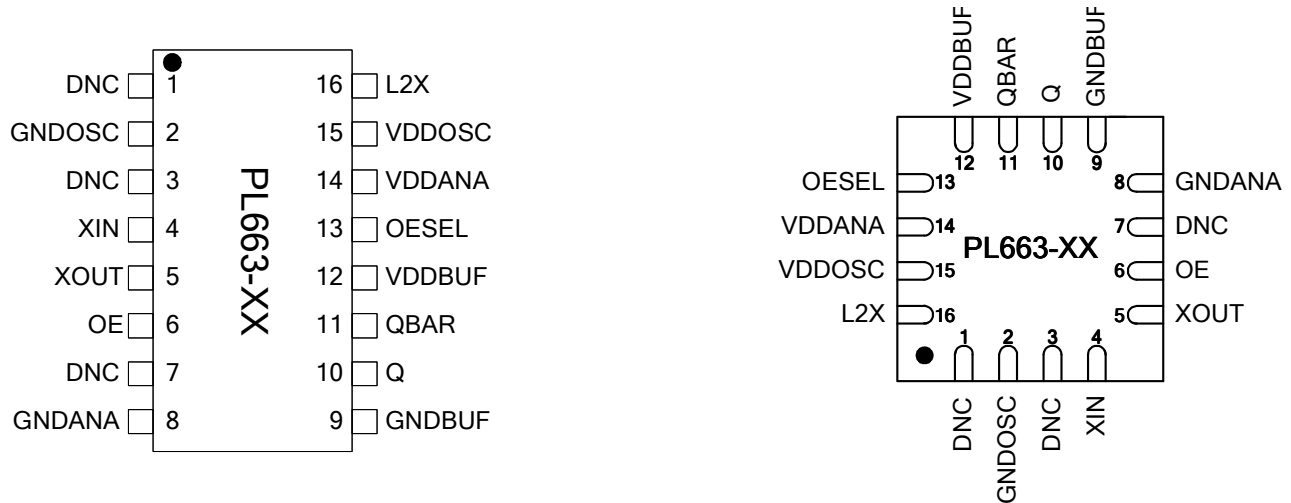
used, feed each bypass cap with its own via. Be sure to connect any ground pin including the bypass caps with short via connection to the ground plane.

**OESEL:** J1 is recommended so the same PCB layout can be used for both OESEL settings.



**PL663 (2x AFM) TSSOP Layout**

### PACKAGE PIN DESCRIPTION AND ASSIGNMENT



2x AFM Package Pin Out

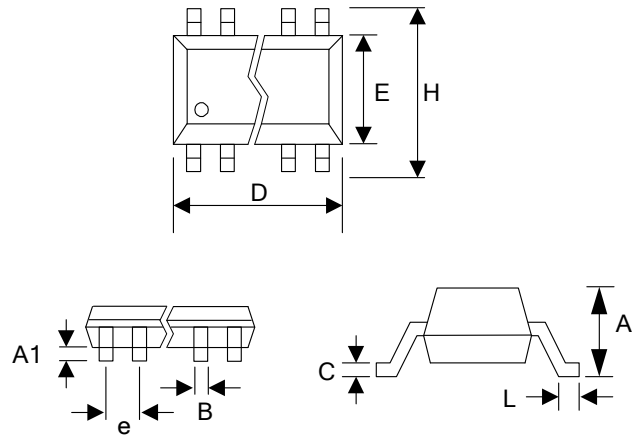
### PIN ASSIGNMENTS

Name	Pin #	Type	Description
DNC	1,3,7	I	Do Not Connect.
GNDOSC	2	P	GND connection for oscillator.
XIN	4	I	Input from crystal oscillator circuitry.
XOUT	5	O	Output from crystal oscillator circuitry.
OE	6	I	Output Enable input. See "OE LOGIC SELECTION TABLE".
GNDANA	8	P	GND connection.
GNDBUF	9	P	GND connection.
Q	10	O	PECL/LVDS/CMOS output.
QBAR	11	O	Complementary PECL/LVDS output or in-phase CMOS.
VDDBUF	12	P	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
OESEL	13	I	Selector input to choose the OE control logic (see "OE SELECTION TABLE"). If no connection is applied, value will be set to default through internal pull-down resistor.
VDDANA	14	P	VDD connection for analog circuitry. VDDANA should be separately decoupled from other VDDs whenever possible.
VDDOSC	15	P	VDD connection for oscillator. VDD should be separately decoupled from other VDDs whenever possible.
L2X	16	I	External inductor connection. The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between L2X and adjacent VDDOSC. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q.

### PACKAGE INFORMATION

#### 16 PIN TSSOP

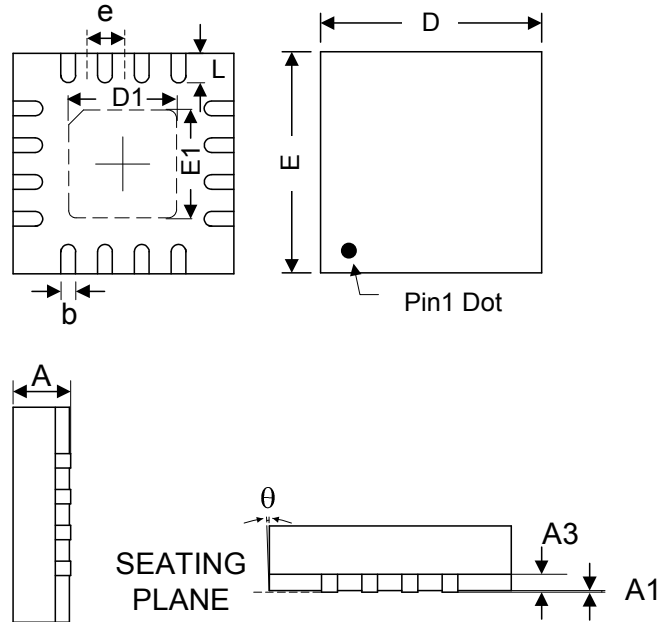
16 PIN TSSOP ( mm )		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



#### 16 PIN 3x3 QFN

##### QFN-16L

Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.203 Ref		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
L	0.250	0.300	0.350
e	0.50BSC		



### ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

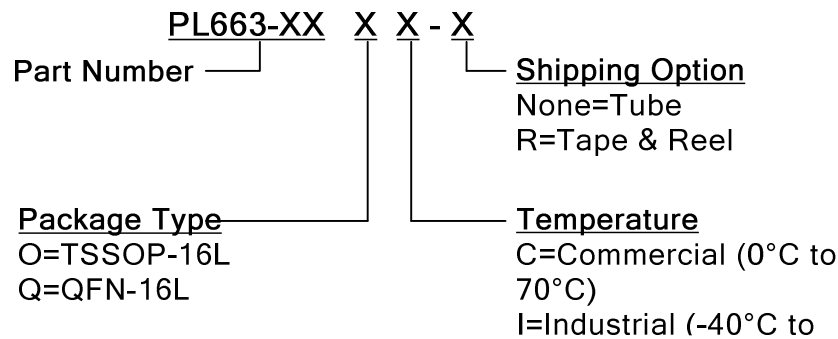
**To order parts, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

#### PART NUMBER

The order number for this device is a combination of the following:  
Part number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option
PL663-XXOC	P663-XX OC	TSSOP – Tube
PL663-XXOC-R	LLLLL	TSSOP – Tape and Reel
PL663-XXQC-R	P663 XX LLL	QFN – Tape and Reel
PL663-XXDC		Die – Waffle Pack

Note: See **Product Selector Guide** on page 3 for specific –XX part numbers.  
**LLLLL and LLL** designates lot number

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