

### PRODUCT DESCRIPTION

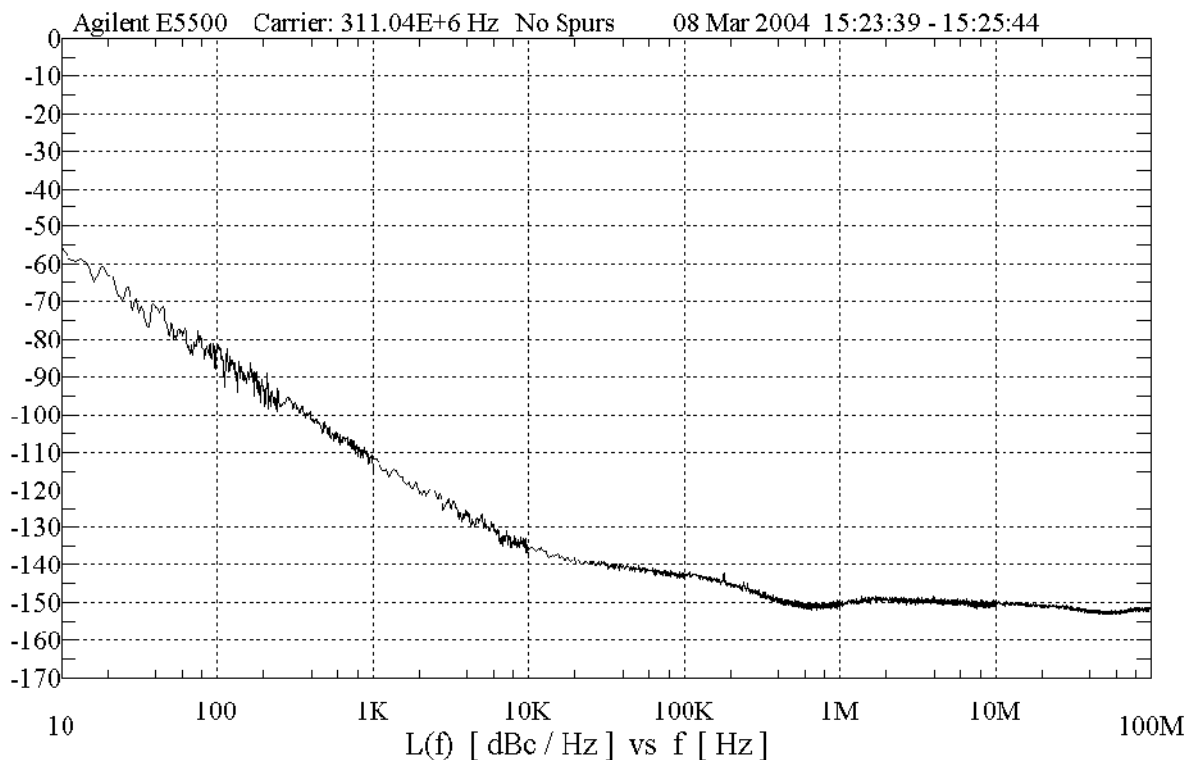
PhaseLink's Analog Frequency Multiplier (AFM) is the industry's first 'Balanced Oscillator' utilizing analog multiplication of the fundamental frequency (at double or quadruple frequency), combined with an attenuation of the fundamental of the reference crystal, without the use of a phase-locked loop (PLL), in CMOS technology.

PhaseLink's world's best performing AFM products can achieve up to 800 MHz output frequency with little jitter or phase noise deterioration. In addition, the low frequency input crystal requirement makes the AFMs the most affordable high-performance timing-source in the market.

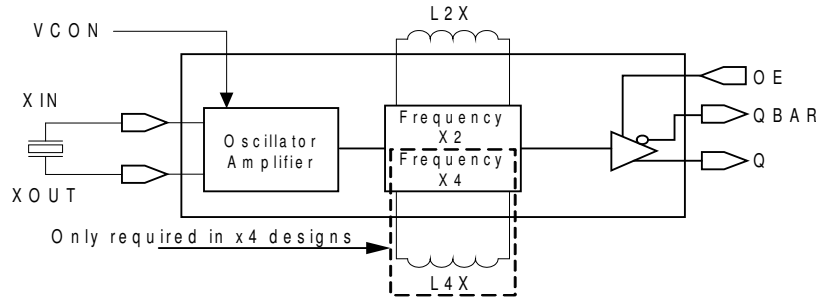
PL560/5-xx family of products utilize low-power CMOS technology and are housed in Green / RoHS compliant 16-pin TSSOP, and 16-pin 3x3 QFN packages.

- Non-PLL frequency multiplication
- Input frequency from 30-200 MHz
- Output frequency from 60-800 MHz
- Low phase noise and jitter (equivalent to fundamental crystal at the output frequency)
- Ultra-low jitter
  - RMS phase jitter < 0.25 ps (12kHz-20MHz)
  - RMS period jitter < 2.5 ps
- Low phase noise
  - -142 dBc/Hz @ 100kHz offset from 155.52 MHz
  - -150 dBc/Hz @ 10MHz offset from 155.52 MHz
- High linearity pull range (typ. 5%)
- +/- 120 PPM pullability VCXO
- Low input frequency eliminates the need for expensive crystals
- Differential output levels (PECL, LVDS), or single-ended CMOS
- Single 3.3V, ±10% power supply
- Optional industrial temperature range (-40°C to +85°C)
- Available in 16-pin Green/RoHS compliant TSSOP, and 3x3 QFN packages

### FEATURES



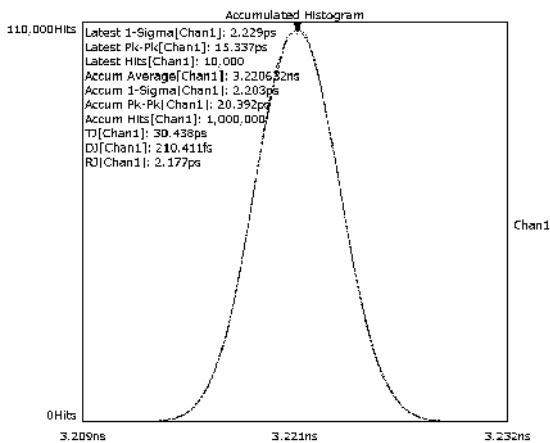
**Figure 1: 2x AFM Phase Noise at 311.04MHz**



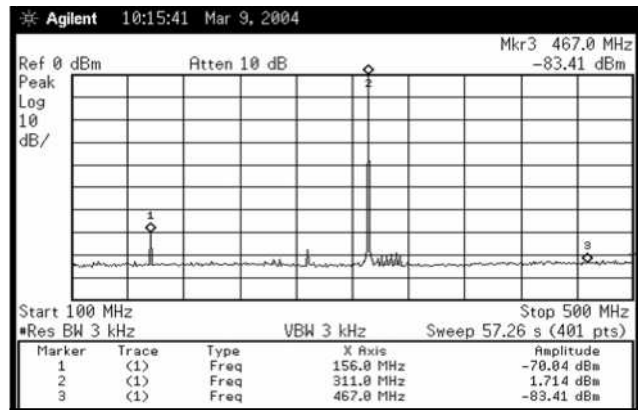
**Figure 2: Block Diagram of VCXO AFM**

Figure 3 shows the period jitter histogram of the 2x Analog Frequency Multiplier at 311.04 MHz, while Figure 4 shows the very low rejection levels of sub-harmonics that correspond to the exceptionally low jitter performance.

**Figure 3: Period Jitter Histogram at 311.04 MHz**  
Analog Frequency Multiplier (2x)  
with 155.52MHz crystal



**Figure 4: Spectrum Analysis at 311.04 MHz**  
Analog Frequency Multiplier (2x)  
with sub-harmonics below -72 dBc



### OE LOGIC SELECTION

OUTPUT	OESL	OE	Output State
LVPECL	0 (Default)	0 (Default)	Enabled
		1	Tri-state
	1	0	Tri-state
LVDS or LVCMOS	0 (Default)	1 (Default)	Enabled
		0	Tri-state
	1	0 (Default)	Enabled
		1	Tri-state

OESL and OE: Connect to VDD or leave floating to set to "1", connect to GND to set to "0". Internally set to default through pull-down / -up.

### PRODUCT SELECTION GUIDE

#### FREQUENCY VERSUS PHASE NOISE PERFORMANCE

Part Number	Input Frequency Range (MHz)	Analog Frequency Multiplication Factor	Output Frequency Range (MHz)	Output Type	Phase Noise at Frequency Offset From Carrier (dBc/Hz)							
					Carrier Freq. (MHz)	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	10MHz
PL560-37	30 - 80	4	120 - 320	LVC MOS	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-38	30 - 80	4	120 - 320	LVPECL	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-39	30 - 80	4	120 - 320	LVDS	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-47	30 - 80	2	60 - 160	LVC MOS	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-48	30 - 80	2	60 - 160	LVPECL	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-49	30 - 80	2	60 - 160	LVDS	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-68	75 - 200	2	150 - 400	LVPECL	311.04	-60	-85	-112	-135	-142	-150	-151
PL560-69	75 - 200	2	150 - 400	LVDS	311.04	-60	-85	-112	-135	-142	-150	-151

Phase noise was measured using Agilent E5500.

#### FREQUENCY VERSUS JITTER, AND SUB-HARMONIC PERFORMANCE

Part Number	Output Freq. (MHz)	RMS Period Jitter (ps)			Peak to Peak Period Jitter (ps)			RMS Accumulated (L.T.) Jitter (ps)			RMS Phase Jitter 12kHz to 20MHz (ps)			Spectral Specifications / Sub-harmonic Content (dBc), Frequency (MHz)						
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Carrier Freq. (Fc)	@ -75% (Fc)	@ -50% (Fc)	@ -25% (Fc)	@ +25% (Fc)	@ +50% (Fc)	@ +75% (Fc)
PL560-37	155		2.5	3		18	20			3		0.25		155.52	-75	-62			-65	-75
PL560-38	155		2.5	3		18	20			3		0.25		155.52	-75	-62			-65	-75
PL560-39	155		2.5	3		18	20			3		0.25		155.52	-75	-62			-65	-75
PL560-47	155		2.5	3		18	20			3		0.25		155.52		-68			-68	
PL560-48	155		2.5	3		18	20			3		0.25		155.52		-68			-68	
PL560-49	155		2.5	3		18	20			3		0.27		155.52		-68			-68	
PL560-68	311		2.5	3		18	20			3		0.18		311.04		-72			-85	
PL560-69	311		2.5	3		18	20			3		0.18		311.04		-72			-85	

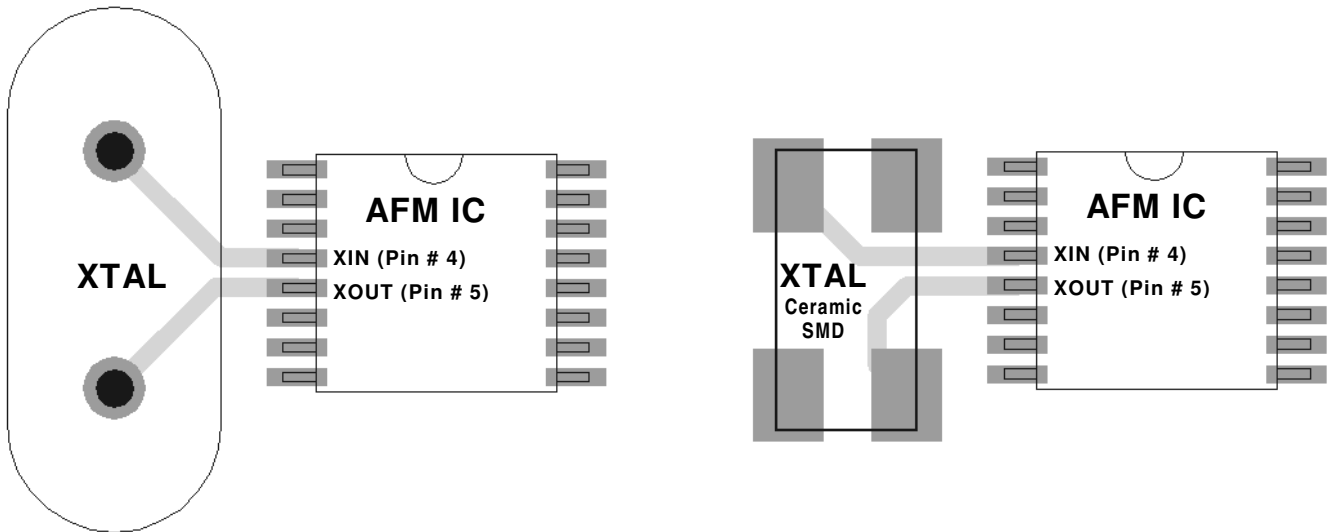
**Note:** Wavecrest data 10,000 hits. No filtering was used in jitter calculations.

Agilent 5500 was used for phase jitter measurements.

Spectral specifications were obtained using Agilent E7401A.

### CRYSTAL SPECIFICATIONS AND BOARD LAYOUT CONSIDERATIONS

#### BOARD LAYOUT CONSIDERATIONS



To minimize parasitic effects, and improve performance:

- Place the crystal as close as possible to the IC.
- Make the board traces that are connected to the crystal pins symmetrical.
- The board trace symmetry is important, as it reduces the negative parasitic effects to produce a clean frequency multiplication with low jitter. Parasitic effects reduce frequency pulling of the VCXO and increase jitter.

#### CRYSTAL SPECIFICATIONS & TUNING PERFORMANCE

CRYSTAL SPECIFICATIONS						TUNING PERFORMANCE					
PART NUMBER	CRYSTAL RESONATOR FREQUENCY (FXIN)	MODE	CL (xtal)		ESR (R <sub>E</sub> )	CRYSTAL			TUNING (Typical)		
			CONDI-TIONS	TYP	MAX	CRYSTAL FREQ (MHz)	C0	C1	C0/C1	VC: 1.65V → 0V	VC: 1.65V → 3.3V
PL565-08 PL560-09 PL560-68/69	75 to 200MHz	Funda-mental	At VCON = 1.65V	5pF	30	155.52	3.0pF	12.2fF	245	-145 ppm	+108 ppm
						155.52	1.8pF	5.7fF	316	-134 ppm	+87 ppm
PL560-37/38/39 PL560-47/48/49	30 to 80MHz	Funda-mental	At VCON = 1.65V	5pF	30	30.72	2.8pF	12.4fF	228	-167ppm	+176 ppm
						30.72	4.5pF	19.1fF	236	-163 ppm	+167 ppm
						38.88	5.1pF	20.9fF	242	-131 ppm	+98 ppm
						38.88	5.3pF	25.6fF	207	-157 ppm	+141 ppm
						77.76	2.0pF	6.7fF	305	-92 ppm	+110 ppm

**Note:** Non specified parameters can be chosen as standard values from crystal suppliers.

CL ratings larger than 5pF require a crystal frequency adjustment. Request detailed crystal specifications from PhaseLink.

### VOLTAGE CONTROL SPECIFICATION

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		XTAL $C_0 / C_1 < 300$	200			ppm
CLK Output Pullability		VCON= 1.65V, $\pm 1.65V$ XTAL $C_0 / C_1 < 300$	$\pm 100$	$\pm 120$		ppm
Linearity				5	10	%
VCON Input Impedance			130			k
VCON Modulation BW		$0V < VCON < 3.3V, -3dB$	16			kHz

### EXTERNAL COMPONENT VALUES

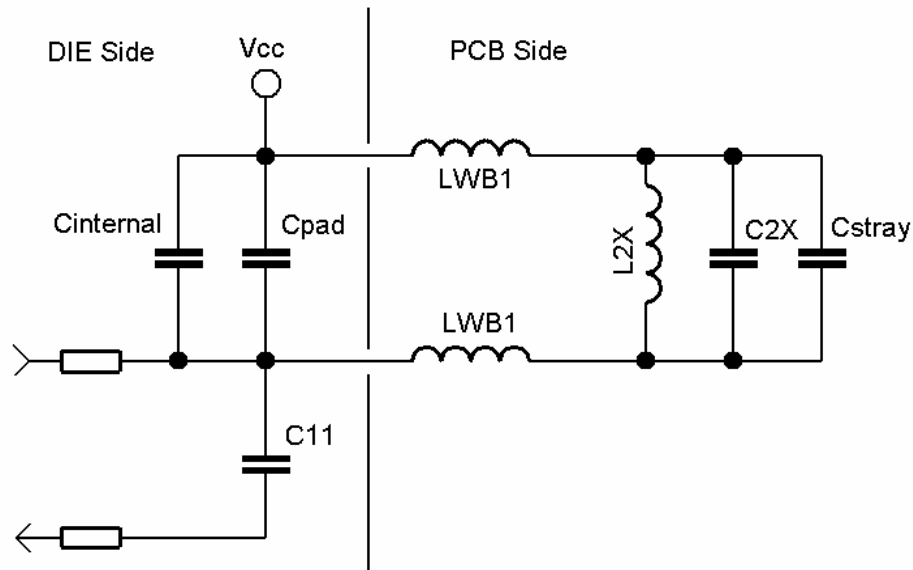
#### INDUCTOR VALUE OPTIMIZATION

The required inductor value(s) for the best performance depends on the operating frequency, and the board layout specifications. The listed values in this datasheet are based on the calculated parasitic values from PhaseLink's evaluation board design. These inductor values provide the user with a starting point to determine the optimum inductor values. Additional fine-tuning may be required to determine the optimal solution.

The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between L2X / L4X and adjacent VDDOSC pin. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q.

To assist with the inductor value optimization, PhaseLink has developed the "AFM Tuning Assistant" software. You can download this software from PhaseLink's web site ([www.phaselink.com](http://www.phaselink.com)). The software consists of two worksheets. The first worksheet (named L2) is used to fine-tune the 'L2' inductor value, and the second worksheet (named L4) is used for fine tuning of the 'L4' (used in 4x AFMs only) inductor value.

For those designs using PhaseLink's recommended board layout, you can use the "AFM Tuning Assistant" to determine the optimum values for the required inductors. This software is developed based on the parasitic information from PhaseLink's board layout and can be used to determine the required inductor and parallel capacitor (see LWB1 and Cstray parameters) values. For those employing a different board layout in their design, we recommend to use the parasitic information of their board layout to calculate the optimized inductor values. Please use the following fine tuning procedure:



**Figure 5: Diagram Representation of the Related System Inductance and Capacitance**

#### DIE SIDE

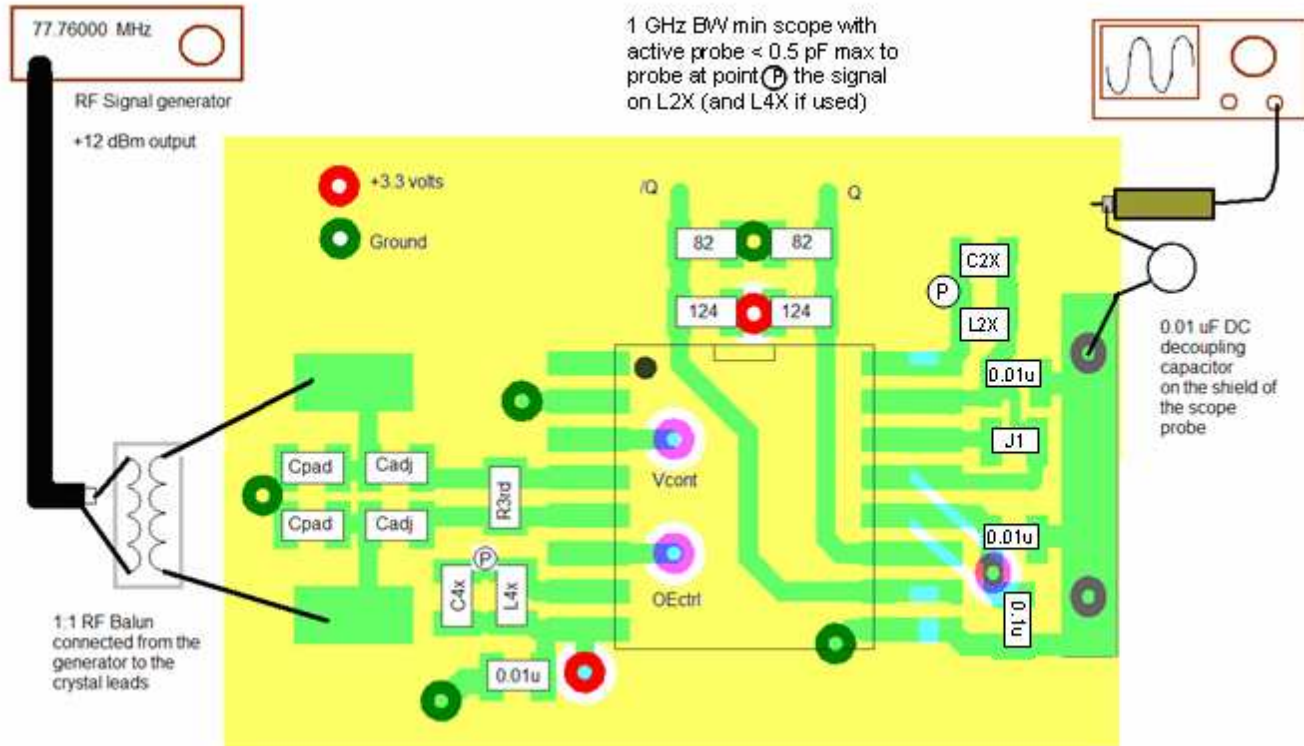
- Cinternal = Based on AFM device
- Cpad = 2.0 pF, Bond pad and its ESD circuitry
- C11 = 0.4 pF, The following amplifier stage

#### PCB side

- LWB1 = 2 nH, (2 places), Stray inductance
- Cstray = 1.0 pF, Stray capacitance
- L2X (L4X) = 2x or 4x inductor
- C2X (C4X) = range (0.1 to 2.7 pF), Fine tune inductor if used

- There are two default variables that normally will not need to be modified. These are Cpad, and C11 and are found in cells B22 and B27 of 'AFM Tuning Assistant', respectively.
- LWB1 is the combined stray inductance in the layout. The DIE wire bond is ~ 0.6 nH and in the case of a leaded part an additional 1.0 nH is added. Your layout inductance must be added to these. There are 2 of these and they are assumed to be approximately symmetrical so you only need to enter this inductance once in cell B23.
- Enter the stray parasitic capacitance into cell B26. An additional 0.5 pF must be added to this value if a leaded part is used.
- Enter the appropriate value for Cinternal into B21 based on the device used (see column D). Use the 'AFM Tuning Assistant' software to calculate L2X (and C2X if used) for your resonance frequency.
- For 4X AFMs, repeat the same procedure in the L4X worksheet.
- See the examples in the following section.

### DETERMINING STRAY L's AND C's IN A LAYOUT



**Figure 6: Diagram Representation of the Board Layout**

Lets take the PL560-38 (4x VCXO) for example. This takes a crystal input in the range of 30 to 80 MHz and multiplies it to an output of 120 to 320 MHz. To determine the stray L's and C's of the layout we will assemble two test units. One AFM will be tuned to the lower range of the device (120 MHz), and the other to the upper range of the device (320 MHz).

**120 MHz AFM Tuning:** Using the "AFM Tuning Assistant" find the PL560-3x in the L2X worksheet. Enter the Cinternal value found next to it into cell B21. In cell B24 enter the closest standard inductor value (see CoilCraft 0603CS series for example) to achieve the closest peak frequency to 60 MHz. Repeat the same procedure for L4X at 120 MHz.

**Results: L2X = 180 nH, L4X = 82 nH.**

**320 MHz AFM tuning:** Repeat the previous procedure for L2X at 120 MHz and L4X at 320 MHz.

**Results: L2X = 24 nH, L4X = 10 nH.**

Proceed and assemble the test units.

**Measuring 120 MHz L2X:** Connect the RF generator and scope probe as shown in Figure 6, above. While power is applied to the PCB, set the generator output to +12 dBm and the frequency to 30 MHz. Since this is the 2x port, the scope will show 60 MHz with ~ 3V pk-pk amplitude. Vary the generator above and below 30 MHz until the amplitude on the scope is maximum and record the generator frequency. For example, the peak is recorded at 29.8x2 or 59.6 MHz.

**Measuring 320 MHz L2X:** Connect the RF generator and scope probe as shown in Figure 6, above. While power is applied to the PCB, set the generator output to +12 dBm and the frequency to 80 MHz. Since this is the 2x port the scope will show 160 MHz with ~ 3V pk-pk amplitude. Vary the generator above and below 80 MHz until the amplitude on the scope is maximum and record the generator frequency. For example, the peak is recorded at 78.0 x 2 = 156 MHz

In the AFM Tuning Assistant, add the scope's probe capacitance to the Cstray cell. For our example 0.5 pF + 1.0 pF = 1.5 pF. With L2X at 24 nH adjust LWB1 (cell B23) until the peak frequency reads 156 MHz. Next replace the L2X value with 180 nH and see if it peaks at 59.6 MHz. If it does not, adjust Cstray until 59.4 MHz is achieved. Again enter 24 nH for L2X and fine tune LWB1 for 156 MHz.

**Results: LWB1 = 1.6 nH, Cstray = 2.9 pF - 0.5 pF = 2.4 pF (subtract scope probe stray capacitance)**

Repeat the same steps for the L4X: Set the generator to 80 MHz. The 82 nH peaks at 118 MHz and the 10 nH peaks at 304 MHz.

**Results: LWB1 = 1.8 nH, Cstray = 2.5 pF - 0.5 pF = 2.0 pF (subtract scope probe stray capacitance)**

### Internal Capacitor Selection by Device

Device Number	Cinternal (pF)	
	2X	4X
P565-08	7.625	6.250
P560-09	7.625	6.250
P560-3x	34.125	16.500
P560-4x	34.125	
P560-6x	7.625	

### ELECTRICAL SPECIFICATIONS

#### ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, DC	$V_I$	GND-0.5	$V_{DD}+0.5$	V
Output Voltage, DC	$V_O$	GND-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature, Industrial	$T_{A_I}$	-40	+85	°C
Ambient Operating Temperature, Commercial	$T_{A_C}$	0	+70	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

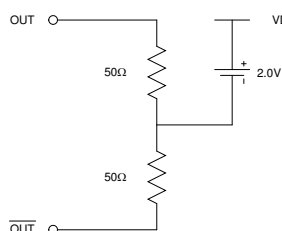
Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

#### LVPECL ELECTRICAL CHARACTERISTICS

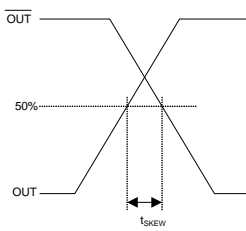
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, loaded outputs	$I_{DD}$	$F_{out} = 622.08\text{MHz}$ , 15pF Load		75	80	mA
Operating Voltage*	$V_{DD}$		2.97		3.63	V
Output Clock Duty Cycle		@ $V_{DD} - 1.3\text{V}$	45	50	55	%
Short Circuit Current				$\pm 50$		mA
Output High Voltage	$V_{OH}$	$R_L = 50 \text{ to}$ $(V_{DD} - 2\text{V})$	$V_{DD}-1.025$			V
Output Low Voltage	$V_{OL}$			$V_{DD}-1.620$		V
Clock Rise Time	$t_r$	@ 20/80%		0.25	0.45	ns
Clock Fall Time	$t_f$	@ 80/20%		0.25	0.45	ns

\*Contact PhaseLink for lower operating voltages

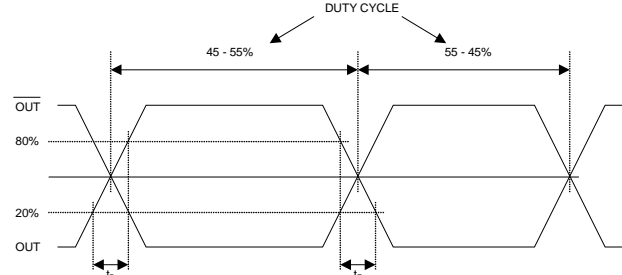
LVPECL Levels Test Circuit



LVPECL Output Skew



LVPECL Transition Time Waveform

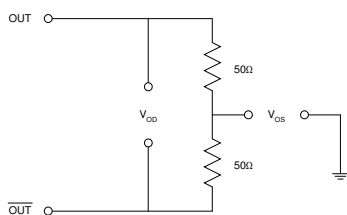


### LVDS ELECTRICAL CHARACTERISTICS

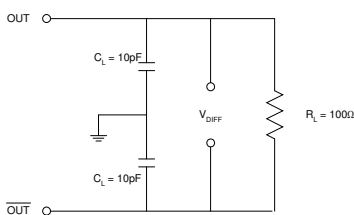
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, loaded outputs	$I_{DD}$	$F_{out} = 622.08\text{MHz}$ , 15pF Load		55	60	mA
Operating Voltage*	$V_{DD}$		2.97		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	45	50	55	%
Short Circuit Current				$\pm 50$		mA
Output Differential Voltage	$V_{OD}$	$R_L = 100$ (see figure)	247	355	454	mV
VDD Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA
Differential Clock Rise Time	$t_r$	$R_L = 100$ $CL = 10\text{ pF}$ (see figure)	0.2	0.5	0.7	ns
Differential Clock Fall Time	$t_f$		0.2	0.5	0.7	ns

\*Contact PhaseLink for lower operating voltages

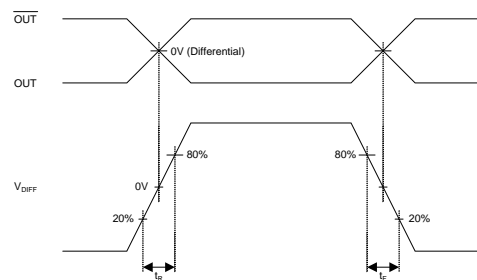
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



### LVC MOS ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, loaded outputs	$I_{DD}$	At 100MHz, 15pF load		16	20	mA
Operating Voltage*	$V_{DD}$		2.97		3.63	V
Output High Voltage (LVTTL)	$V_{OH3.3}$	$I_{OH} = -8.5\text{mA}$ , 3.3V	2.4			V
Output Low Voltage (LVTTL)	$V_{OL3.3}$	$I_{OL} = 8.5\text{mA}$ , 3.3V			0.4	V
Output High Voltage (LVCMOS)	$V_{OHC3.3}$	$I_{OH} = -4\text{mA}$ , 3.3V	$V_{DD} - 0.4$			V
Output Drive Current	$I_{OSD3.3}$	$V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$ (per output), 3.3V		8.5		mA
Output Clock Rise/Fall Time	$T_r, T_f$	10% / 90% $V_{DD}$ , 10 pF load		1.2	1.6	ns
Output Clock Duty Cycle		Measured @ 50% $V_{DD}$	45	50	55	%

\*Contact PhaseLink for lower operating voltages

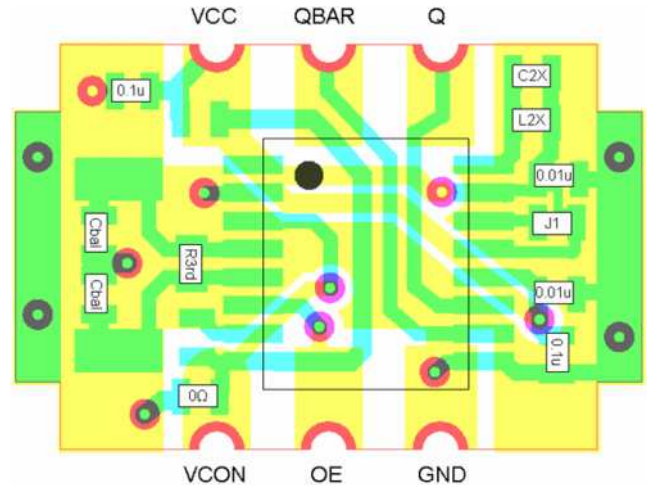
### BOARD DESIGN AND LAYOUT CONSIDERATIONS

**L2X and L4X:** Try to reduce the PCB trace inductance to a minimum by placing L2X and L4X as physically close to their respective pins as possible. Also be sure to bypass each Vdd connection especially taking care to place a 0.01 uF bypass at the Vdd side of L2X and L4X (see recommended layout).

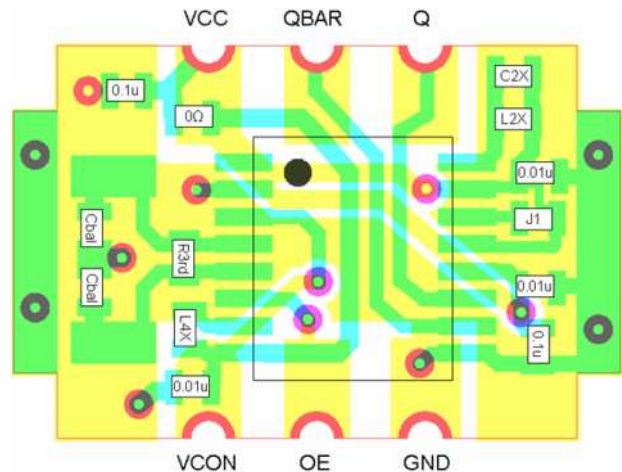
**Crystal connections:** Be sure to keep the ground plane under the crystal connections continuous so that the stray capacitance is consistent on both crystal connections. Also be sure to keep the crystal connections symmetrical with respect to one another and the crystal connection pins of the IC. If you chose to use a series capacitance and or inductor to fine tune the crystal frequency be sure to put symmetrical pads for this cap on both crystal pins (see Cadj in recommended layout), even if one of the capacitors will be a 0.01 uF and the other is used to tune the frequency. To further maintain a symmetrical balance on a crystal that may have more internal Cstray on one pin or the other, place capacitor pads (Cbal) on each crystal lead to ground (see recommended layout). R3rd is only required if a 3<sup>rd</sup> overtone crystal is used.

**V<sub>DD</sub> and GND:** Bypass VDDANA and VDDBUF with separate bypass capacitors and if a V<sub>DD</sub> plane is used, feed each bypass cap with its own via. Be sure to connect any ground pin including the bypass caps with short via connections to the ground plane.

**OESEL:** J1 is recommended so the same PCB layout can be used for both OESEL settings.

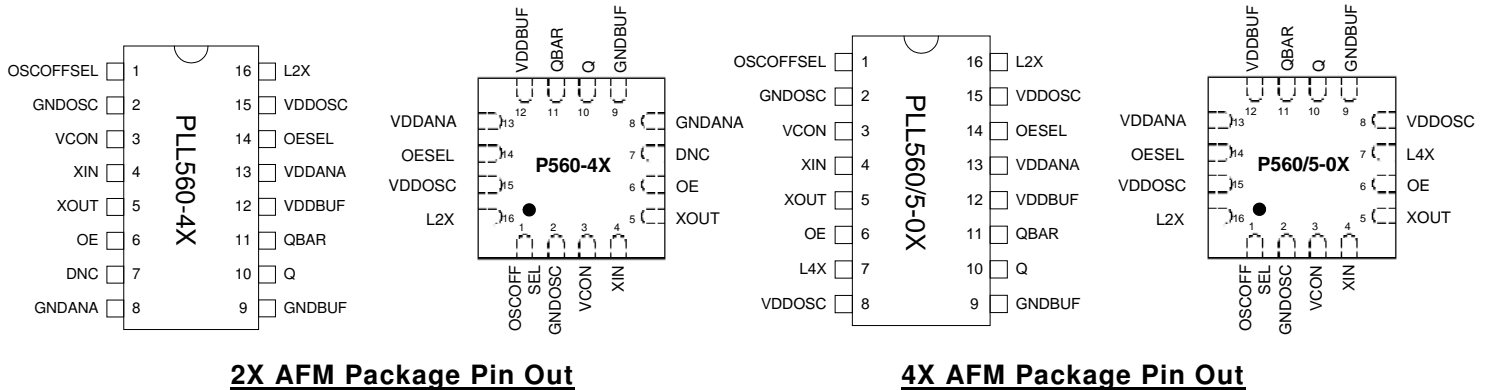


**2X Layout (TSSOP)**



**4X Layout (TSSOP)**

### PACKAGE PIN DESCRIPTION AND ASSIGNMENT



### PIN ASSIGNMENTS

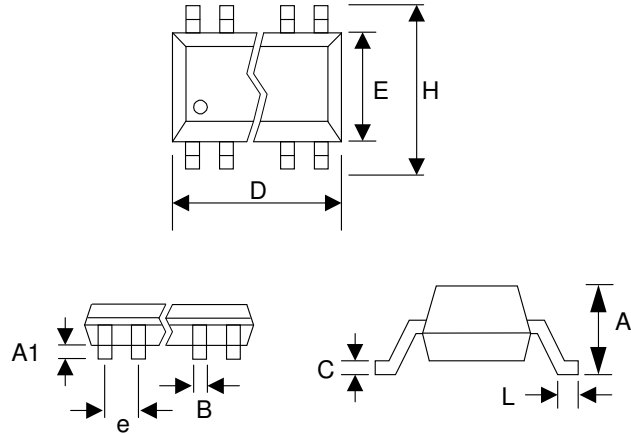
Name	Pin#	Type	Product	Description
OSCOFFSEL	1	I	2X & 4X	Set to "0" (GND) to choose to turn off the oscillator when outputs are disabled (OE). Default (no connect) is OSC always on.
GNDOSC	2	P	2X & 4X	GND connection for oscillator circuitry.
VCON	3	I	2X & 4X	Control Voltage input. Use this pin to change the output frequency by varying the applied Control Voltage.
XIN	4	I	2X & 4X	Input from crystal oscillator circuitry.
XOUT	5	O	2X & 4X	Output from crystal oscillator circuitry.
OE	6	I	2X & 4X	Output Enable input (see "OE LOGIC SELECTION TABLE").
DNC	7	I	2X	Do Not Connect.
L4X			4X	External inductor connection. See INDUCTOR VALUE OPTIMIZATION on page 5. This inductor is used with 4X AFMs.
GNDANA	8	P	2X	GND connection.
VDDOSC*			4X	V <sub>DD</sub> connection for oscillator circuitry.
GNDBUF	9	P	2X & 4X	GND connection for output buffer circuitry.
Q	10	O	2X & 4X	PECL/LVDS or CMOS output.
QBAR	11	O	2X & 4X	Complementary PECL/LVDS output or in phase CMOS.
VDDBUF*	12	P	2X & 4X	V <sub>DD</sub> connection for output buffer circuitry.
VDDANA*	13	P	2X & 4X	V <sub>DD</sub> connection for analog circuitry.
OESEL	14	I	2X & 4X	Selector input to choose the OE control logic (see "OE SELECTION TABLE"). Internal pull-down.
VDDOSC*	15	P	2X & 4X	V <sub>DD</sub> connection for oscillator circuitry.
L2X	16	I	2X & 4X	External inductor connection. See INDUCTOR VALUE OPTIMIZATION on page 5.

\* All V<sub>DD</sub> pins should be separately decoupled whenever possible.

### PACKAGE INFORMATION

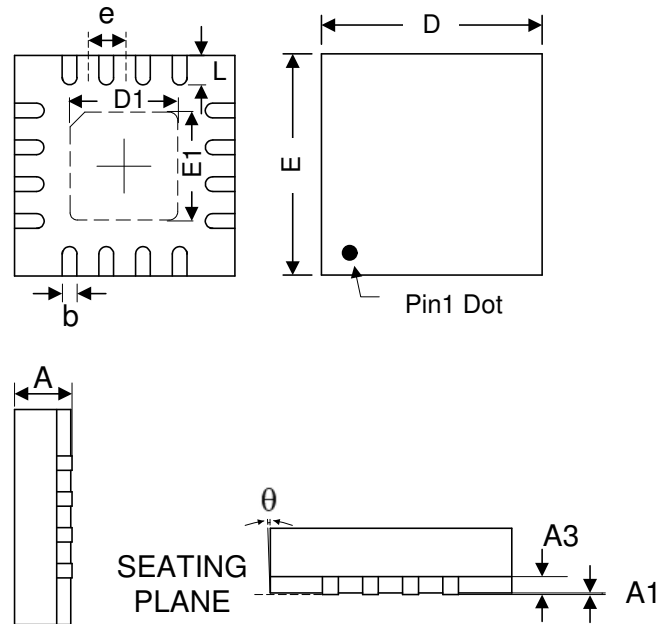
16 PIN TSSOP ( mm )

Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



QFN-16L

Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
L	0.250	0.300	0.350
e	0.50BSC		



### ORDERING INFORMATION

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information

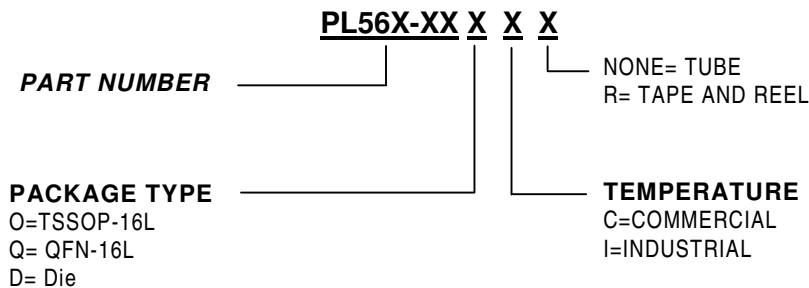
**For part ordering, please contact our Sales Department:**

2880 Zanker Rd., San Jose, CA 95134, USA

Tel: (408) 571-1668 Fax: (408) 571-1688

#### PART NUMBER

The order number for this device is a combination of the following:  
Part number, Package type and Operating temperature range



Order Number	Marking	Package Option*
PL560-XXDC	-	Die Only
PL560/5-XXOC	P560/5-XX OC	TSSOP – Tube
PL560/5-XXOC-R	LLLLL	TSSOP – Tape and Reel
PL560/5-XXQC	P560/5 XX(I)	QFN – Tube
PL560/5-XXQC-R	LLL	QFN – Tape and Reel

Marking Notes : "LLL", "LLLLL" represents the production lot number

furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

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