PhaseLink Corporation

(Preliminary) **Analog Frequency Multiplier**

PL565-78 for 491.52 MHz Wireless Base Station VCXO Family

PRODUCT DESCRIPTION

PhaseLink's Analog Frequency Multiplier (AFM) is the industry's first 'Balanced Oscillator' utilizing analog multiplication of the fundamental frequency (at quadruple frequency), combined with an attenuation of the fundamental of the reference crystal, without the use of a phase-locked loop (PLL), in CMOS technology.

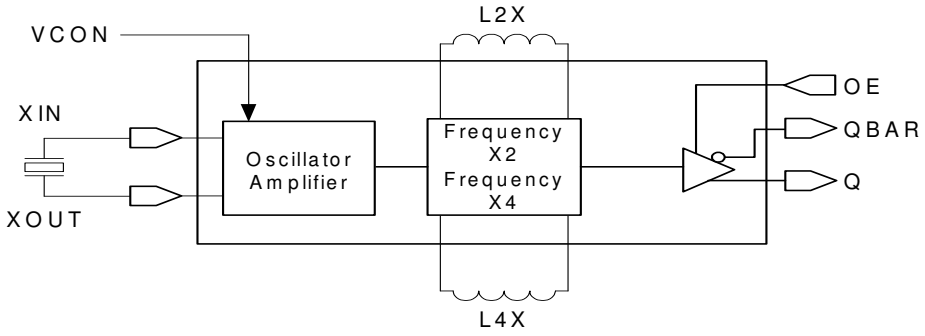
PhaseLink's world's best performing AFM products can achieve up to 800 MHz output frequency with little jitter or phase noise deterioration.

PL565-78, however, is custom designed to meet the stringent phase noise requirements of wireless base station applications, operating at 491.52 MHz.

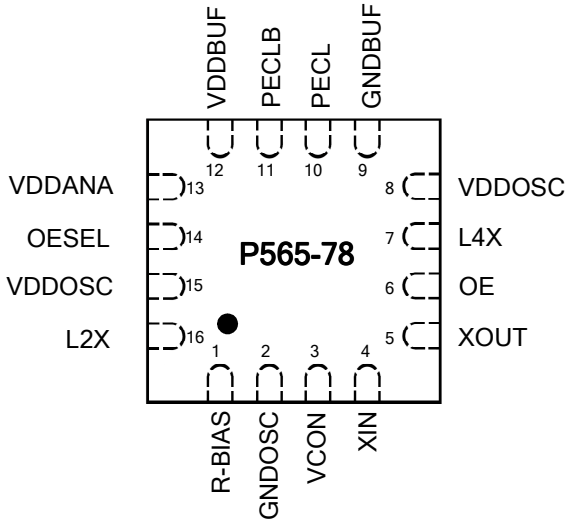
FEATURES

- Non-PLL frequency multiplication by 4.
- Input frequency: 122.88 MHz
- Output frequency: 491.52 MHz
- Low phase noise and jitter (equivalent to fundamental crystal at the output frequency)
- Ultra-low jitter
  - RMS phase jitter < 100 fs (12kHz-20MHz)
  - RMS random period jitter < 2 ps
- Low phase noise
  - -65 dBc/Hz @10Hz offset from the carrier
  - -96 dBc/Hz @100Hz offset from the carrier
- High linearity pull range (typ. 5%)
- VCXO, set pullability ±100ppm ~ ±150ppm
- Differential output levels: LVPECL
- Single 3.3V, ±10% power supply
- Operating temperature range: -40°C to +85°C
- Available in 3x3mm QFN-16L package.

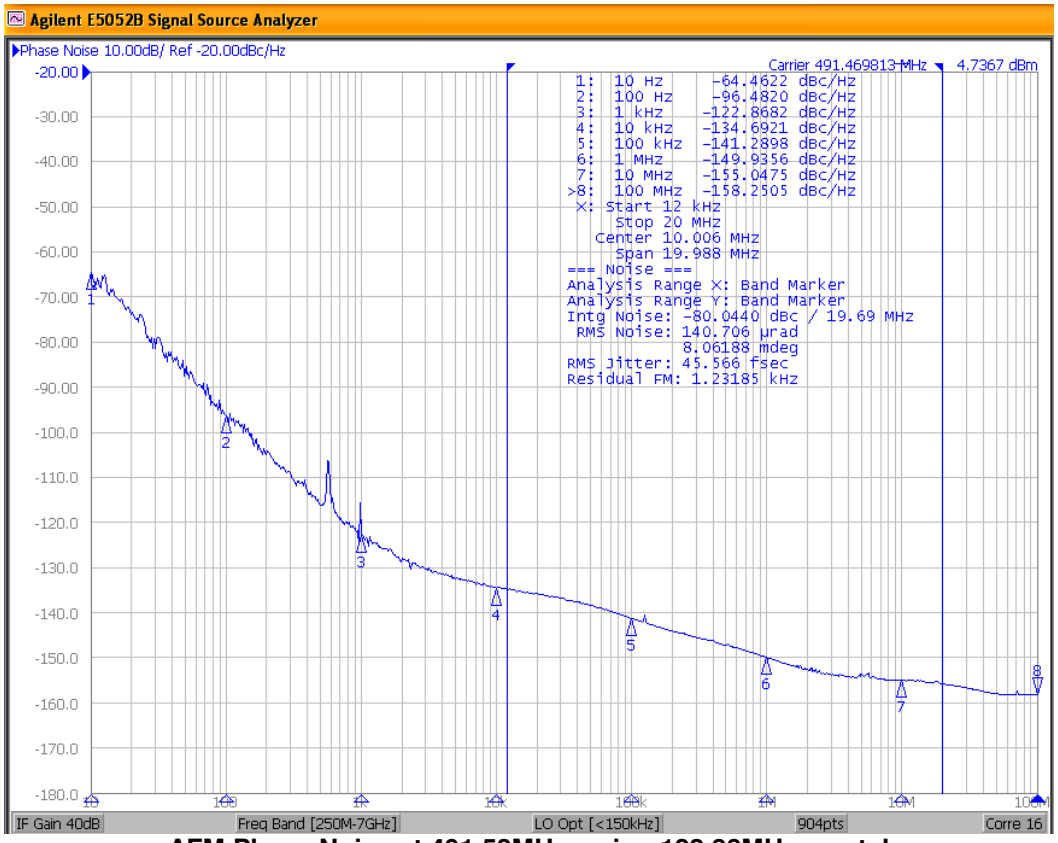
PL565-78 Block Diagram



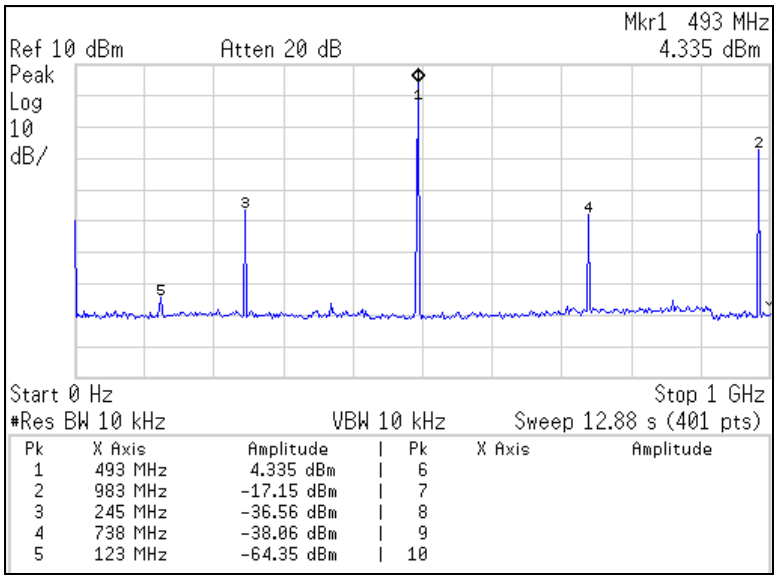
PIN ASSIGNMENT AND DESCRIPTION



Name	QFN Pin #	Type	Description
R-BIAS	1	I	External bias resistor connection
GNDOSC	2	P	GND connection
VCON	3	I	Control voltage input
XIN	4	I	Crystal Input pad
XOUT	5	O	Crystal Output pad
OE	6	I	Output Enable input
L4X	7	I	External inductor connection
VDDOSC	8	P	VDD connection
GNDBUF	9	P	GND connection
PECL	10	O	LVPECL output
PECLB	11	O	LVPECL complementary output
VDDBUF	12	P	VDD connection
VDDANA	13	P	VDD connection
OESEL	14	I	OE style selection pin
VDDOSC	15	P	VDD connection
L2X	16	I	External inductor connection



AFM Phase Noise at 491.52MHz, using 122.88MHz crystal



AFM Spectrum at 491.52MHz, using 122.88MHz crystal

The analog frequency multiplication preserves the low phase noise of the quartz crystal oscillator while keeping unwanted sub harmonics from the multiplication at very low levels. Sub harmonics appear only at large distance from the carrier, far outside the loop bandwidth of a PLL that uses the AFM signal to multiply up further to a multiple GHz network clock. This means the impact of the sub harmonics on the application is negligible.

PHASE NOISE PERFORMANCE

Part Number	Input Freq. (MHz)	Output Freq. (MHz)	Phase Noise at Frequency Offset From Carrier (dBc/Hz)							Phase Jitter 12KHz ~ 20MHz (ps)
			10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	10MHz	
PL565-78	122.88	491.52	-64	-96	-123	-135	-141	-150	-155	0.05

Phase noise was measured using Agilent E5052B.

SUB-HARMONIC PERFORMANCE

Part Number	Input Frequency (MHz)	Output Frequency (MHz)	Spectral Specifications / Sub-harmonic Content (dBc), Freq. (MHz)					
			@ -75%(Fc)	@ -50%(Fc)	@ -25%(Fc)	@ +25%(Fc)	@ +50%(Fc)	@ +75%(Fc)
PL565-78	122.88	491.52	-60	-40	-70	-70	-40	-70

Note: Spectral specifications were obtained using Agilent E7401A

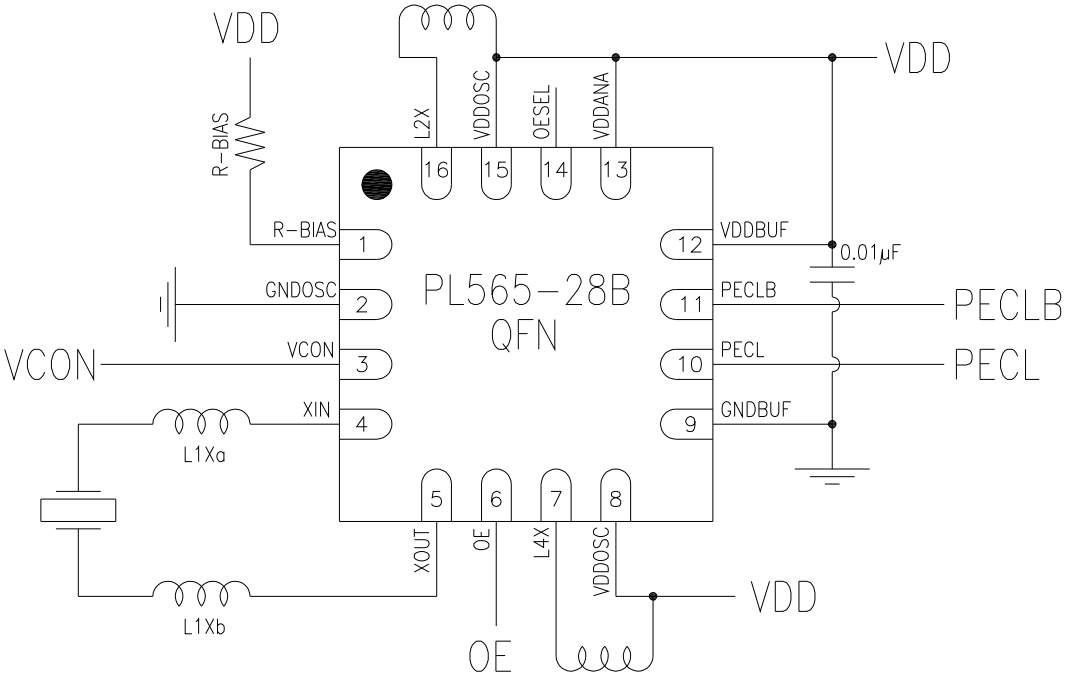
AFM MULTIPLYING TECHNIQUE

The analog frequency multiplication is achieved through a “squaring” operation.

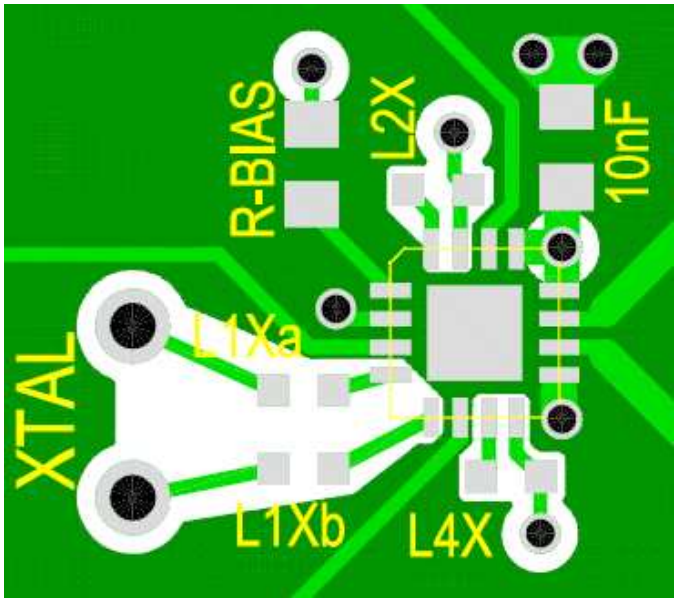
The math is as follows: $SIN^2(x) = 0.5 - 0.5 \times COS(2x)$

A very important property of this processing is that the result is a pure sine wave with double frequency. In theory there are no sub harmonics but in practice the squaring operation is not perfect and a low level of sub harmonics is present anyway. The key is that the resulting sub harmonics are very low and simple filtering with only one inductor per squarer is adequate for excellent performance.

APPLICATION CIRCUIT



RECOMMENDED PCB LAYOUT



- Avoid ground planes underneath the crystal and inductor traces to limit parasitic capacitance.
- Add bypass capacitor close to VDDBUF pin.
- Avoid bypass capacitors near VDDOSC pins to lower cross-talk of unwanted frequencies.
- L1X(a,b) can be used to increase the VCXO pulling range. Using ferrite core inductors limits the oscillation amplitude which can have a positive effect on phase noise.
- L2X and L4X tune the frequency multiplier tank circuits. They need to be wire wound inductors with high Q-factor, preferably >20.
- The large center pad is the “thermal relief” pad and can be connected to ground.

TYPICAL COMPONENT VALUES FOR 491.52MHz OPERATION:

L1Xa = L1Xb = 100nH for typical +140/-130ppm Frequency Pulling with Crystal C1=6fF and C0=2pF
L2X = 36 nH , Coilcraft 0402CS or 0402HP
L4X = 9.5 nH , Coilcraft 0402CS or 0402HP
R-BIAS = 300 Ω

INDUCTOR VALUE OPTIMIZATION

The required inductor values for the best performance depend on the operating frequency, and the board layout or module specifications. The listed values in this datasheet are based on the calculated parasitic values from PhaseLink's evaluation board design. These inductor values provide the user with a starting point to determine the optimum inductor values. Additional fine-tuning may be required to determine the optimal solution.

The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between L2X / L4X and adjacent VDDOSC pin. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q.

To assist with the inductor value optimization, PhaseLink has developed AFM "Tuning Assistant" documents. You can download these documents from PhaseLink's web site (www.phaselink.com). The documents consist of tables with recommended inductor values for certain output frequency ranges.

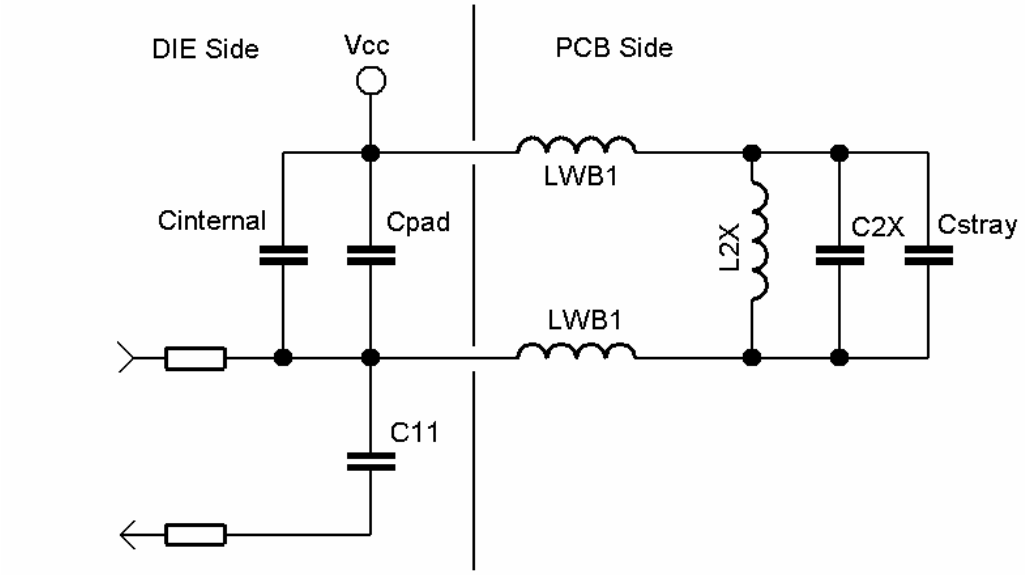


Figure 10: Diagram Representation of the Related System Inductance and Capacitance

DIE SIDE
- Cinternal at L2X = 7.625 pF , at L4X = 6.25 pF
- Cpad = 1.0 pF, Bond pad and its ESD circuitry
- C11 = 0.4 pF, The following amplifier stage

PCB side
- LWB1 = 2 nH, (2 places), Stray inductance
- Cstray = 0.5 pF, Stray capacitance
- L2X (L4X) = 2x or 4x inductor
- C2X (C4X) = range (0.1 to 2.7 pF), Fine tune the tank, if used.

Work out the resonance of this network and you have a good first guess for the required inductor values for optimum performance. Non-linear behavior at large signal amplitudes can shift the tank resonance significantly, especially at the L2X side, to a lower frequency than the calculation suggests. The Tuning Assistant documents are based upon actual lab tests and are corrected for the non-linear behavior.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, DC	V_I	GND-0.5	V_{DD}+0.5	V
Output Voltage, DC	V_O	GND-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature, Industrial	T_{A_I}	-40	+85	°C
Ambient Operating Temperature, Commercial	T_{A_C}	0	+70	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (HBM)			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

VOLTAGE CONTROL SPECIFICATION

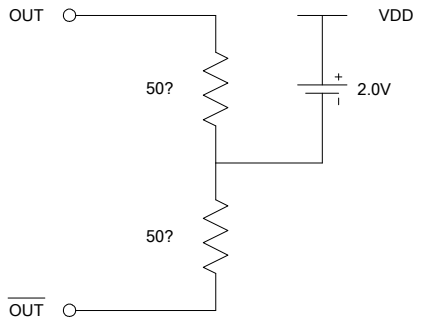
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range*		XTAL C_0/C_1 <300	200			ppm
CLK Output Pullability*		VCON= 1.65V, ± 1.65V XTAL C_0/C_1 <300	±100	±120		ppm
Linearity				5	10	%
VCON Input Impedance			130			kΩ
VCON Modulation BW		0V < VCON < 3.3V, -3dB		40		kHz

* Note: The VCXO Tuning Range and Pullability can be controlled with the value for inductor L1X. See Tuning Assistant document for a guide to chose the L1X value based upon crystal frequency and motional parameters.

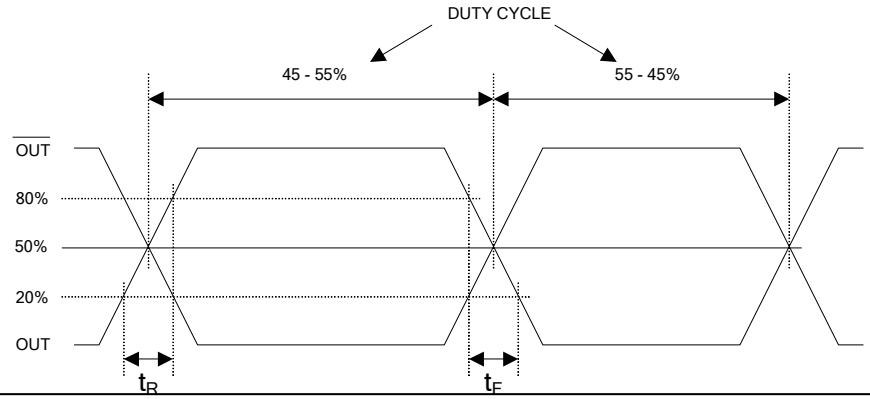
LVPECL ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, loaded outputs	I_{DD}	Fout = 491.52MHz		75	80	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@V_{DD}–1.3V	45	50	55	%
Short Circuit Current				±50		mA
Output High Voltage	V_{OH}	R_L = 50Ω to (V_{DD} – 2V)	V_{DD}-1.025			V
Output Low Voltage	V_{OL}				V_{DD}-1.620	V
Clock Rise Time	t_r	@ 20/80%		0.25	0.45	ns
Clock Fall Time	t_f	@ 80/20%		0.25	0.45	ns

LVPECL Levels Test Circuit



LVPECL Transistion Time Waveform



OE LOGIC SELECTION

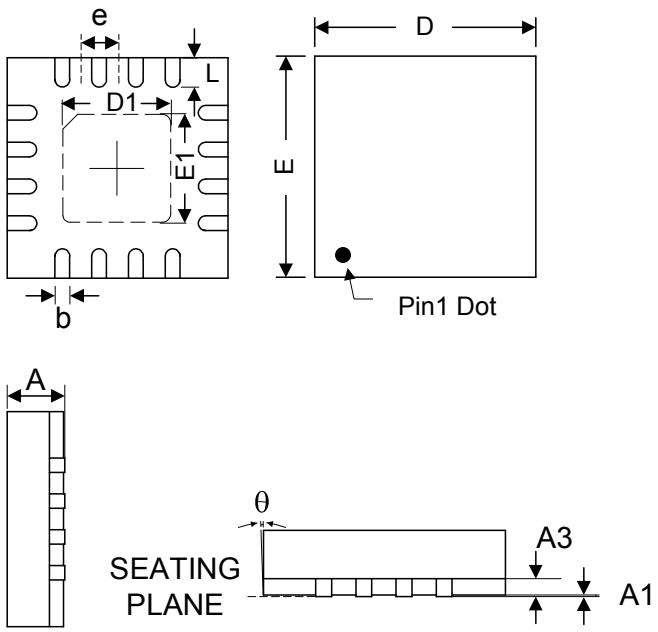
OESEL	OE	Output State
0 (Default)	0 (Default)	Enabled
	1	Tri-state
1	0	Tri-state
	1 (Default)	Enabled

0 (Default): Connect to GND or leave floating to set to “0”. Internal pull-down.
1 (Default): Connect to VDD or leave floating to set to “1”. Internal pull-up.
0: Connect to GND to set to “0”. 1: Connect to VDD to set to “1”.

PACKAGE INFORMATION

QFN-16L

Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20	
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
L	0.250	0.300	0.350
e		0.50BSC	

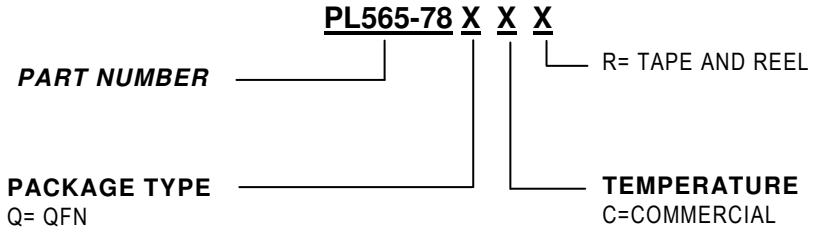


ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2880 Zanker Rd., San Jose, CA 95134, USA
Tel: (408) 571-1668 Fax: (408) 571-1688

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



Order Number	Marking	Package Option*
PL565-78QC	P565 78 LLL	QFN – Tape & Reel

*Note: LLL represent the production lot number