PLL520-30

PECL and LVDS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

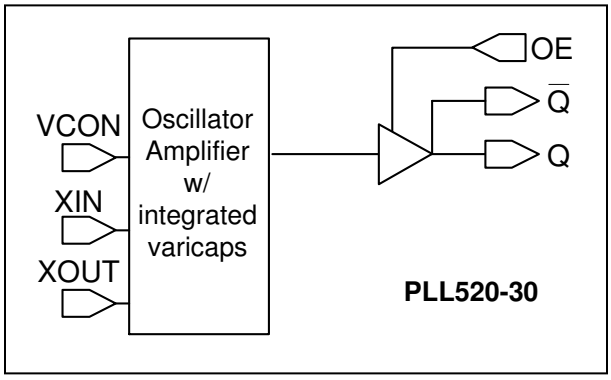
FEATURES

- 65MHz to 130MHz Fundamental Mode Crystals.
- Output range (no PLL):
  - 65MHz – 130MHz (3.3V).
  - 65MHz – 105MHz (2.5V).
- Low Injection Power for crystal 50uW.
- Complementary outputs: PECL or LVDS.
- Selectable OE Logic
- Integrated variable capacitors.
- Supports 2.5V or 3.3V-Power Supply.
- Available in die form.
- Thickness 10 mil.

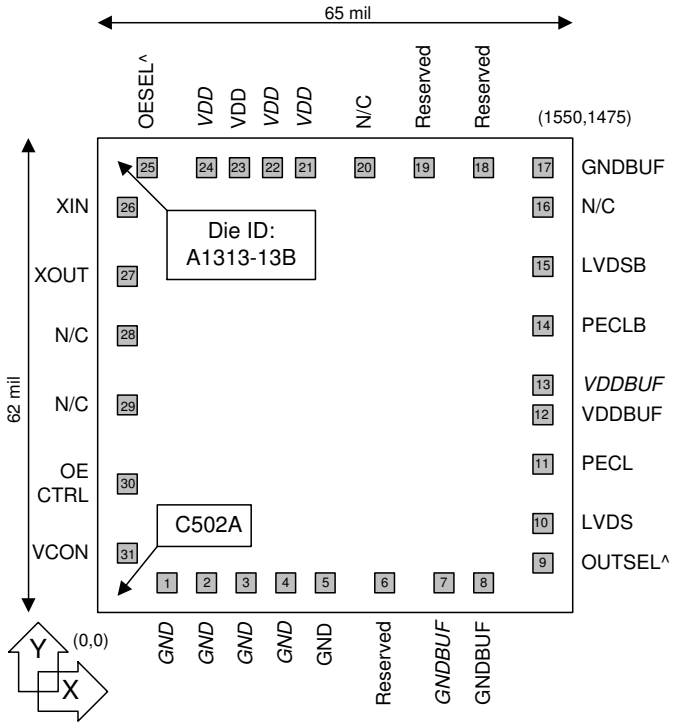
DESCRIPTION

The PLL520-30 is a VCXO IC specifically designed to pull frequency fundamental crystals from 65MHz to 130MHz, with selectable PECL or LVDS outputs and OE logic (enable high or enable low). Its design was optimized to tolerate higher limits of interelectrodes capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. Its internal varicaps allow an on chip frequency pulling, controlled by the VCON input.

BLOCK DIAGRAM



DIE CONFIGURATION



DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

OUTPUT SELECTION AND ENABLE

OUTSEL (Pad #9)	Selected Output
0	LVDS
1	PECL (default)

OESEL (Pad #25)	OE_CTRL (Pad #30)	State
0	0	Tri-state
	1	Output enabled (default)
1 (default)	0	Output enabled (default)
	1	Tri-state

Pad #9, #25: Bond to GND to set to "0". Internal pull up.

Pad #30: Logical states defined by PECL levels if OESEL is "1"
Logical states defined by CMOS levels if OESEL is "0"

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ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Built-in Capacitance	CX+	65MHz to 130MHz (at V_{DD})			2	pF
	CX-				2	
Inter-electrode capacitance	C_0			2.6		
C0/C1 ratio (gamma)	γ				300	-
Oscillation Frequency	OF	Fund., 3.3V Supplies Fund., 2.5V Supplies	65 65		130 105	MHz

3. Voltage Control Crystal Oscillator (3.3V)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range *		XTAL C_0/C_1 < 250 0V ≤ VCON ≤ V_{DD}		200		ppm
VCXO pullability *		VCON=1.65V, ±1.65V	±100			ppm
On-chip Varicaps control range *		VCON = 0 to V_{DD} 3.3V Supplies 2.5V Supplies		 4 – 18 7 – 18		pF
Linearity *					10	%
VCXO Tuning Characteristic				65		ppm/V
VCON input impedance				60		kΩ
VCON modulation BW		0V ≤ VCON ≤ V_{DD}, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

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4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}	PECL/LVDS			70/40	mA
Operating Voltage	V_{DD}	3.3V Supplies 2.5V Supplies	2.97 2.375		3.63 2.625	V
Output Clock Duty Cycle		@ 1.25V (LVDS), 3.3V Supply @ V_{DD} – 1.3V (PECL), 3.3V Supply	45 45	50 50	55 55	%
		@ 1.25V (LVDS), 2.5V Supply @ V_{DD} – 1.3V (PECL), 2.5V Supply	43 43	50 50	57 57	%
Short Circuit Current				±50		mA

5. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	77.76MHz		2.5		ps
Period jitter peak-to-peak	77.76MHz		18.5		ps
Integrated jitter RMS	Integrated 12 kHz to 20 MHz at 77.76MHz		0.5		ps

6. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	77.76MHz	-75	-95	-125	-145	-155	dBc/Hz

Note: Phase Noise at VCON = 0V

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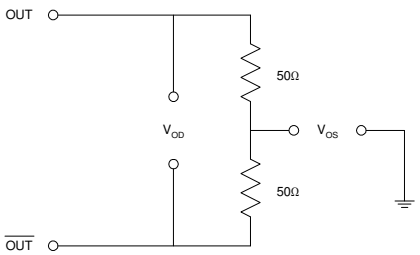
7. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

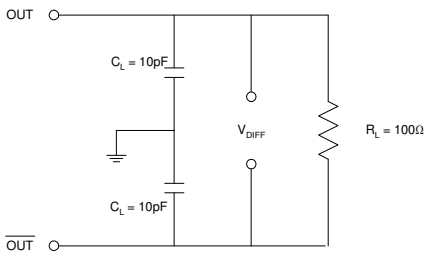
8. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

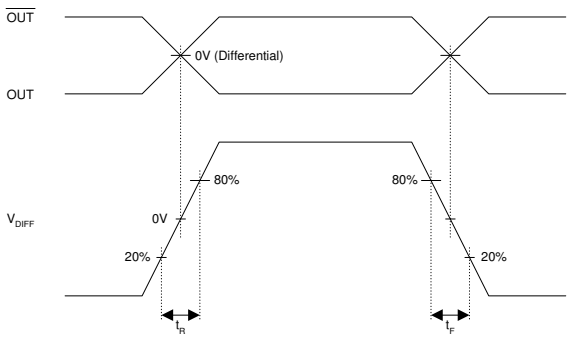
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



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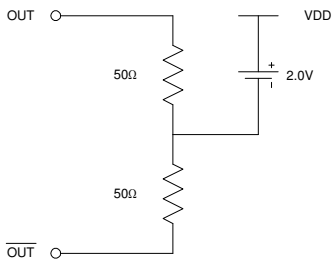
9. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025	V_{DD} – 0.750	V
Output Low Voltage	V_{OL}		V_{DD} – 1.900	V_{DD} – 1.620	V

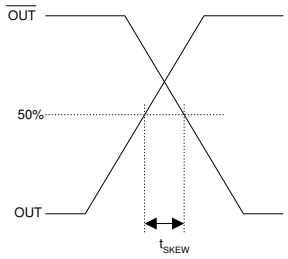
10. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

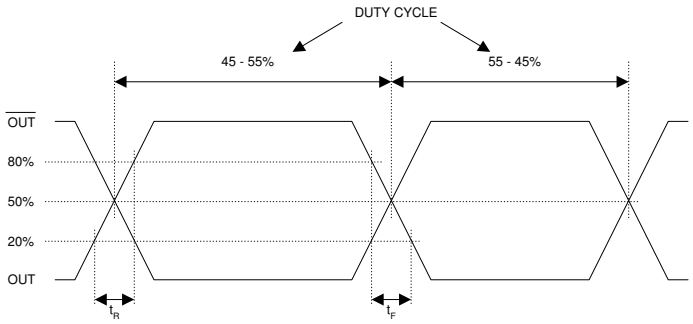
PECL Levels Test Circuit



PECL Output Skew



PECL Transistion Time Waveform



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PAD ASSIGNMENT

Pad #	Name	X (µm)	Y (µm)	Description
1	Optional GND	248	109	Optional Ground.
2	Optional GND	361	109	Optional Ground.
3	Optional GND	473	109	Optional Ground.
4	Optional GND	587	109	Optional Ground.
5	GND	702	109	Ground.
6	Reserved	874	109	Reserved for future use.
7	Optional GNDBUF	1042	109	Optional Ground, buffer circuitry.
8	GNDBUF	1171	109	Ground, buffer circuitry.
9	OUTSEL	1400	125	Output type selector. Internal pull up. See Output Selection and Enable table on page 1. Internal pull up.
10	LVDS	1400	259	LVDS output.
11	PECL	1400	476	PECL output.
12	VDDBUF	1400	616	3.3V power supply, buffer circuitry.
13	Optional VDDBUF	1400	716	Optional 3.3V power supply, buffer circuitry.
14	PECLB	1400	871	Complementary PECL output.
15	LVDSB	1400	1089	Complementary LVDS output.
16	Not connected	1400	1227	Not Connected.
17	GNDBUF	1389	1365	Ground, buffer circuitry.
18	Reserved	1232	1365	Reserved for future use.
19	Reserved	1042	1365	Reserved for future use.
20	Not connected	854	1365	Not Connected.
21	Optional VDD	659	1365	Optional 3.3V power supply.
22	Optional VDD	559	1365	Optional 3.3V power supply.
23	VDD	459	1365	3.3V power supply.
24	Optional VDD	358	1365	Optional 3.3V power supply.
25	OESEL	194	1365	Used to choose between PECL and CMOS OE logic levels. See Output Selection and Enable table on page 1. Internal pull up
26	XIN	109	1223	Crystal input. See Crystal Specifications on page 2.
27	XOUT	109	1017	Crystal output. See Crystal Specifications on page 2.
28	Not connected	109	858	Not Connected.
29	Not connected	109	646	Not Connected.
30	OE_CTRL	109	397	Used to enable/disable the output(s). See Output Selection and Enable table on page 1.
31	VCON	109	181	Voltage control input.

Note: for optimal Phase Noise performance, it is recommended to bond all optional VDD and GND pads.

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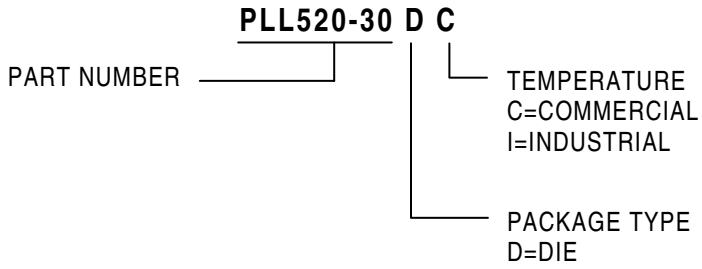
ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PLL520-30DC	P520-30DC	Die – Waffle Pack

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