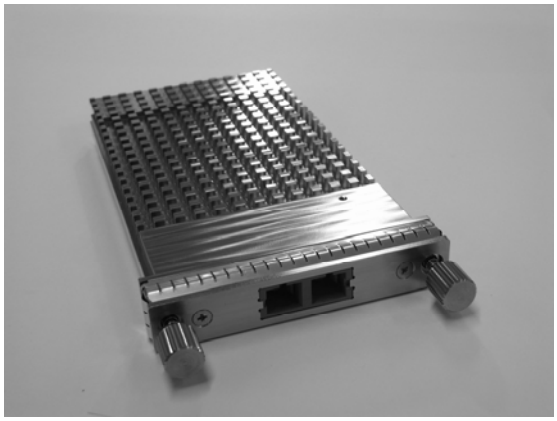
40Gb/s CFP Optical Transceiver Module

SCF0400L4 Series

(40GBASE-LR4, ITU-T OTU-3,1310nm 4-lane CWDM, DFB-LD, PIN-PD)

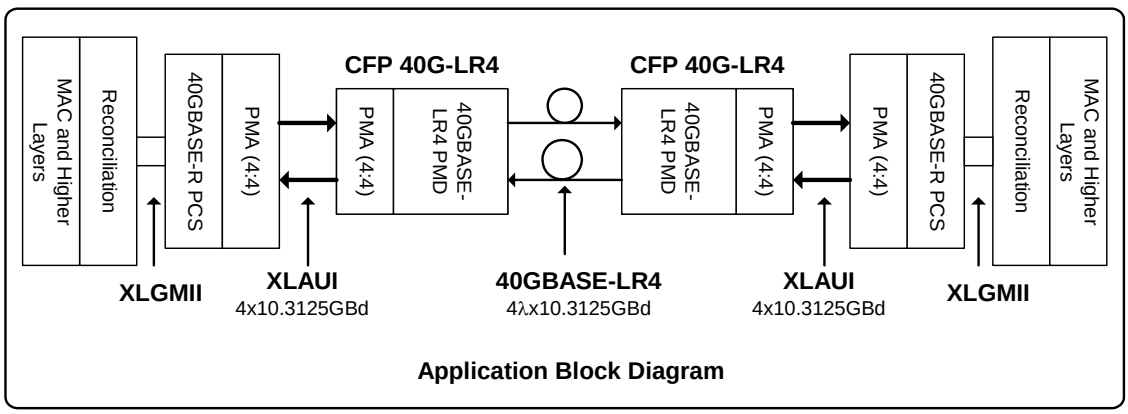
Features

- 4-lane x 10Gb/s CWDM Optical Interface
  - High quality and reliability optical sub-assemblies
  - 1310nm Un-cooled CWDM DFB-DML Transmitter with optical MUX
  - High Sensitivity PIN-TIA with optical DEMUX
  - 1271, 1291, 1311, 1331nm CWDM grid in ITU-T G.694.2 up to 10km over a SMF
- IEEE802.3ba Compliant
  - IEEE802.3 Clause 87 40GBASE-LR4
  - XLAUI(4x10G) Electrical Interface
  - MDIO Interface for module management
- OTU-3 Rate Operation
  - 9.953 and up to 4x11.146 Gb/s lane operation
  - ITU-T C4S1-2D1 Option Available
- CFP MSA Compliant
  - Easy supply management for hot pluggability
  - CFP MSA Form Factor
  - 148pin Electrical Connector
  - Duplex SC or LC Receptacle
- Low Power Consumption
  - 3.3V single power supply
  - Power consumption less than 8W (Class 1)



Applications

- 40GE Enterprise switches and routers
- Carrier Grade 40GE Core-routers
- CWDM Point to Point and Ring Application
- Inter Rack Connection
- Other high speed data connections



Application Block Diagram

1. General Description

The SCF0400L4 is the CFP optical transceiver module which is a hot pluggable form factor designed for high speed optical networking application. The SCF0400L4 is designed for 40Gigabit Ethernet application and provides 40GBASE-LR4 compliant optical interface, XLAUI electrical interface and MDIO module management interface. The SCF0400L4 converts 4-lane 10Gb/s electrical data streams to 4-lane CWDM10Gb/s optical output signal and 4-lane CWDM 10Gb/s optical input signal to 4-lane 10Gb/s electrical data streams. This 4-lane 10Gb/s electrical signal is fully compliant with 802.3ba XLAUI specification and allows FR4 host PCB trace up to 25cm.

The high performance uncooled CWDM DFB-LD transmitter and high sensitivity PIN receiver provide superior performance for 40Gigabit Ethernet applications up to 10km links and compliant optical interface with IEEE802.3ba Clause 40GBASE-LR4 requirements..

2. Functional Description

The SCF0400L4 CFP transceiver is a bi-directional module with a transmitter and receiver in one package. The SCF0400L4 contains a duplex SC or LC connector for the optical interface and a 148-pin connector for the electrical interface. Figure 2.1 shows the functional block diagram of SCF0400L4 CFP transceiver. SCF0400L4 contains 4-lane optical transmitter, 4-lane optical receiver and module management block including MDIO interface.

Transmitter Operation

The transceiver module receives 4-lane 10Gb/s XLAUI electrical inputs. CDR reshapes and retimes received electrical signal to compensate the degraded electrical signal which comes through host board and host connectors. The transmitter converts 4-lane XLAUI signals to an optical signal through 4 Laser drivers and Lasers diodes which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each Laser launches optical signal in specific wavelength specified in IEEE802.3ba 40GBASE-LR4 requirements. These 4-lane optical signals will be multiplexed into one fiber by 4 to1 WDM Optical MUX. The optical output power is held constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or through MDIO module management Interface.

Receiver Operation

The SCF0400L4 receives 4-lane CWDM optical signal. The optical signal will be de-multiplexed by 1 to 4 WDM optical DEMUX and fed into each Receiver Optical Sub-Assembly. Each ROSA converts optical signal to electrical signal. The regenerated electrical signals are retimed and de-jittered by CDRs. CDRs generate 4-lane 10Gb/s

electrical output signal which is compliant with XLAUI interface requirements. Each received optical signal is monitored by the DOM section. The monitored value is reported through the MDIO section. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be launched.

Management Data I/O (MDIO)

The SCF0400L4 supports the MDIO interface specified in IEEE802.3 Clause 45. This 2-wire management data I/O interface is provided for the module status monitoring and control. The management data clock (MDC) provides clocking for the data that is passed on the MDIO port. Five further pins allow for loading of a port address (PORT_ADDR0-4) into the module.

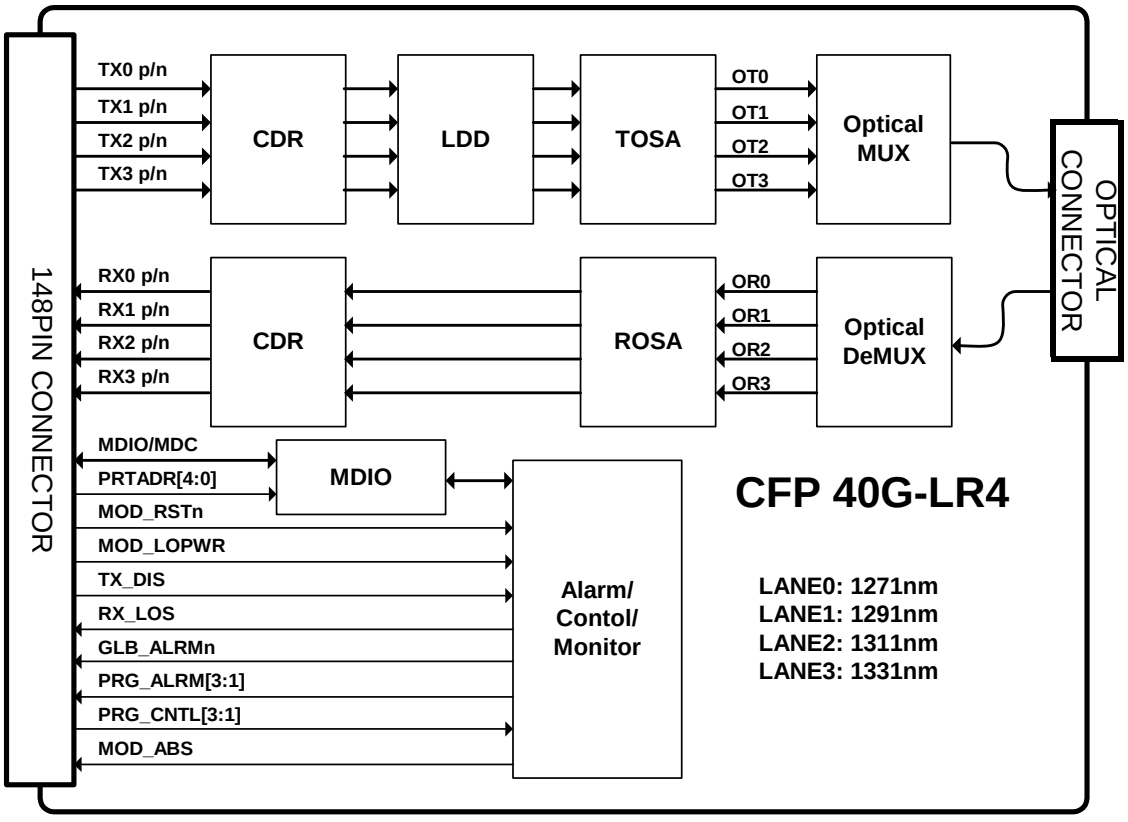
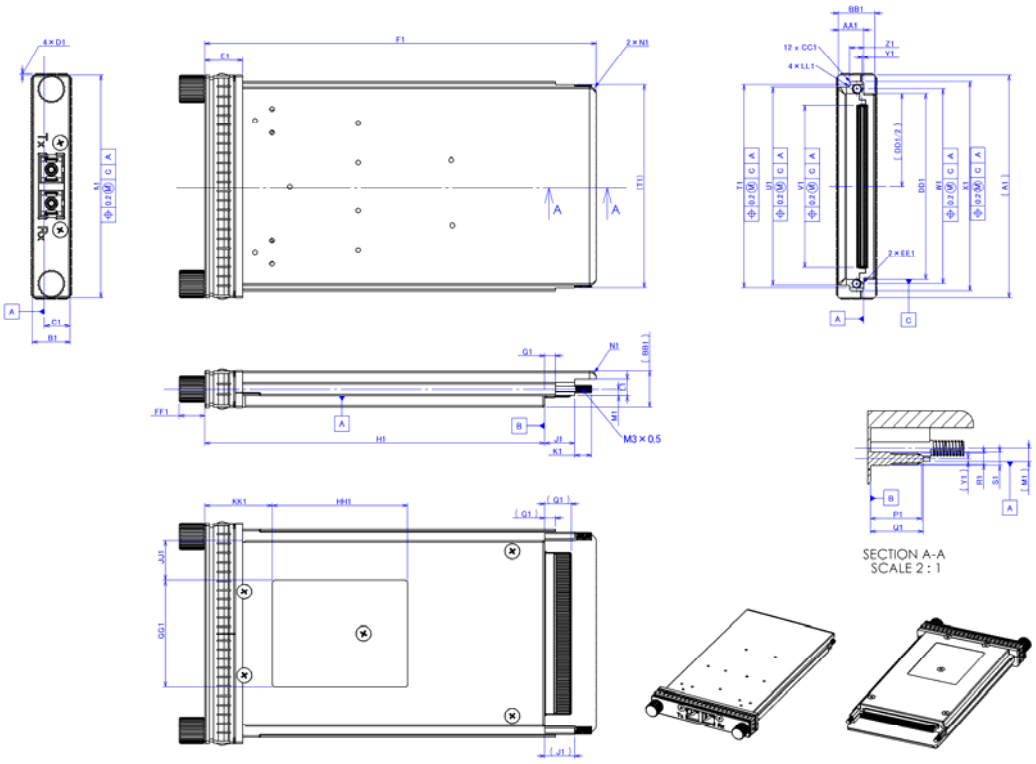


Figure 2.1. Functional Block Diagram

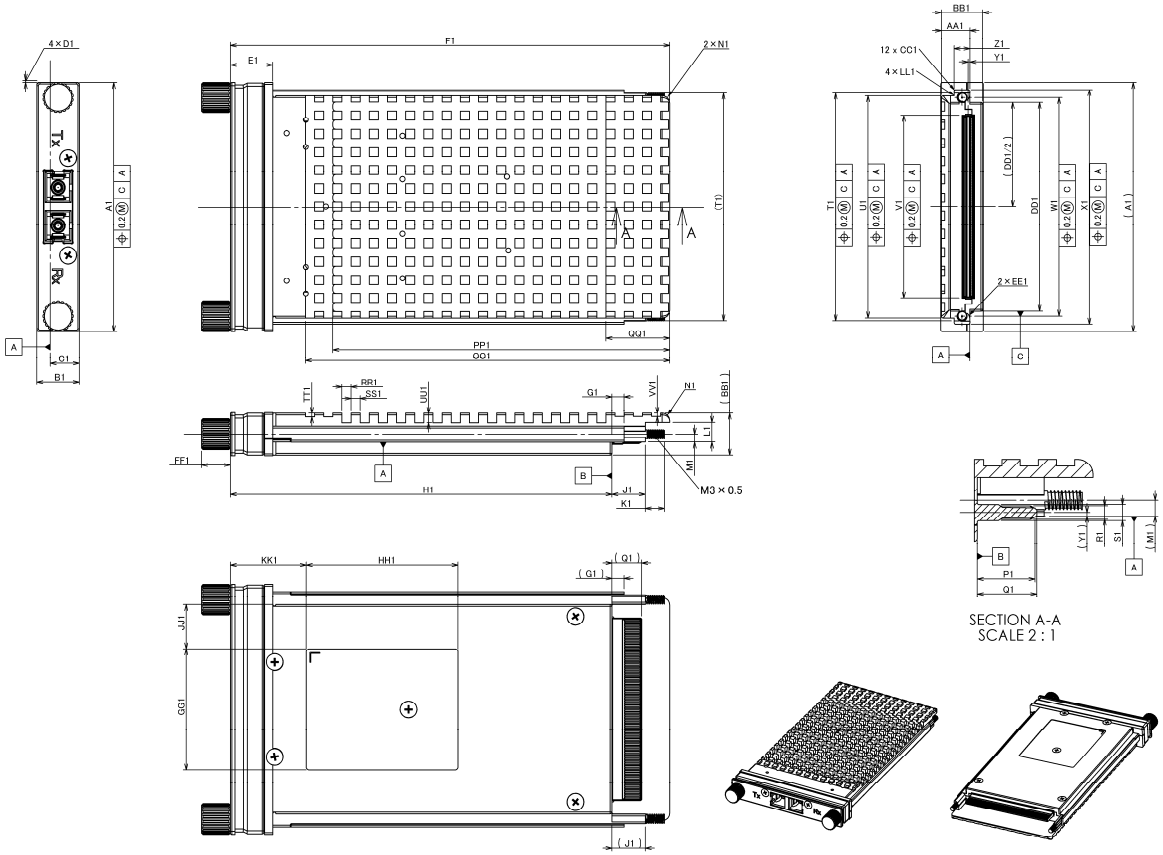
3. Package Dimensions

Figure 3.1 shows the package dimensions of SCF0400L4. The SCF0400L4 transceiver is designed to be complaint with CFP MSA specification.



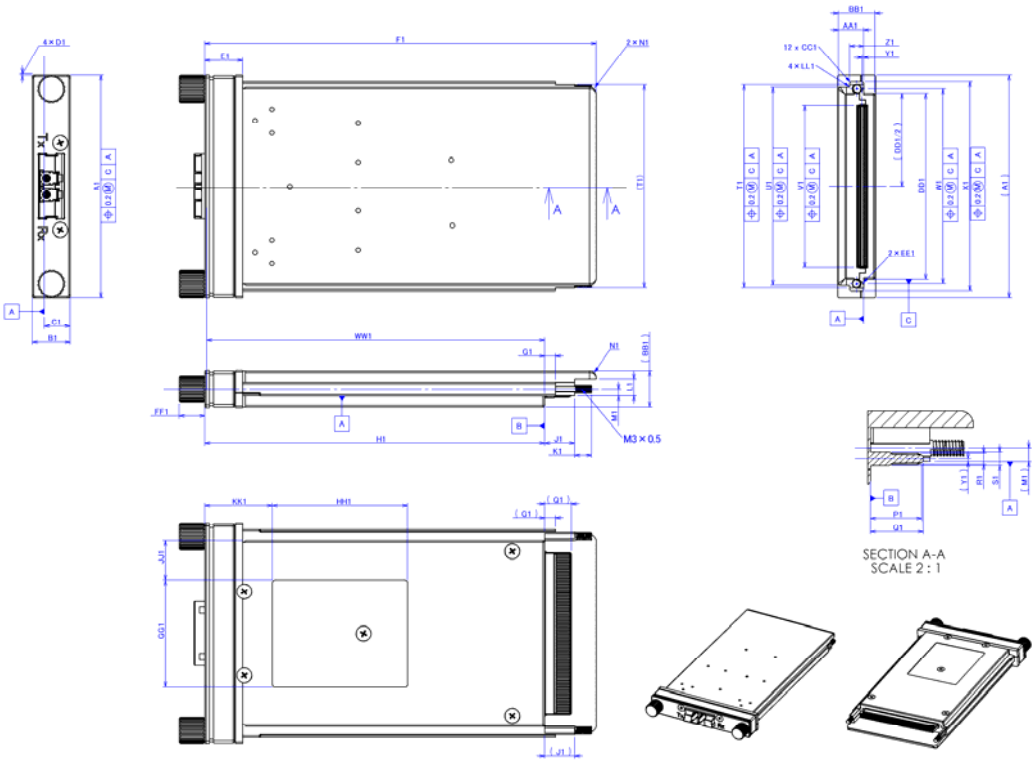
Dimensions in mm

Figure 3.1. (a) SC with Flat Top Package Drawing



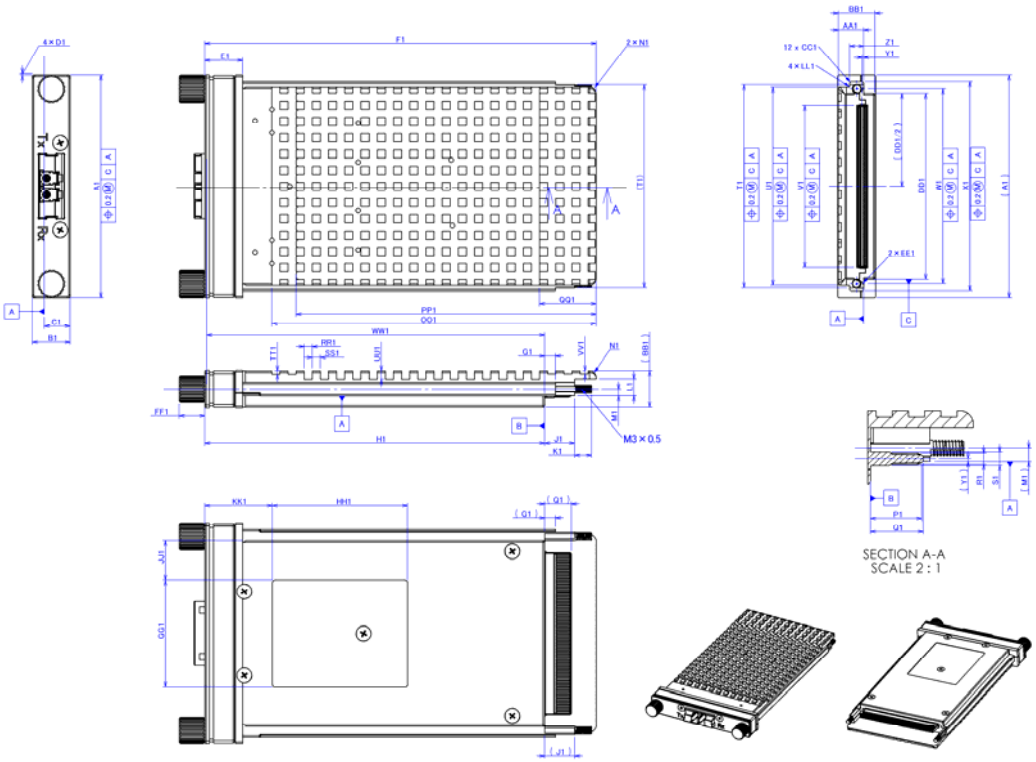
Dimensions in mm

Figure 3.1. (b) SC with Integral Heat Sink Package Drawing



Dimensions in mm

Figure 3.1. (c) LC with Flat Top Package Drawing



Dimensions in mm

Figure 3.1. (d) LC with Integral Heat Sink Package Drawing

Table 3.1. Package dimensions

MODULE DIMENSIONS				Note
KEY	VALUE	TOLERANCE	DESCRIPTION	
A1	82.00	±0.10	WIDTH OF MODULE FACEPLATE, OVERALL	
B1	14.00	±0.10	HEIGHT OF MODULE FACEPLATE, OVERALL	
C1	9.60	±0.20	HEIGHT OF MODULE FACEPLATE TO DATUM -A-	
D1	0.65	MIN.	HEIGHT OF EMI SPRING FINGERS	
E1	14.00	±0.50	LENGTH OF MODULE FACEPLATE, OVERALL	
F1	144.75	±0.20	LENGTH OF MODULE, OVERALL	
G1	4.00	±0.20	LENGTH OF MODULE RAIL SHOULDER	
H1	125.70	±0.20	DISTANCE FROM MODULE FACEPLATE TO HARDSTOP DATUM -B-	
J1	11.00	±0.20	DISTANCE FROM CONNECTOR PROTECTOR TO HARDSTOP DATUM -B-	
K1	6.00	±0.50	M3 THUMBSCREW THREAD LENGTH IN FULLY LOADED POSITION	
L1	6.40	±0.20	DISTANCE FROM DATUM -A- TO BOTTOM SURFACE OF MODULE TAIL	
M1	2.60	±0.20	DISTANCE FROM DATUM -A- TO CENTERLINE OF M3 THUMBSCREW HOLE	
N1	R2.00	MIN.	TOP MODULE LEAD-IN RADIUS	
P1	9.08	±0.15	LENGTH OF CONNECTOR CONTACT PIN FROM DATUM -B-	
Q1	9.80	±0.08	LENGTH OF CONNECTOR END FROM DATUM -B-	
R1	2.18	±0.08	CONNECTOR TIP THICKNESS, OVERALL	
S1	2.62	±0.08	CONNECTOR SHOULDER THICKNESS, OVERALL	
T1	75.00	±0.20	WIDTH OF MODULE CONNECTOR PROTECTOR, OVERALL	
U1	73.20	±0.20	WIDTH, TOP SHOULDER, MODULE, OVERALL	
V1	60.05	±0.08	WIDTH, CONNECTOR, OVERALL	
W1	72.00	±0.20	CENTERLINE TO CENTERLINE DISTANCE OF M3 THUMB SCREW HOLES	
X1	77.20	±0.20	WIDTH, MODULE BODY, OVERALL	
Y1	0.60	±0.15	DATUM -A- TO CENTERLINE OF CONNECTOR	
Z1	5.20	±0.20	HEIGHT, RAIL SHOULDER, MODULE, OVERALL	
AA1	9.40	±0.20	DATUM -A- TO TOP OF MODULE	
BB1	13.60	±0.20	HEIGHT, MODULE BODY, OVERALL	
CC1	R0.6	±0.10	MODULE OUTSIDE CORNER RADIUS	
DD1	68.80	±0.20	WIDTH, MODULE BOTTOM, OVERALL	
EE1	R2.60	±0.20	RADIUS, CLEARANCE, MODULE, CONNECTOR PROTECTOR FEATURE	
FF1	9.50	±0.50	THUMBSCREW HEIGHT FROM MODULE FACEPLATE TOP FRONT SURFACE	
GG1	40.00	±0.20	LABEL RECESS WIDTH	
HH1	50.00	±0.20	LABEL RECESS LENGTH	
JJ1	14.40	±0.20	LABEL RECESS TO SIDE OF MODULE	
KK1	25.00	±0.20	LABEL RECESS TO MODULE FACEPLATE	
LL1	R0.4	MAX.	MODULE INSIDE CORNER RADIUS	
OO1	120.00	±0.50	LENGTH OF HEATSINK	1
PP1	111.00	±0.50	LENGTH OF HEATSINK	1
QQ1	21.00	±0.50	LENGTH OF HEATSINK	1
RR1	3.00	±0.20	BI-DIRECTIONAL HEATSINK FIN DIMENSIONS (EACH DIRECTION)	1
SS1	3.00	±0.20	BI-DIRECTIONAL HEATSINK FIN DIMENSIONS (EACH DIRECTION)	1
TT1	1.20	±0.20	HEIGHT OF FIN	1
UU1	3.20	±0.20	HEIGHT OF FIN	1
VV1	1.20	±0.20	HEIGHT OF FIN	1
WW1	125.00	±0.50	CFP module stopper to LC connector Latch	2

Note1: Apply to Integral Heat Sink Option, Note2: Apply to LC Duplex Option

4. Pin Assignment and Pin Description

4.1. CFP Transceiver Electrical Pin Assignment

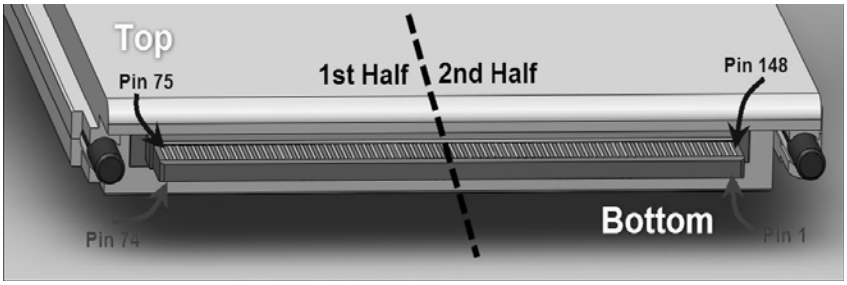


Figure 4.1. CFP Transceiver Electrical Pin Numbering

Table 4.1. CFP Transceiver Electrical Pin Assignment

Top Raw 2nd Half		Bottom Row 2nd Half		Top Raw 1st Half		Bottom Row 1st Half	
PIN#	Name	PIN#	Name	PIN#	Name	PIN#	Name
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	NC (note1)	2	3.3V_GND	110	NC	39	MOD_RSTn
146	NC (note1)	3	3.3V_GND	109	NC	40	RX_LOS
145	GND	4	3.3V_GND	108	GND	41	GLB_ALRMn
144	NC (note2)	5	3.3V_GND	107	NC	42	PRTADR4
143	NC (note2)	6	3.3V	106	NC	43	PRTADR3
142	GND	7	3.3V	105	GND	44	PRTADR2
141	NC (note2)	8	3.3V	104	NC	45	PRTADR1
140	NC (note2)	9	3.3V	103	NC	46	PRTADR0
139	GND	10	3.3V	102	GND	47	MDIO
138	NC (note2)	11	3.3V	101	NC	48	MDC
137	NC (note2)	12	3.3V	100	NC	49	GND
136	GND	13	3.3V	99	GND	50	NUC (note3)
135	NC (note2)	14	3.3V	98	NC	51	NUC (note3)
134	NC (note2)	15	3.3V	97	NC	52	GND
133	GND	16	3.3V_GND	96	GND	53	NUC (note3)
132	NC (note2)	17	3.3V_GND	95	NC	54	NUC (note3)
131	NC (note2)	18	3.3V_GND	94	NC	55	3.3V_GND
130	GND	19	3.3V_GND	93	GND	56	3.3V_GND
129	NC (note2)	20	3.3V_GND	92	NC	57	3.3V_GND
128	NC (note2)	21	NUC (note3)	91	NC	58	3.3V_GND
127	GND	22	NUC (note3)	90	GND	59	3.3V_GND
126	NC (note2)	23	GND	89	RX3n	60	3.3V
125	NC (note2)	24	NC	88	RX3p	61	3.3V
124	GND	25	NC	87	GND	62	3.3V
123	TX3n	26	GND	86	RX2n	63	3.3V
122	TX3p	27	NUC (note3)	85	RX2p	64	3.3V
121	GND	28	NUC (note3)	84	GND	65	3.3V
120	TX2n	29	NUC (note3)	83	RX1n	66	3.3V
119	TX2p	30	PRG_CNTL1	82	RX1p	67	3.3V
118	GND	31	PRG_CNTL2	81	GND	68	3.3V
117	TX1n	32	PRG_CNTL3	80	RX0n	69	3.3V
116	TX1p	33	PRG_ALRM1	79	RX0p	70	3.3V_GND
115	GND	34	PRG_ALRM2	78	GND	71	3.3V_GND
114	TX0n	35	PRG_ALRM3	77	NC	72	3.3V_GND
113	TX0p	36	TX_DIS	76	NC	73	3.3V_GND
112	GND	37	MOD_LOPWR	75	GND	74	3.3V_GND

note1) These pins are not used for this product. These pins are internally terminated by AC 100ohm.

note2) These pins are not used for this product. The paired pins are internally terminated by AC 100ohm

note3) These pins are internally used and DO NOT allow to connect any signal, power supply and GND.

4.2. Host PCB CFP Foot Print

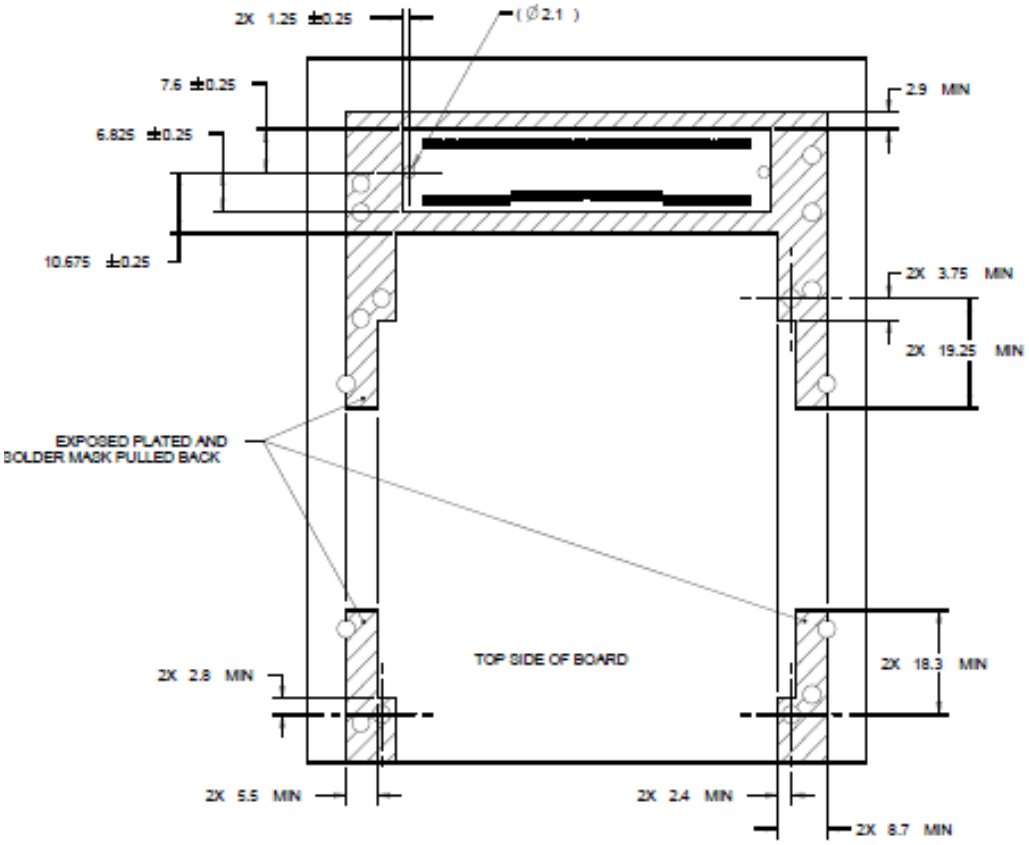


Figure 4.2. Host PCB CFP Foot Print

Table 4.2. Host Connector Assembly Information

Part Name	Supplier	Part Number
External Blacket Assy.	Tyco Electronics	2057626-1
Guide Rail	Tyco Electronics	2057592-2
Host Connector Cover Assy.	Tyco Electronics	2057631-1
Backer Plate Assy.	Tyco Electronics	2057930-1
Host Connector	Tyco Electronics	2057630-1

4.3. Pin Descriptions

Table 4.3. Pin Description

PIN#	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2	3.3V_GND			
3	3.3V_GND			
4	3.3V_GND			
5	3.3V_GND			
6	3.3V			3.3V Module Supply Voltage
7	3.3V			3.3V Module Supply Voltage
8	3.3V			3.3V Module Supply Voltage
9	3.3V			3.3V Module Supply Voltage
10	3.3V			3.3V Module Supply Voltage
11	3.3V			3.3V Module Supply Voltage
12	3.3V			3.3V Module Supply Voltage
13	3.3V			3.3V Module Supply Voltage
14	3.3V			3.3V Module Supply Voltage
15	3.3V			3.3V Module Supply Voltage
16	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
17	3.3V_GND			
18	3.3V_GND			
19	3.3V_GND			
20	3.3V_GND			
21	NUC			Module Vendor I/O. Must No Connect at host board
22	NUC			Module Vendor I/O. Must No Connect at host board
23	GND			
24	NC			Not Connected Internally
25	NC			Not Connected Internally
26	GND			
27	NUC			Module Vendor I/O. Must No Connect at host board
28	NUC			Module Vendor I/O. Must No Connect at host board
29	NUC			Module Vendor I/O. Must No Connect at host board
30	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
31	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤8W, "01":≤16W, "10": ≤24W, "11" or NC: >24W = not used
32	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤8W, "01":≤16W, "10": ≤24W, "11" or NC: >24W = not used
33	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
34	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
35	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
36	TX_DIS	I	LVCMOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled

Table 4.3. Pin Description (Continued)

PIN#	Name	I/O	Logic	Description
38	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
39	MOD_RSTn	I	LVCMOS w/ PUR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
40	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
41	GLB_ALRMn	O	LVCMOS	Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
42	PRTADR4	I	1.2V CMOS	MDIO Physical Port address bit 4
43	PRTADR3	I	1.2V CMOS	MDIO Physical Port address bit 3
44	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
45	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
46	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
49	GND			
50	NUC			Module Vendor I/O. Must No Connect at host board
51	NUC			Module Vendor I/O. Must No Connect at host board
52	GND			
53	NUC			Module Vendor I/O. Must No Connect at host board
54	NUC			Module Vendor I/O. Must No Connect at host board
55	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND			
57	3.3V_GND			
58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Voltage
61	3.3V			3.3V Module Supply Voltage
62	3.3V			3.3V Module Supply Voltage
63	3.3V			3.3V Module Supply Voltage
64	3.3V			3.3V Module Supply Voltage
65	3.3V			3.3V Module Supply Voltage
66	3.3V			3.3V Module Supply Voltage
67	3.3V			3.3V Module Supply Voltage
68	3.3V			3.3V Module Supply Voltage
69	3.3V			3.3V Module Supply Voltage
70	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
71	3.3V_GND			
72	3.3V_GND			
73	3.3V_GND			
74	3.3V_GND			

Table 4.3. Pin Description (Continued)

PIN#	Name	I/O	Logic	Description
75	GND			
76	NC			Not Connected Internally
77	NC			Not Connected Internally
78	GND			
79	RX0p	O	HS I/O	Lane 0 Receiver Output (Positive)
80	RX0n	O	HS I/O	Lane 0 Receiver Output (Negative)
81	GND			
82	RX1p	O	HS I/O	Lane 1 Receiver Output (Positive)
83	RX1n	O	HS I/O	Lane 1 Receiver Output (Negative)
84	GND			
85	RX2p	O	HS I/O	Lane 2 Receiver Output (Positive)
86	RX2n	O	HS I/O	Lane 2 Receiver Output (Negative)
87	GND			
88	RX3p	O	HS I/O	Lane 3 Receiver Output (Positive)
89	RX3n	O	HS I/O	Lane 3 Receiver Output (Negative)
90	GND			
91	NC			Not Connected Internally
92	NC			Not Connected Internally
93	GND			
94	NC			Not Connected Internally
95	NC			Not Connected Internally
96	GND			
97	NC			Not Connected Internally
98	NC			Not Connected Internally
99	GND			
100	NC			Not Connected Internally
101	NC			Not Connected Internally
102	GND			
103	NC			Not Connected Internally
104	NC			Not Connected Internally
105	GND			
106	NC			Not Connected Internally
107	NC			Not Connected Internally
108	GND			
109	NC			Not Connected Internally
110	NC			Not Connected Internally
111	GND			

Table 4.3. Pin Description (Continued)

PIN#	Name	I/O	Logic	Description
112	GND			
113	TX0p	I	HS I/O	Lane 0 Transmitter Input (Positive)
114	TX0n	I	HS I/O	Lane 0 Transmitter Input (Negative)
115	GND			
116	TX1p	I	HS I/O	Lane 1 Transmitter Input (Positive)
117	TX1n	I	HS I/O	Lane 1 Transmitter Input (Negative)
118	GND			
119	TX2p	I	HS I/O	Lane 2 Transmitter Input (Positive)
120	TX2n	I	HS I/O	Lane 2 Transmitter Input (Negative)
121	GND			
122	TX3p	I	HS I/O	Lane 3 Transmitter Input (Positive)
123	TX3n	I	HS I/O	Lane 3 Transmitter Input (Negative)
124	GND			
125	NC			Internally terminated with AC 100 Ohm
126	NC			
127	GND			
128	NC			Internally terminated with AC 100 Ohm
129	NC			
130	GND			
131	NC			Internally terminated with AC 100 Ohm
132	NC			
133	GND			
134	NC			Internally terminated with AC 100 Ohm
135	NC			
136	GND			
137	NC			Internally terminated with AC 100 Ohm
138	NC			
139	GND			
140	NC			Internally terminated with AC 100 Ohm
141	NC			
142	GND			
143	NC			Internally terminated with AC 100 Ohm
144	NC			
145	GND			
146	NC			Internally terminated with AC 100 Ohm
147	NC			
148	GND			

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5. Absolute Maximum Ratings and Recommended Operating Conditions

Table 5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Strage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH		85	%	
Operating Case Temperature	Topc	0	70	degC	
Supply Voltage	3.3V	-0.3	3.6	V	
Voltag on any XLAUI pin	V_{XAUI}	-0.3	1.9	V	
Voltage on any 3.3V LVCMOS pin	V_{LVCMOS}	-0.3	Vcc+0.3	V	
Voltage on any 1.8V LVCMOS pin	V_{LVCMOS}	-0.7	1.65	V	
Receiver Input Optical Power each lane	Mip		3.3	dBm	

Table 5.2. Recommended Operating Conditions and supply requirements

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	0	70	degC	
Relative Humidity (non-condensing)	Rhop		85	%	
Power Supply Voltage	3.3V	3.135	3.465	V	
Power Supply Current for 3.3V			2.5	A	
Total Power Dissipation	Pw	-	8	W	
Low Power Mode dissipation	Plow	-	2	W	

6. Electrical Interface

6.1 Electrical High Speed I/O Interface

Table 6.1.1. XLAUI Input Interface

XLAUI Receiver Parameters	symbol	Min	Typ	Max	Units	Note
Signal Rate Per Lane			10.3125		Gb/s	
Signal Rate tolerance		-100		100	ppm	
AC Common Mode Voltage Tolerance, RMS	CMVLTac			20	mV	
Minimum Differential Input Return Loss	Rldiff	IEEE802.3ba Equation 83B-5			dB	
Total Input Jitter Tolerance	Tjin			0.62	UI	
Deterministic Input Jitter Tolerance	Tdin			0.42	UI	
Transmitter Input Eye Mask (X1, X2)		(0.31, 0.5)			UI	1
Transmitter Input Eye Mask (Y1, Y2)		(42.5, 425)			mV	1

Table 6.1.2 XLAUI Output Interface

XLAUI Driver Parameters	symbol	Min	Typ	Max	Units	Note
Signal Rate Per Lane			10.3125		Gb/s	
Signal Rate tolerance		-100		100	ppm	
Single-end Output Voltage	Vosingle	-0.4		4	V	
Output AC Common Mode Voltage, RMS	Vocomac			15	mV	
Output Rise and Fall Time (20%-80%)	Trftl	24			ps	
Minimum Differential Output Return Loss	Rldiff	IEEE802.3ba Equation 83B-6			dB	
Total Output Jitter	Tjo			0.4	UI	
Deterministic Output Jitter	Tdo			0.25	UI	
Receiver Output Eye Mask (X1, X2)		(0.2, 0.5)			UI	2
Receiver Output Eye Mask (Y1, Y2)		(136, 380)			mV	2

Note1: Refer to Figure 6.1.1

Note2: Refer to Fig.6.1.2

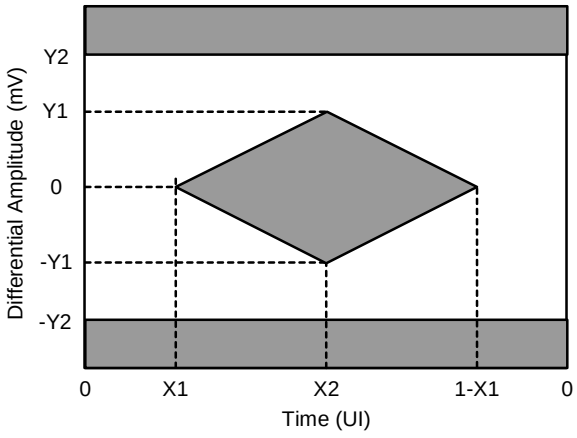


Figure 6.1.1. CAUI Receiver Eye Mask

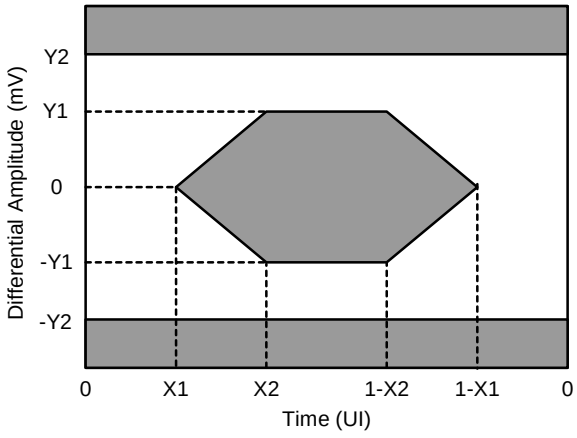


Figure 6.1.2. CAUI Transmitter Eye Mask

6.2 Electrical Low Speed I/O Interface

Table 6.2.1. 3.3V CMOS DC parameters

(MOD_RSTn, MOD_LOPWR, TX_DIS, PRG_CNTL, MOD_ABS, RX_LOS, GLB_ALRMn, PRG_ALRM)

Parameter	symbol	Min	Typ	Max	Units	Note
Output High Voltage (IOH=-100uA)	Voh	Vcc-0.2		Vcc+0.3	V	
Output Low Voltage (IOL=100uA)	Vol	-0.3		0.2	V	
Intput High Voltage	Vih	2		Vcc+0.3	V	
Input Low Voltage	Vil	-0.3		0.8	V	
Input Leakage Current	IIN	-10		10	μA	
Minimun Pulse Width of Control Pin Signal	t_CNTL	100			μS	

Table 6.2.2. 1.2V CMOS DC parameters (MDIO, MDC, PRTADR4:0)

Parameter	symbol	Min	Typ	Max	Units	Note
Intput High Voltage	Vih	0.84		1.5	V	
Input Low Voltage	Vil	-0.3		0.36	V	
Input Leakage Current	IIN	-100		100	μA	
Output High Voltage	Voh	1.0		1.5	V	
Output Low Voltage	Vol	-0.3		0.2	V	
Output high current (Vi =1.0V)	Iioh			-4	mA	
Output low current (Vi = 0.2V)	Iol	4			mA	
Input Capacitance	Ci			10	pF	

Table 6.2.3. MDIO and MDC AC parameters

Parameter	symbol	Min	Typ	Max	Units	Note
MDC clock Frequency	fMDC	0.1		4	MHz	
MDC clock period	tprd	250		10000	ns	
MDIO data hold time	Thold	10			ns	
MDIO data setup time	Tsetup	10			ns	
MDC high and low time	twidth	40		60	%	
		160			ns	
Delay from MDC rising edge to MDIO data change	Tdelay			175	ns	
MDIO/MDC termination in CFP	Zt	100			kOhm	

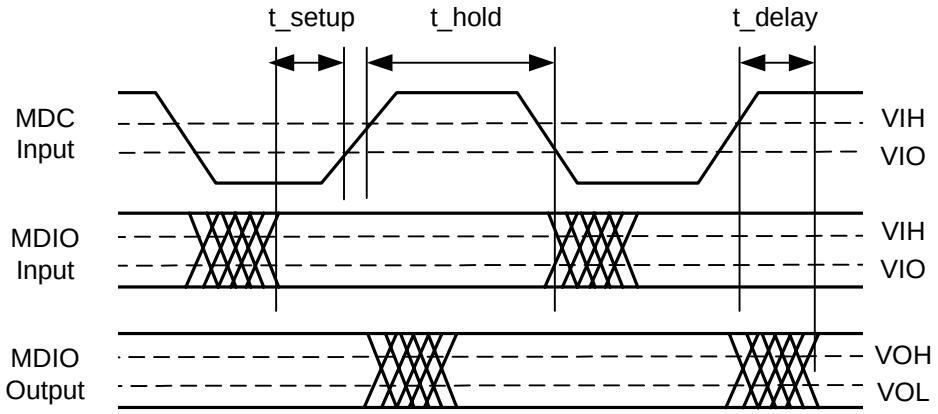


Table 6.2.1. MDIO and MDC AC parameters

7. Optical Interface

Table 7.1. Optical Interface

CFP 40G-LR4						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Note**
Fiber type			SMF			
Signaling speed, each lane		9.95328 ± 20ppm			Gbps	2, 3
Signaling speed, each lane		10.3125 ± 100ppm			Gbps	1,2,3
Signaling speed, each lane		10.75460 ± 20ppm			Gbps	2, 3
Signaling speed, each lane		11.14274 ± 20ppm			Gbps	2, 3
Signaling speed, each lane		11.14584 ± 20ppm			Gbps	2, 3
Operating Reach			2 – 10k		m	
Lane wavelength (range): L0	L0	1264.5	1271	1277.5	nm	
Lane wavelength (range): L1	L1	1284.5	1291	1297.5	nm	
Lane wavelength (range): L2	L2	1304.5	1311	1317.5	nm	
Lane wavelength (range): L3	L3	1324.5	1331	1337.5	nm	
Transmitter Optical Interface						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Note**
SMSR	SMSR	30		-	dB	
Total average launch power	Po2			8.3	dBm	
Average launch power, each lane 1	Poln	-7		2.3	dBm	1, 2, 4
Average launch power, each lane 2	Poln	-2.3		2.3	dBm	3
OMA, each lane1	OMA	-4		3.5	dBm	1, 2
OMA, each lane2	OMA	-2.5		3.5	dBm	3
DifferenceOMA between any two lanes	dOMA			6.5	dB	
OMA - TDP, each lane	OMAtdp	-4.8			dBm	
Transmitter and Dispersion Penalty (TDP), each lane	TDP			2.6	dB	
Average power Disabled, each lane	Podis			-30	dBm	
Extinction Ratio 1	ER2	3.5	5	-	dB	1, 2
Extinction Ratio 2	ER2	4.5	5.5	-	dB	3
Eye Mask {X1, X2, X3, Y1, Y2, Y3}	PM	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				5
RIN12OMA	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	Torlt			20	dB	
Transmitter Refrectance	Toref			-12	dB	
Receiver Optical Interface						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Note**
Damage threshold	Pindm	3.3			dBm	
Average receive power, each lane 1	Pinave	-13.7		2.3	dBm	1, 2, 4
Average receive power, each lane 2	Pinave	-10.5		2.3	dBm	3
Receive power, each lane (OMA)	PinOMA	-11.5		3.5	dBm	1, 2, 4
Difference in OMA between any two lanes	OMArD			7.5	dBm	
Stressed Sensitivity in OMA Vertical eye closure penalty 1.6dB Stressed eye jitter 0.3 UI	OMAst			-9.6	dBm	6
Rx-Lane LOS Assert	LOSas	-30	-23	-20	dBm	
Rx-Lane LOS Deassert	LOSdea		-21	-17	dBm	
Rx-Lane LOS Hysteresis	Sdhys	0.5			dB	
Receiver reflectance (max)	ORL			-26	dB	

Note1: Apply to SCF0400L4, Note2: Apply to SCF0410L4, Note3: Apply to SCF0420L4

Note4: Minimum value is informative, Note5: Refer to Fig.7.1., Note6: Only apply to 40GEBASE-LR4 operation.

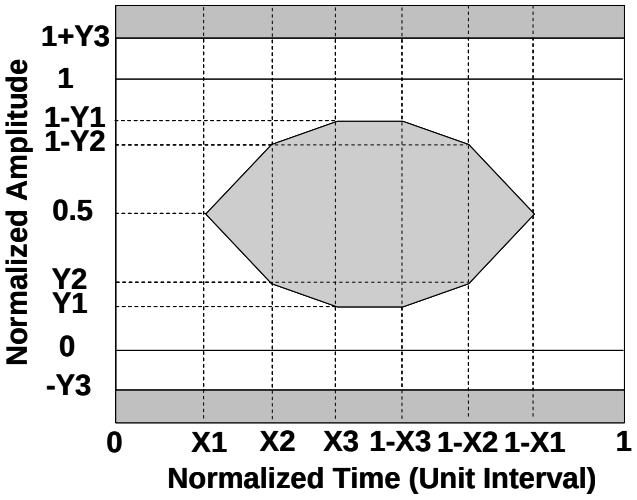
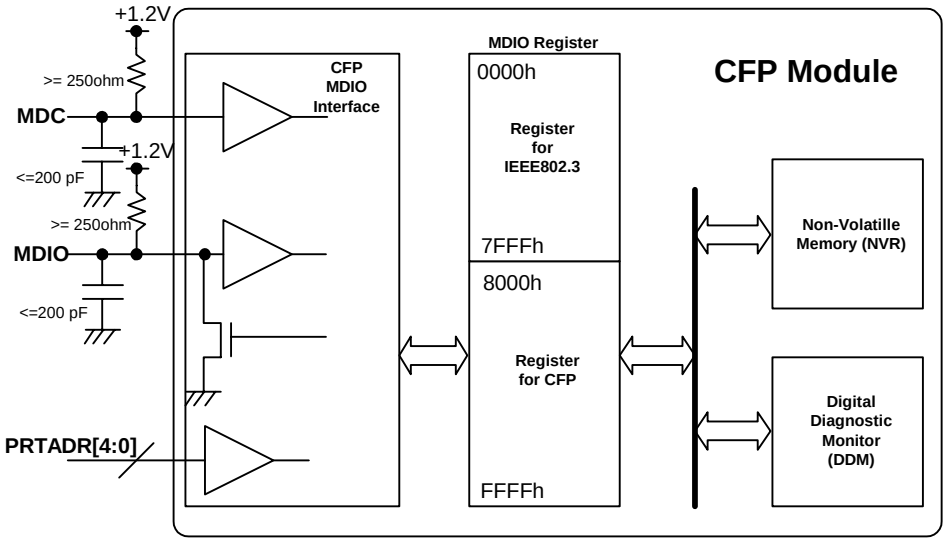


Fig 7.1. Transmission eye mask definition

8. MDIO and Non-Volatile Registers Map

8.1 MDIO Interface and CFP Register Allocation



Note: Capacitor represents stray capacity

> 600ohm pull-up is preferred

Figure 8.1. CFP MDIO Interface

Table 8.1. CFP Register Allocation

Starting Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 Use.
8000	807F	RO	128	8	CFP NVR 1. Basic ID registers.
8080	80FF	RO	128	8	CFP NVR 2. Extended ID registers.
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers.
8180	81FF	RO	128	8	CFP NVR 4.
8200	83FF	RO	4x128	N/A	MSA Reserved.
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers.
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers.
8500	86FF	RO	6x128	N/A	Reserved by CFP MSA.
8800	887F	R/W	128	8	User NVR 1. User data registers.
8880	88FF	R/W	128	8	User NVR 2. User data registers.
8900	8FFF	RO	14x128	N/A	Reserved by CFP MSA.
9000	9FFF	RO	4096	N/A	Reserved for vendor private use.
A000	A07F	R/W	128	16	CFP Module VR 1. CFP Module level control / DDM registers.
A080	A0FF	RO	128	16	Reserved by CFP MSA.
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA.
A200	A27F	R/W	128	16	Network Lane VR 1. Network lane specific registers.
A280	A2FF	R/W	128	16	Network Lane VR 2. Network lane specific registers.
A300	A3FF	RO	2x128	N/A	Reserved by CFP MSA.
A400	A47F	R/W	128	16	Host Lane VR 1. Host lane specific registers.
A480	AFFF	RO	23x128	N/A	Reserved by CFP MSA.
B000	FFFF	RO	5x4096	N/A	Reserved by CFP MSA.

8.2 Non-Volatile Register (NVR) Map

Table 8.2.1. CFP NVR-1

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value and Description	LSB Unit
Base ID Information						
8000	1	RO	7~0	Module Identifier	0Eh: CFP	
8001	1	RO		Extended Identifier		N/A
			7~6	Power Class	00b: Power Class 1 Module (8Wmax)	N/A
			5~4	Lane Ratio Type	10b: Network lane : Host lane = n : n	N/A
			3~1	WDM Type	001b: CWDM	N/A
			0	CLEI Presence	0: No CLEI code present, 1: CLEI code present	N/A
8002	1	RO	7~0	Connector Type Code	01h : SC, 07h : LC	N/A
8003	1	RO	7~0	Ethernet Application Code	05h: 40GE SMF 10km, 40GE-LR4	N/A
8004	1	RO	7~0	Fiber Channel Application Code	00h: Undefined type	N/A
8005	1	RO	7~0	Copper Link Application Code	00h: Undefined type	N/A
8006	1	RO	7~0	SONET/SDH Application Code	00h: Undefined type	N/A
8007	1	RO	7~0	OTN Application Code	00h: Undefined type	N/A
8008	1	RO		Additional Capable Rates		N/A
			7~5	Reserved		0
			4	111.8 Gbps	0: Not supported	N/A
			3	103.125 Gbps	0: Not supported	N/A
			2	41.25 Gbps	1: Supported. (SCF040x0L4)	N/A
			1	43 Gbps	1: Supported (SCF0410L4,SCF0420L4) 0: Not supported (SCF0400L4)	N/A
			0	39.8 Gbps	0: Not supported	N/A
8009	1	RO		Number of Lanes Supported		N/A
			7~4	Number of Network Lanes	4: 4 lanes	N/A
			3~0	Number of Host Lanes	4: 4 lanes	N/A
800A	1	RO		Media Properties		N/A
			7~6	Media Type	00b: SMF	N/A
			5	Directionality	0: Normal	N/A
			4	Optical Multiplexing and De-multiplexing	1: With optical MUX/DEMUX	N/A
			3~0	Active Fiber per Connector	4: 4 TX Lanes and 4 RX Lanes	N/A
800B	1	RO	7~0	Maximum Network Lane Bit Rate	8-bit value x 0.2 Gbps	0.2 Gbps
800C	1	RO	7~0	Maximum Host Lane Bit Rate	8-bit value x 0.2 Gbps	0.2 Gbps
800D	1	RO	7~0	Maximum Single Mode Optical Fiber Length	8-bit value x 1 km for single mode fiber length	1 km
800E	1	RO	7~0	Maximum Multi-Mode Optical Fiber Length	8-bit value x 10 m for multi-mode fiber length	10 m
800F	1	RO	7~0	Maximum Copper Cable Length	8-bit value x 1 m for copper cable length	1 m
8010	1	RO		Transmitter Spectral Characteristics 1		N/A
			7~5	Reserved	0	0
			4~0	Number of Active Transmit Fibers	1: 1 fiber	N/A
8011	1	RO		Transmitter Spectral Characteristics 2		N/A
			7~5	Reserved	0	0
			4~0	Number of Wavelengths per active Transmit Fiber	4: 4 wavelenghts	N/A
8012	2	RO	7~0	Minimum Wavelength per Active Fiber	C594h : 1264.5nm	0.025 nm

Table 8.2.1. CFP NVR-1 (Continued)

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value and Description	LSB Unit
Base ID Information						
8014	2	RO	7~0	Maximum Wavelength per Active Fiber	D0FCh: 1337.5 nm	0.025 nm
8016	2	RO	7~0	Maximum per Lane Optical Width	32C8h: 13000pm	1 pm
8018	1	RO		Device Technology 1		N/A
			7~4	Laser Source Technology	0010b: DFB	N/A
			3~0	Transmitter modulation technology	0000b: DML	N/A
8019	1	RO		Device Technology 2		N/A
			7	Wavelength control	0: No wavelength control	N/A
			6	Cooled transmitter	0: Un-cooled transmitter device	N/A
			5	Tunability	0: Transmitter not Tunable	N/A
			4	VOA implemented	0: Detector side VOA not implement	N/A
			3~2	Detector Type	01b: PIN detector	N/A
			1	CDR with EDC	0: CDR without EDC	N/A
			0	Reserved	0	0
801A	1	RO		Signal Code		N/A
			7~6	Modulation	01b: NRZ	N/A
			5~2	Signal coding	0000b: Non-PSK	N/A
			1~0	Reserved	00b	0
801B	1	RO	7~0	Maximum Total Optical Output Power per Connector	43h: 6700uW	100 uW
801C	1	RO	7~0	Maximum Optical Input Power per Network Lane	10h: 1600uW	100 uW
801D	1	RO	7~0	Maximum Power Consumption	28h: 8W	200 mW
801E	1	RO	7~0	Maximum Power Consumption in Low Power Mode	64h: 2W	20 mW
801F	1	RO	7~0	Maximum Operating Case Temp Range	46h: 70deg C	1 degC
8020	1	RO	7~0	Minimum Operating Case Temp Range	0h: 0deg C	1 degC
8021	16	RO	7~0	Vendor Name	"SumitomoElectric"	N/A
8031	3	RO	7~0	Vendor OUI	5Fh	N/A
8034	16	RO	7~0	Vendor Part Number	"SCF04x0L4xNxxxxx"	N/A
8044	16	RO	7~0	Vendor Serial Number	Manufacturer serial number in ASCII code.	N/A
8054	8	RO	7~0	Date Code	Date code in YYYYMMDD	N/A
805C	2	RO	7~0	Lot Code	Lot code in ASCII code.	N/A
805E	10	RO	7~0	CLEI Code	CLEI Code in ASCII code.	N/A
8068	1	RO	7~0	CFP MSA Hardware Specification Revision Number	A: Rev. 1.0	N/A
8069	1	RO	7~0	CFP MSA Management Interface Specification Revision Number	C: Rev. 1.2	
806A	2	RO	7~0	Module Hardware Version	02h: 0.2 (ES), 10h: 1.0 (CS)	N/A
806C	2	RO	7~0	Module Firmware Version	02h: 0.2 (ES), 10h: 1.0 (CS)	N/A

Table 8.2.1. CFP NVR-1 (Continued)

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value and Description	LSB Unit
Base ID Information						
806E	1	RO		Digital Diagnostic Monitoring		N/A
			7~4	Reserved	0	0
			3	Received power measurement type	1: Average Power	N/A
			2	Transmitted power measurement type	1: Average Power	N/A
			1~0	Reserved	0	0
806F	1	RO		DDM Capability 1		N/A
			7~6	Transceiver auxiliary monitor 2	00b: Not supported	N/A
			5~4	Transceiver auxiliary monitor 1	00b: Not supported	N/A
			3	Reserved	0	0
			2	Transceiver SOA bias current monitor	0: Not supported	N/A
			1	Transceiver power supply voltage monitor	1: supported	N/A
			0	Transceiver temperature monitor	1: supported	N/A
8070	1	RO		Digital Diagnostic Monitoring Capability 2	Per lane DDM capability	N/A
			7~4	Reserved	0	0
			3	Network Lane received power monitor	1: supported	N/A
			2	Network Lane laser output power monitor	1: supported	N/A
			1	Network Lane laser bias current monitor	1: supported	N/A
			0	Network Lane laser temperature monitor	0: Not supported	N/A
8071	1	RO		Module Enhanced Options		
			7	Host Lane Loop-back	0: Not supported	
			6	Host Lane PRBS Supported	0: Not supported	
			5	Host Lane emphasis control	0: Not supported	
			4	Network Lane Loop-back	0: Not supported	
			3	Network Lane PRBS	0: Not supported	
			2	Decision Threshold Voltage	0: Not supported	
			1	Decision Phase control functions	0: Not supported	
			0	Unidirectional TX/RX only Operation	0: Not supported	
8072	1	RO	7~0	Maximum High-Power-up Time	5h: 5 sec	1 sec
8073	1	RO	7~0	Maximum TX-Turn-on Time	Ah: 10 sec	1 sec
8074	1	RO	7~0	Host Lane Signal Spec	2: XLAUI	N/A
8075	1	RO		Heat Sink Type		N/A
			7~1	7:1 Reserved	0	0
			0	Heat Sink Type	1: Integrated heat Sink 0: Flat Top	N/A
8076	9	RO		Reserved		0
807F	1	RO	7~0	CFP NVR 1 Checksum	The 8-bit unsigned sum of all CFP NVR 1 contents from address 8000h through 807Eh	N/A

Table 8.2.2. CFP NVR-2

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value and Description	LSB Unit
Alarm/Warning Threshold Registers						
8080	2	RO	7~0	Transceiver Temp High Alarm Threshold	5000h: 80deg C	1/256 degC
8082	2	RO	7~0	Transceiver Temp High Warning Threshold	4800h: 75deg C	
8084	2	RO	7~0	Transceiver Temp Low Warning Threshold	F600h: -10deg C	
8086	2	RO	7~0	Transceiver Temp Low Alarm Threshold	F100h: -15deg C	
8088	2	RO	7~0	VCC High Alarm Threshold	943Eh: 3.7950V	0.1 mV
808A	2	RO	7~0	VCC High Warning Threshold	8DCCh: 3.6300V	
808C	2	RO	7~0	VCC Low Warning Threshold	7404h: 2.9700V	
808E	2	RO	7~0	VCC Low Alarm Threshold	6D92h: 2.8050V	
8090	2	RO	7~0	SOA Bias Current High Alarm Threshold	FFFFh	2 uA
8092	2	RO	7~0	SOA Bias Current High Warning Threshold	FFFFh	
8094	2	RO	7~0	SOA Bias Current Low Warning Threshold	0000h	
8096	2	RO	7~0	SOA Bias Current Low Alarm Threshold	0000h	
8098	2	RO	7~0	Auxiliary 1 Monitor High Alarm Threshold	FFFFh	TBD
809A	2	RO	7~0	Auxiliary 1 Monitor High Warning Threshold	FFFFh	
809C	2	RO	7~0	Auxiliary 1 Monitor Low Warning Threshold	0000h	
809E	2	RO	7~0	Auxiliary 1 Monitor Low Alarm Threshold	0000h	
80A0	2	RO	7~0	Auxiliary 2 Monitor High Alarm Threshold	FFFFh	TBD
80A2	2	RO	7~0	Auxiliary 2 Monitor High Warning Threshold	FFFFh	
80A4	2	RO	7~0	Auxiliary 2 Monitor Low Warning Threshold	0000h	
80A6	2	RO	7~0	Auxiliary 2 Monitor Low Alarm Threshold	0000h	
80A8	2	RO	7~0	Laser Bias Current High Alarm Threshold	C350h: 100.0000mA	See A2A0h
80AA	2	RO	7~0	Laser Bias Current High Warning Threshold	9C40h: 80.0000mA	
80AC	2	RO	7~0	Laser Bias Current Low Warning Threshold	0000h	
80AE	2	RO	7~0	Laser Bias Current Low Alarm Threshold	0000h	

Table 8.2.2. CFP NVR-2 (Continued)

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value and Description	LSB Unit
Alarm/Warning Threshold Registers						
80B0	2	RO	7~0	Laser Output Power High Alarm Threshold	845Ch: 5.30dBm	See A2B0h
80B2	2	RO	7~0	Laser Output Power High Warning Threshold	5383h: 3.30dBm	
80B4	2	RO	7~0	Laser Output Power Low Warning Threshold	0630h: -8.00dBm	
80B6	2	RO	7~0	Laser Output Power Low Alarm Threshold	03E8h: -10.00dBm	
80B8	2	RO	7~0	Laser Temperature High Alarm Threshold	FFFFh	See A2C0h
80BA	2	RO	7~0	Laser Temperature High Warning Threshold	FFFFh	
80BC	2	RO	7~0	Laser Temperature Low Warning Threshold	0000h	
80BE	2	RO	7~0	Laser Temperature Low Alarm Threshold	0000h	
80C0	2	RO	7~0	Receive Optical Power High Alarm Threshold	845Ch: 5.30dBm	See A2D0h
80C2	2	RO	7~0	Receive Optical Power High Warning Threshold	5383h: 3.30dBm	
80C4	2	RO	7~0	Receive Optical Power Low Warning Threshold	0232h: -12.50dBm	
80C6	2	RO	7~0	Receive Optical Power Low Alarm Threshold	0162h: -14.50dBm	
80C8	55	RO	7~0	Reserved	00h	0
80FF	1	RO	7~0	CFP NVR 2 Checksum	The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h through 80FEh	NA

Table 8.2.3. CFP NVR-3

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value and Description	LSB Unit
Network Lane BOL Measurements						
8100	32	RO	7~0	RX Sensitivity Spec for network lanes 0 ~ 15.	FB82h: -11.5dBm	0.01 dBm
8120	32	RO	7~0	TX Power Spec for network lanes 0 ~ 15.	00E6h: 2.3dBm	0.01 dBm
8140	32	RO	7~0	Measured ER for network lanes 0 ~ 15.	015Eh: 5dB	0.01 dB
8160	32	RO	7~0	Path Penalty for network lanes 0 ~ 15.	00C8h: 2.0dB	0.01 dB

Table 8.2.4. CFP NVR-4

Hex Addr	Size	Access Type	Bit	Register Name Bit Filed Name	Value and Description	LSB Unit
8180	1	RO	7~0	CFP NVR 3 Checksum	The 8-bit unsigned sum of all CFP NVR 3 contents from address 8100h through 817Fh	
8181	127	RO	7~1	Reserved	00h	N/A

9. Qualification Testing

The SCF0400L4 series 40Gb/s transceivers are qualified to Sumitomo Electric Industries internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

10. RoHS COMPLIANCY

Compliancy versus requirements contained inside the following reference document is guaranteed: "Directive 2002/95/EC of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment" from official journal of European Union (European Parliament and of the Council). This product is Compliant at RoHS-6/6 level and contains no leaded solders.

11. Laser Safety Information

The SCF0400L4 series transceivers use a semiconductor laser that is classified as Class 1 laser products per the laser safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC60825-1:2007 and IEC60825-1:2001 International standards.

Caution

If this product is used under conditions not recommended in the specification or is used with unauthorized revision, the classification for laser product safety is invalid. Reclassify the product at your responsibility and take appropriate safety measures.

12. Electromagnetic Compatibility

EMI (Emission)

The SCF0400L4 series 40Gb/s transceivers are designed to meet FCC Class B limits for emissions and noise immunity per CENELEC EN50 081 and 082 specifications.

RF Immunity

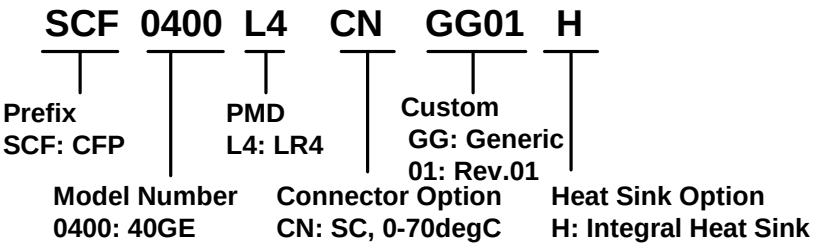
The SCF0400L4 has an immunity to operate when tested in accordance with IEC 61000-4-3 (80- 1000MHz, Test Level 3) and GR-1089.

Electrostatic Discharge (ESD) Immunity

The SCF0400L4 has an immunity against direct and indirect ESD when tested accordance with IEC 61000-4-2.

13. Ordering Information

13.1. Part Numbering System



13.2. Evaluation Board Kit

For test purposes the evaluation board model number SK0400A may be ordered to use with the SCF0400L4 series transceivers.

SK0400A : SCF0400/0410 CFP evaluation board

14. Ordering Number

Table 14. SCF0400L4 Series Part Number Information

MPN	Optical I/F		Operating Lane Data Rate				
	40GE-LR4	C4S1-2D1	9.95328Gb/s	10.3125Gb/s	10.75460Gb/s	11.14274Gb/s	11.14584Gb/s
SC and Flat Top							
SCF0400L4CNGG01	V			V			
SCF0410L4CNGG01	V		V	V	V	V	V
SCF0420L4CNGG01	V	V	V	V	V	V	V
LC and Flat Top							
SCF0400L4LNGG01	V			V			
SCF0410L4LNGG01	V		V	V	V	V	V
SCF0420L4LNGG01	V	V	V	V	V	V	V
SC and Heat Sink Top							
SCF0400L4CNGG01H	V			V			
SCF0410L4CNGG01H	V		V	V	V	V	V
SCF0420L4CNGG01H	V	V	V	V	V	V	V
LC and Heat Sink Top							
SCF0400L4LNGG01H	V			V			
SCF0410L4LNGG01H	V		V	V	V	V	V
SCF0420L4LNGG01H	V	V	V	V	V	V	V

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