

# FLC157XP

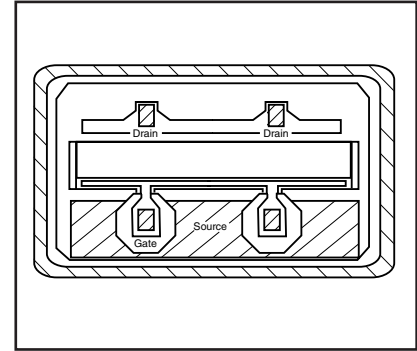
## GaAs FET & HEMT Chips

### FEATURES

- High Output Power:  $P_{1dB} = 31.5\text{dBm}$  (Typ.)
- High Gain:  $G_{1dB} = 6.0\text{dB}$ (Typ.)
- High PAE:  $\eta_{add} = 29.5\%$ (Typ.)
- Proven Reliability

### DESCRIPTION

The FLC157XP chip is a power GaAs FET that is designed for general purpose applications in the C-Band frequency range as it provides superior power, gain, and efficiency.



Eudyna stringent Quality Assurance Program assures the highest reliability and consistent performance.

### ABSOLUTE MAXIMUM RATING (Ambient Temperature $T_a=25^\circ\text{C}$ )

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	$V_{DS}$		15	V
Gate-Source Voltage	$V_{GS}$		-5	V
Total Power Dissipation	$P_{tot}$	$T_c = 25^\circ\text{C}$	8.3	W
Storage Temperature	$T_{stg}$		-65 to +175	$^\circ\text{C}$
Channel Temperature	$T_{ch}$		175	$^\circ\text{C}$

Eudyna recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage ( $V_{DS}$ ) should not exceed 10 volts.
2. The forward and reverse gate currents should not exceed 9.6 and -1.0 mA respectively with gate resistance of  $200\Omega$ .
3. The operating channel temperature ( $T_{ch}$ ) should not exceed  $145^\circ\text{C}$ .

### ELECTRICAL CHARACTERISTICS (Ambient Temperature $T_a=25^\circ\text{C}$ )

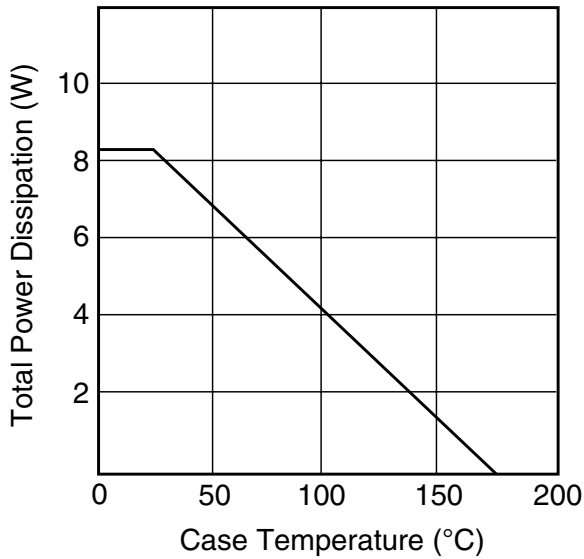
Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Saturated Drain Current	$I_{DSS}$	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}$	-	600	900	mA
Transconductance	$g_m$	$V_{DS} = 5\text{V}, I_{DS} = 400\text{mA}$	150	300	-	mS
Pinch-off Voltage	$V_p$	$V_{DS} = 5\text{V}, I_{DS} = 30\text{mA}$	-1.0	-2.0	-3.5	V
Gate Source Breakdown Voltage	$V_{GSO}$	$I_{GS} = -30\mu\text{A}$	-5	-	-	V
Output Power at 1dB Gain Compression Point	$P_{1dB}$	$V_{DS} = 10\text{V}$ $I_{DS} \approx 0.6I_{DSS}$ $f = 8\text{GHz}$	30.5	31.5	-	dBm
Power Gain at 1dB Gain Compression Point	$G_{1dB}$		5.0	6.0	-	dB
Power-added Efficiency	$\eta_{add}$		-	29.5	-	%
Thermal Resistance	$R_{th}$	Channel to Case	-	15	18	$^\circ\text{C/W}$

Note: RF parameter sample size 10pcs. criteria (accept/reject)=(2/3)

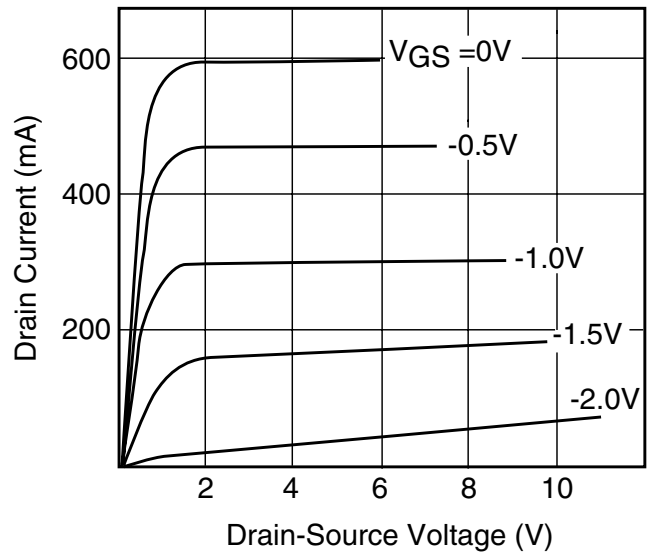
The chip must be enclosed in a hermetically sealed environment for optimum performance and reliability.

**Eudyna**

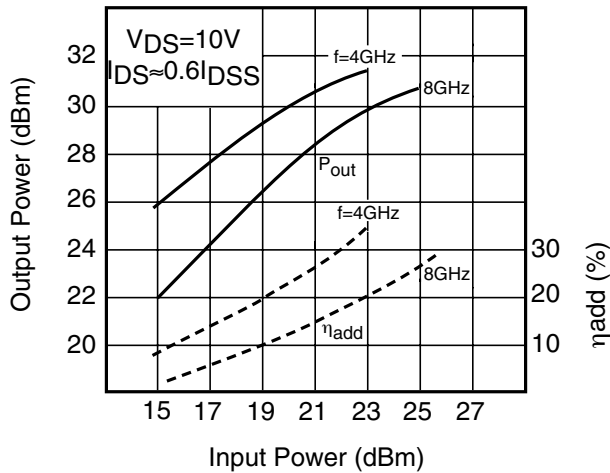
**POWER DERATING CURVE**



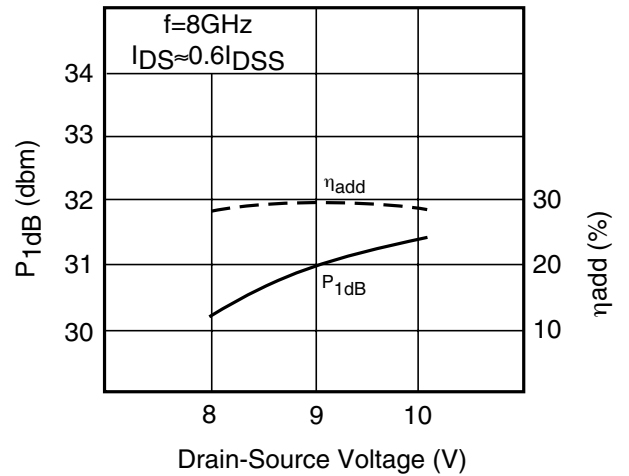
**DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE**



**OUTPUT POWER vs. INPUT POWER**



**P<sub>1dB</sub> & η<sub>add</sub> vs. V<sub>DS</sub>**



## S-PARAMETERS

$V_{DS} = 10V, I_{DS} = 400mA$

FREQUENCY (MHZ)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	.993	-25.9	15.864	165.0	.013	76.4	.185	-39.7
500	.918	-98.4	10.322	123.1	.041	40.2	.293	-115.6
1000	.881	-134.6	6.162	100.0	.049	24.2	.337	-139.9
2000	.868	-159.5	3.250	77.3	.051	15.8	.375	-150.6
3000	.868	-169.8	2.178	61.7	.051	14.8	.413	-152.6
4000	.871	-176.3	1.625	48.3	.050	16.3	.456	-153.5
5000	.875	178.9	1.284	36.0	.050	19.3	.503	-154.9
6000	.881	174.8	1.051	24.6	.050	23.3	.550	-156.8
7000	.886	171.2	.878	13.8	.052	27.9	.597	-159.3
8000	.892	167.8	.743	3.7	.054	32.5	.641	-162.2
9000	.897	164.6	.633	-5.8	.057	36.7	.682	-165.4
10000	.903	161.5	.541	-14.6	.061	40.2	.720	-168.7
11000	.907	158.4	.462	-22.9	.067	42.8	.753	-172.1
12000	.912	155.5	.393	-30.5	.072	44.6	.783	-175.6

NOTE:\* The data includes bonding wires.

n: number of wires      Gate    n=2 (0.3mm length, 25µm Dia Au wire)  
                                  Drain    n=2 (0.3mm length, 25µm Dia Au wire)  
                                  Source n=4 (0.3mm length, 25µm Dia Au wire)

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