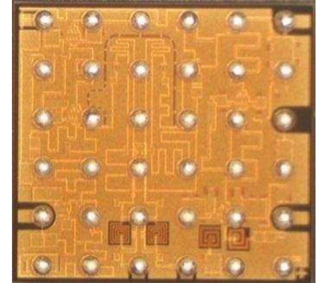
SMM5146XZ

12.7 – 15.4GHz Down converter MMIC



FEATURES

- Wafer Level Chip Scale Package with Solder Ball
- Integrated Balanced Mixer, LO Buffer Amplifier, Low Noise Amplifier and x2 multiplier
- 10dB Conversion Gain :10dB
- Input Third Order Intercept Point (IIP3) : +2dBm
- Low Noise Figure : 2.6dB
- +10dBm LO Drive Level

DESCRIPTION

The SMM5146XZ is a image-rejection down converter MMIC for applications in the 12.7 to 15.4GHz frequency range. The device consists of a image rejection resistive PHEMT mixer, LO amplifier, Low Noise Amplifier and x2 multiplier in a flip chip form. The flip chip die can be used in solder reflow process.
Sumitomo Electric Device Innovations's stringent Quality Assurance Program assures the highest reliability and consistent performance.a

ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
Drain Voltage	V_{DD}	6	V
Gate Voltage (for Gain Control)	V_{GC}	-1	V
Input RF Power	Pin_{RF}	0	dBm
Input LO Power	Pin_{LO}	15	dBm
Storage Temperature	Tstg	-40 to +125	deg.C

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Conditions	Unit
Drain Voltage	V_{DD}	5	V
Gate Voltage (for Gain Control)	V_{GC}	-0.5 to 0	V
Input LO Power	Pin_{LO}	10	dBm
Operating Case Temperature	Tc	-40 to +85	deg.C

ELECTRICAL CHARACTERISTICS (Case Temperature Tc=25deg.C)

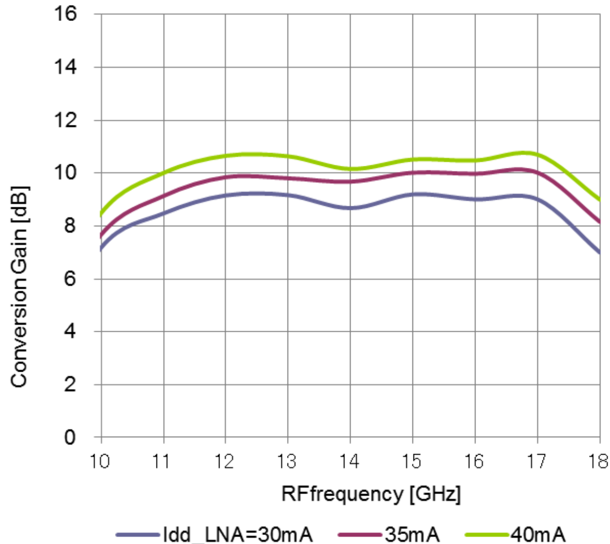
Item	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
RF Frequency Range	f_{RF}	V_{DD_LOA}=5V	12.7		15.4	GHz
IF Frequency Range	f_{IF}	V_{DD_LNA}=5V	DC		2.0	GHz
LO Frequency Range	f_{LO}	I_{DD_LNA}=35mA *1	5.3		8.7	GHz
LO Input Power	Pin_{LO}	IF=1000MHz *2	---	10	---	dBm
Conversion Gain	Gc		7	10	---	dB
Gain Control Range	ΔGain		---	8	---	dB
Noise Figure	NF		---	2.6	3.3	dB
Input 3rd.Order Intercept Point	IIP3		---	2	---	dBm
Image rejection	IR		---	20	---	dB
RF Return Loss	RL_{RF}		---	10	---	dB
LO-RF Isolation	ISO_{LO-RF}		---	30	---	dB
LO-IF Isolation	ISO_{LO-IF}		---	50	---	dB
RF-IF Isolation	ISO_{RF-IF}		---	50	---	dB
Current Consumption @ LOA	I_{DD_LOA}			100	145	mA
V_{GC} Voltage	V_{GC}		-0.5	---	0.0	V

*1. Adjust V_{GC} voltage between 0 to -0.5V to set to I_{DD_LNA}=35mA

*2. Electrical characteristics are tested with IF freq.=1000MHz and external IF 90° hybrid.

CONVERSION GAIN vs. RF FREQUENCY

@ V_{DD}=5V, T_C=+25deg.C
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



NOISE FIGURE vs. RF FREQUENCY

@ V_{DD}=5V, T_C=+25deg.C
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)

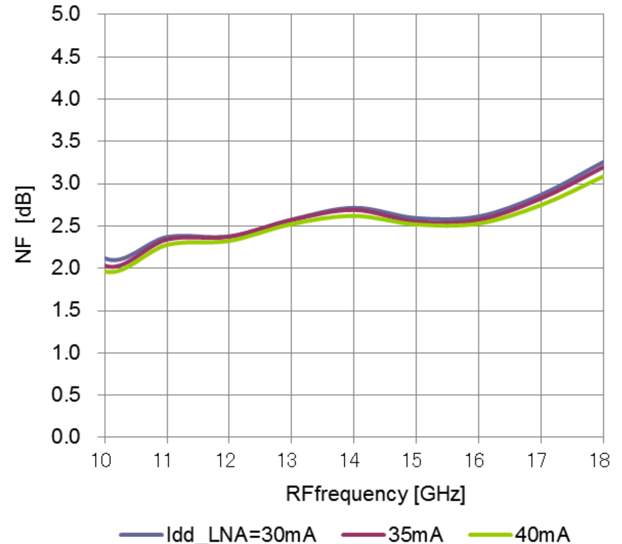
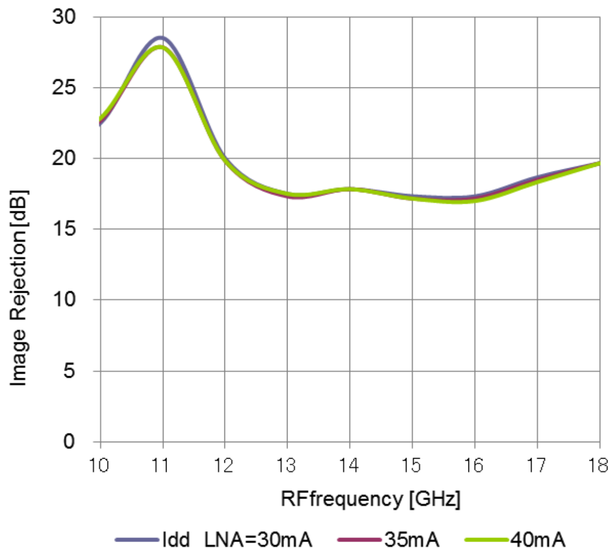


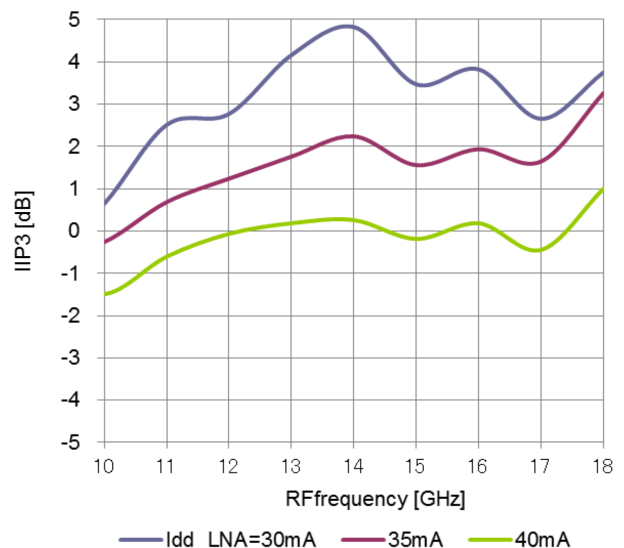
IMAGE REJECTION vs. RF FREQUENCY

@ V_{DD}=5V, T_C=+25deg.C
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



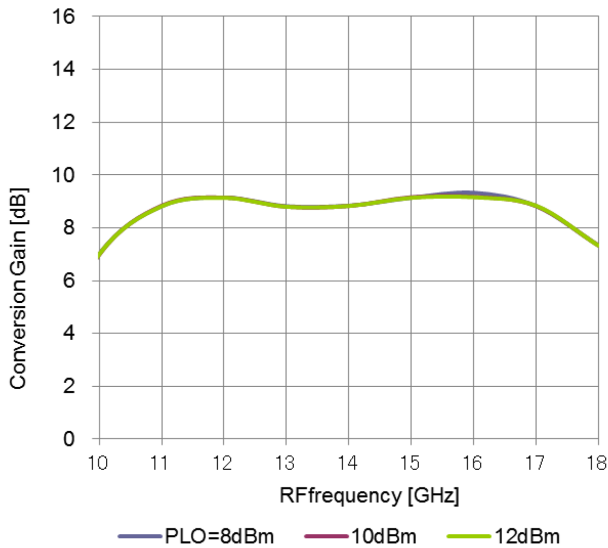
INPUT IP3 vs. RF FREQUENCY

@ V_{DD}=5V, T_C=+25deg.C
Pin_{LO}=10dBm, Pin_{RF}=-17dBm(S.C.L), f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



CONVERSION GAIN vs. FRECUENCY by LO input power

@ V_{DD}=5V, I_{DD_LNA}=35mA, T_C=+25deg.C
Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



IIP3 vs. FRECUENCY by LO input power

@ V_{DD}=5V, I_{DD_LNA}=35mA, T_C=+25deg.C
Pin_{RF}=-17dBm(S.C.L), f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)

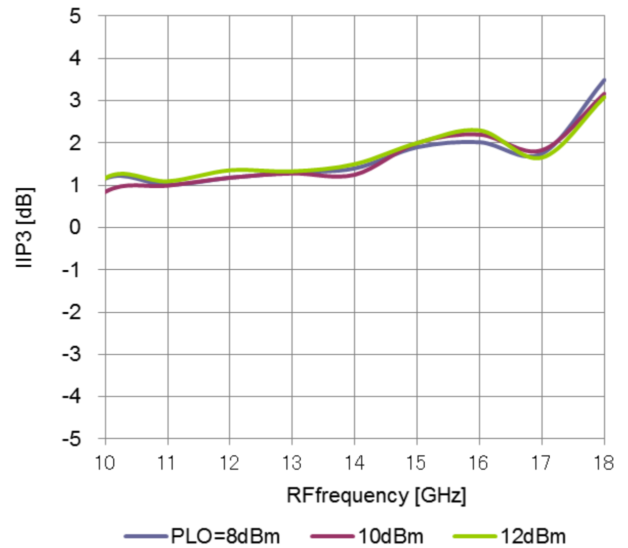
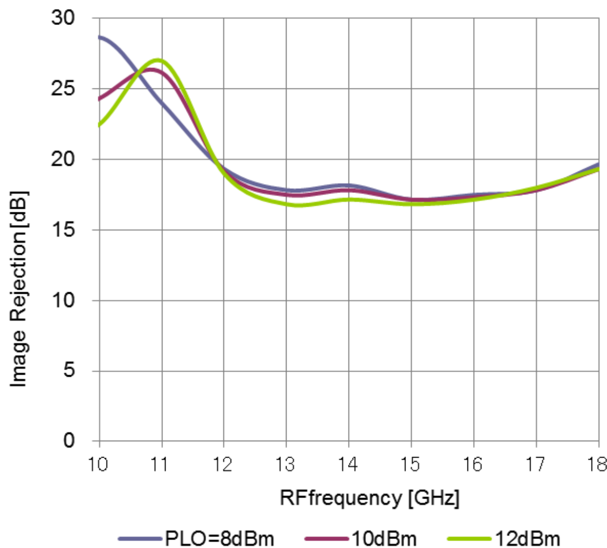


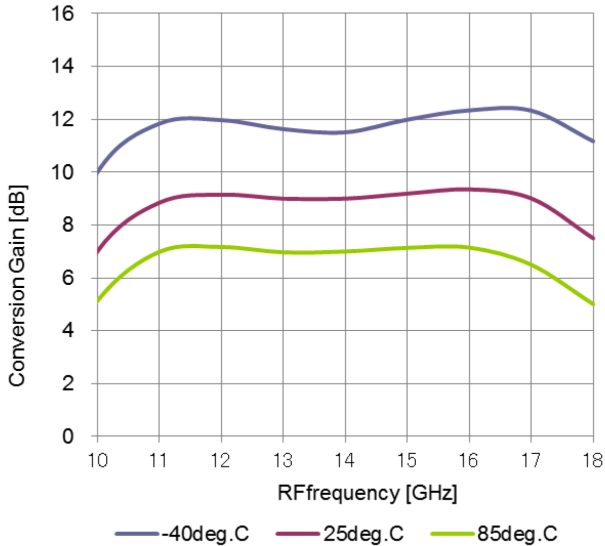
IMAGE REJECTION vs. FREQUENCY by LO input power

@ V_{DD}=5V, T_C=+25deg.C
Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



CONVERSION GAIN vs. FRECUENCY by temperature

@ V_{DD}=5V, I_{DD_LNA}=35mA
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



IIP3 vs. FRECUENCY by temperature

@ V_{DD}=5V, I_{DD_LNA}=35mA
Pin_{LO}=10dBm, Pin_{RF}=-17dBm(S.C.L.), f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)

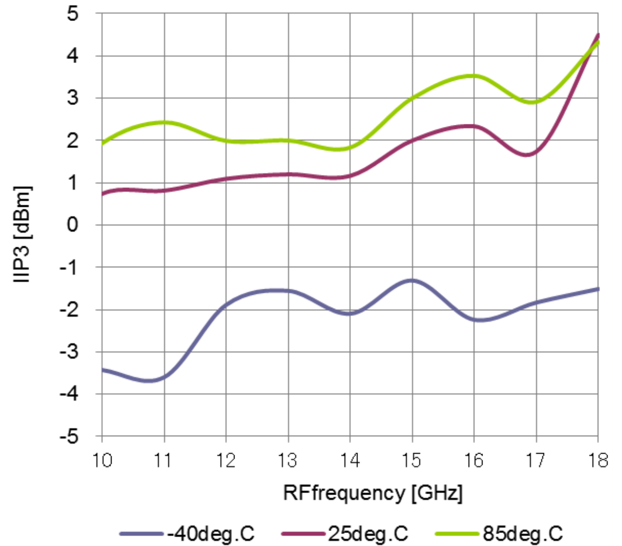
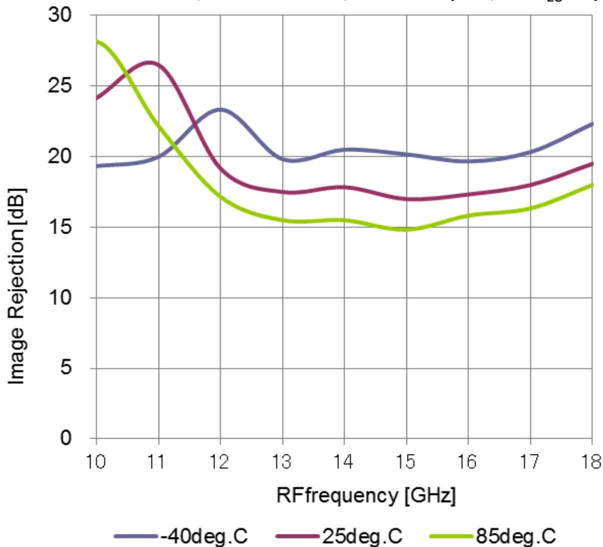


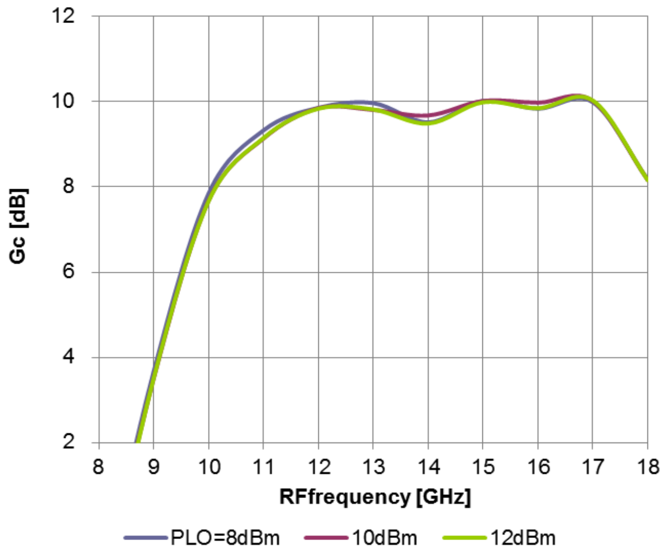
IMAGE REJECTION vs. FREQUENCY by temperature

@ V_{DD}=5V, I_{DD_LNA}=35mA
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



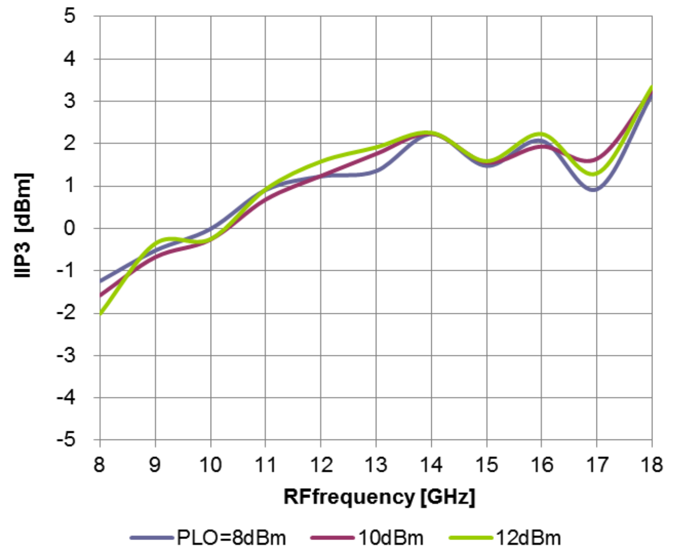
CONVERSION GAIN vs. LO INPUT POWER

@ V_{DD}=5V, I_{DD_LNA}=35mA, T_C=+25deg.C
Pin$_{RF}$=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



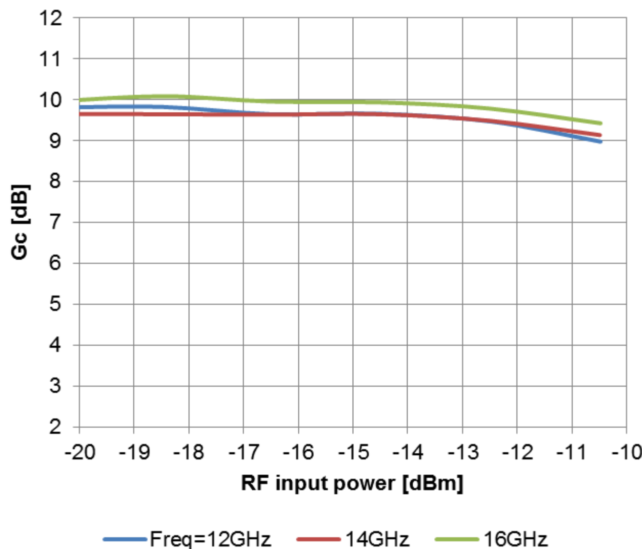
INPUT IP3 vs. LO INPUT POWER

@ V_{DD}=5V, I_{DD_LNA}=35mA, T_C=+25deg.C
Pin$_{RF}$=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



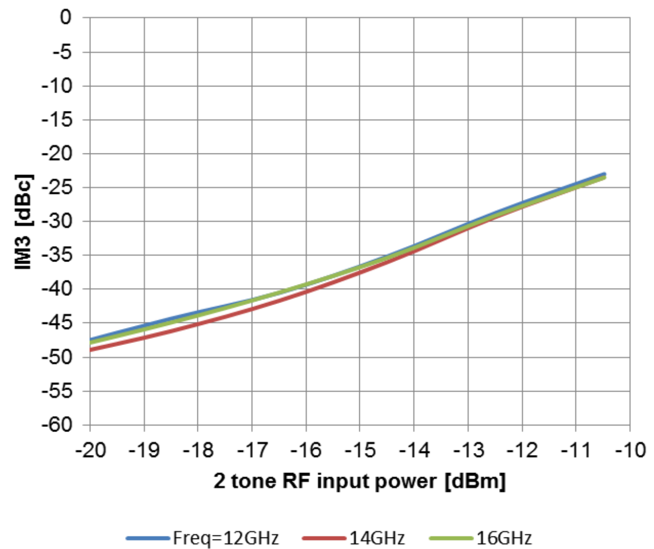
CONVERSION GAIN vs. RF INPUT POWER

@ V_{DD}=5V, I_{DD_LNA}=35mA, T_C=+25deg.C
Pin$_{RF}$=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



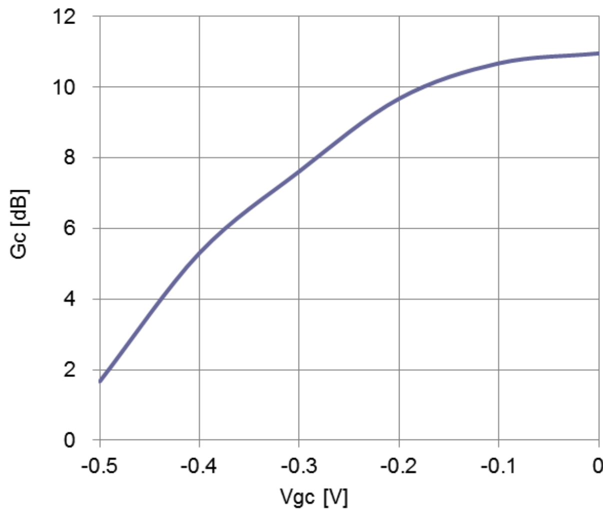
IM3 vs. RF INPUT POWER

@ V_{DD}=5V, I_{DD_LNA}=35mA, T_C=+25deg.C
Pin$_{RF}$=-17dBm(2tone), f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



CONVERSION GAIN vs. VGC

@ V_{DD}=5V, T_C=+25deg.C
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



INPUT IP3 vs. VGC

@ V_{DD}=5V, T_C=+25deg.C
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)

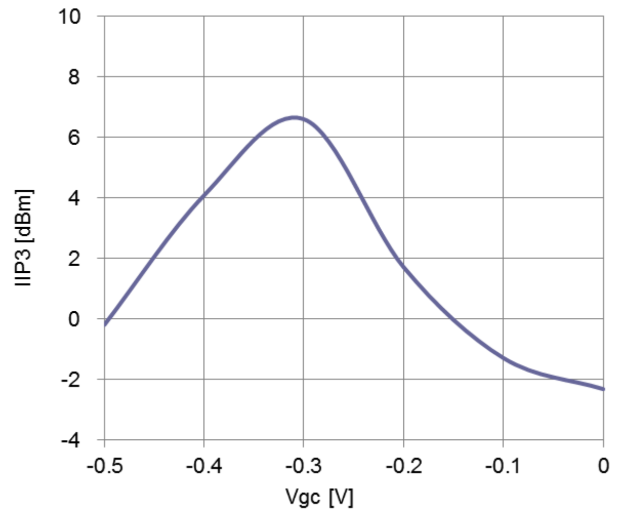
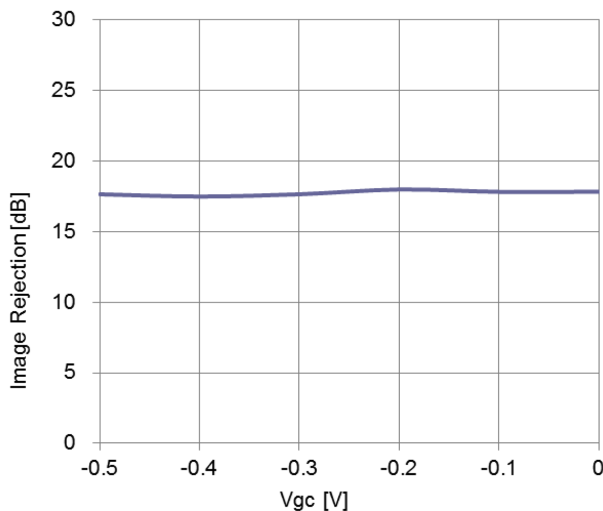


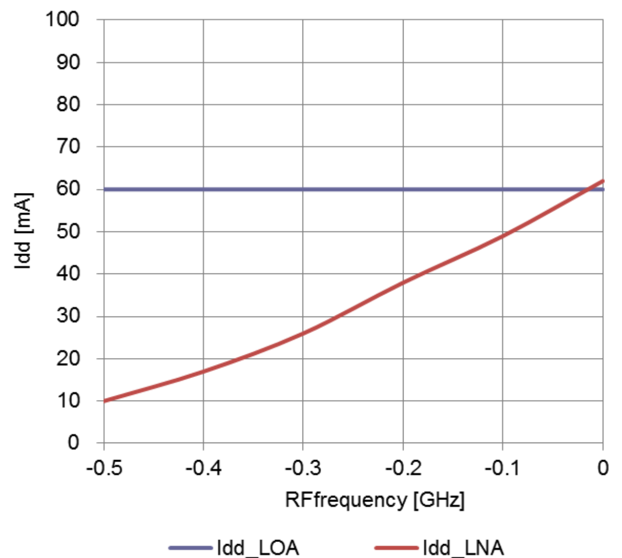
IMAGE REJECTION vs. VGC

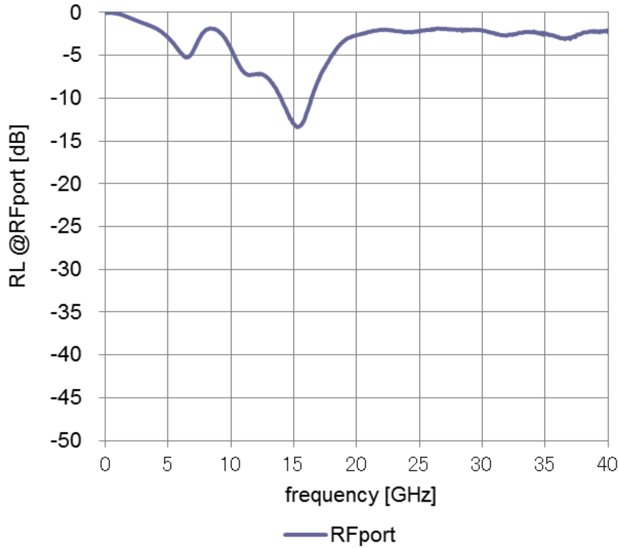
@ V_{DD}=5V, T_C=+25deg.C
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)

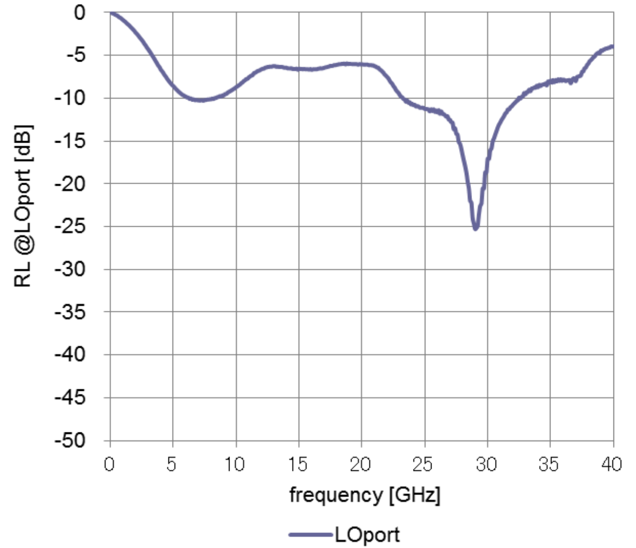


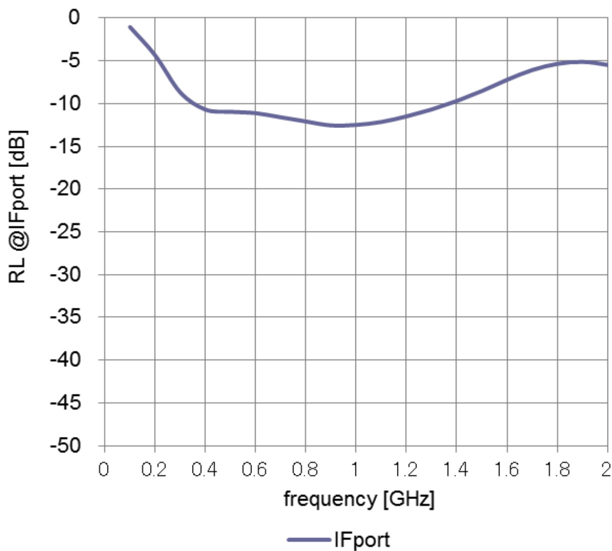
IDD vs. VGC

@ V_{DD}=5V, T_C=+25deg.C
Pin_{LO}=10dBm, Pin_{RF}=-17dBm, f_{IF}=1GHz (LSB; $f_{IF}=f_{LO}-f_{RF}$)



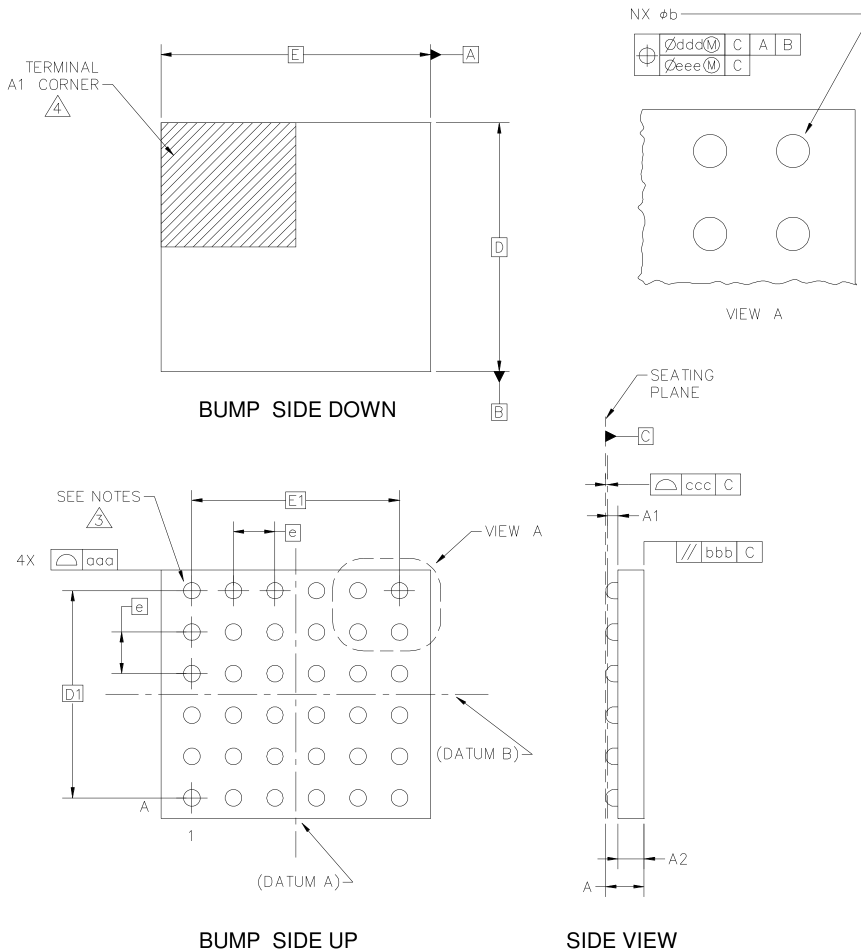






Return loss at IF port was measured with external Coupler (LDC32900M03B-703)

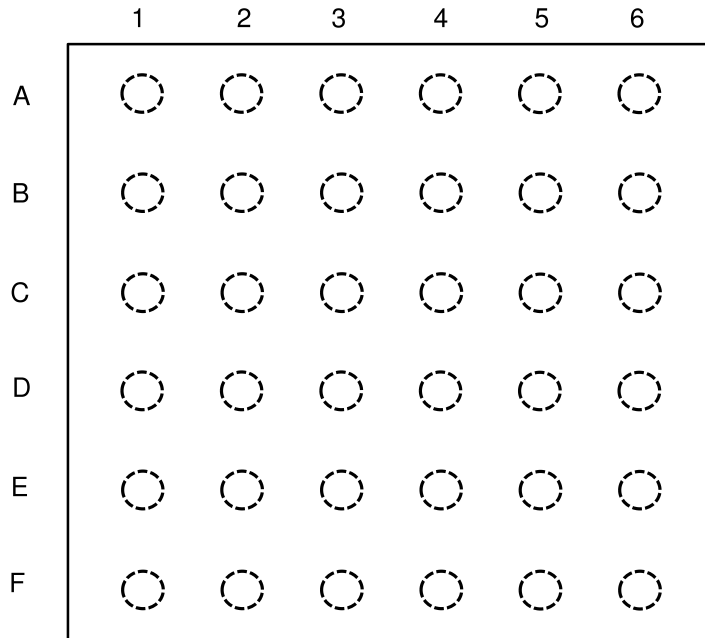
■ Chip outline



Symbol	Dimensions (typ.)	Note
A	0.396	
A1	0.121	
A2	0.275	
b	0.168	
D	2.37	
D1	2.00	
E	2.57	
E1	2.00	
e	0.40	
MD	6	
ME	6	
N	36	
aaa	0.07	
bbb	0.046	
ccc	0.03	
ddd	0.07	
eee	0.03	

NOTES :
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. △3 BALL DESIGNATION PER JEDEC STD MS-028 AND JEP95
4. △4 DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
5. PRIMARY DATUM C IS SEATING PLANE
6. ALLOY OF SOLDER BALL : Sn-3.0Ag-0.5Cu

■ Pin Assignment

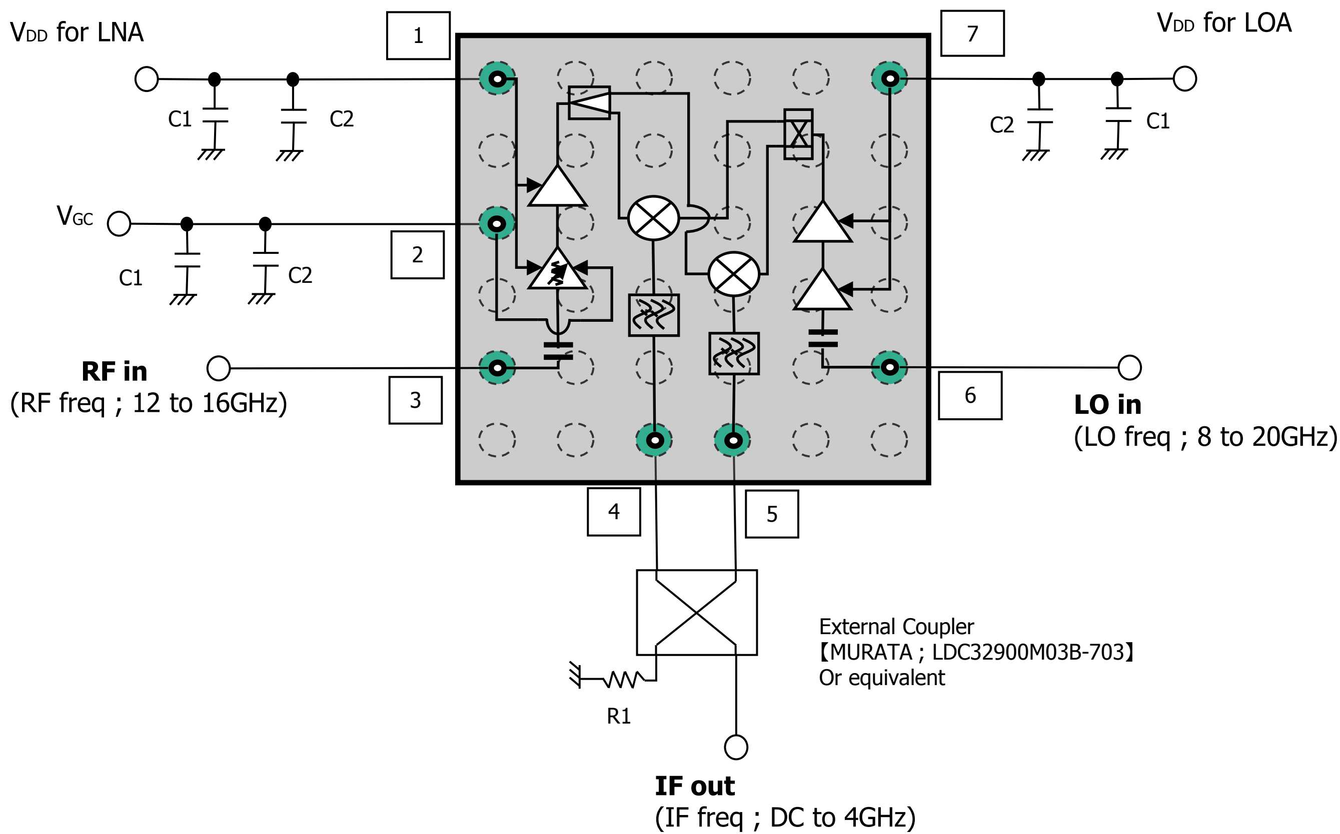


Bump Side Down (Die Top View)

Pin Assignment

	1	2	3	4	5	6
A	VDD_LNA	GND	GND	GND	GND	VDD_LOA
B	GND	GND	GND	GND	GND	GND
C	VGC	GND	GND	GND	GND	GND
D	GND	GND	GND	GND	GND	GND
E	RFIN	GND	GND	GND	GND	LOIN
F	GND	GND	IFOUT(I)	IFOUT(Q)	GND	GND

■ **Application Circuit Block Diagram**



Pin Assignment

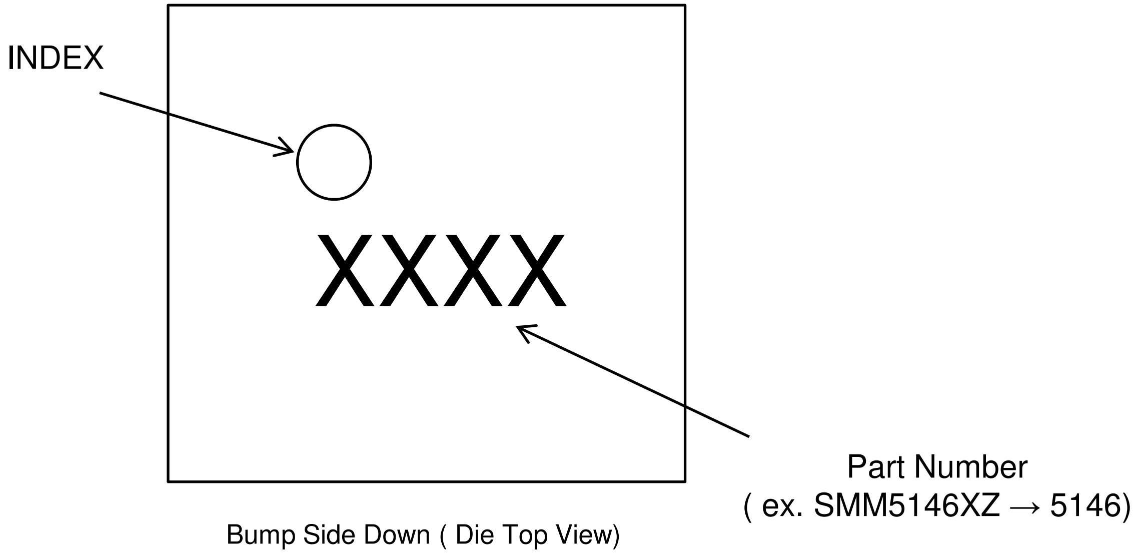
Pin	Name
1	VDD_LNA
2	VGC
3	RF Input
4, 5	IF Output
6	LO Input
7	VDD_LOA

*All bumps except Pin 1 to 7 are GND

Component List

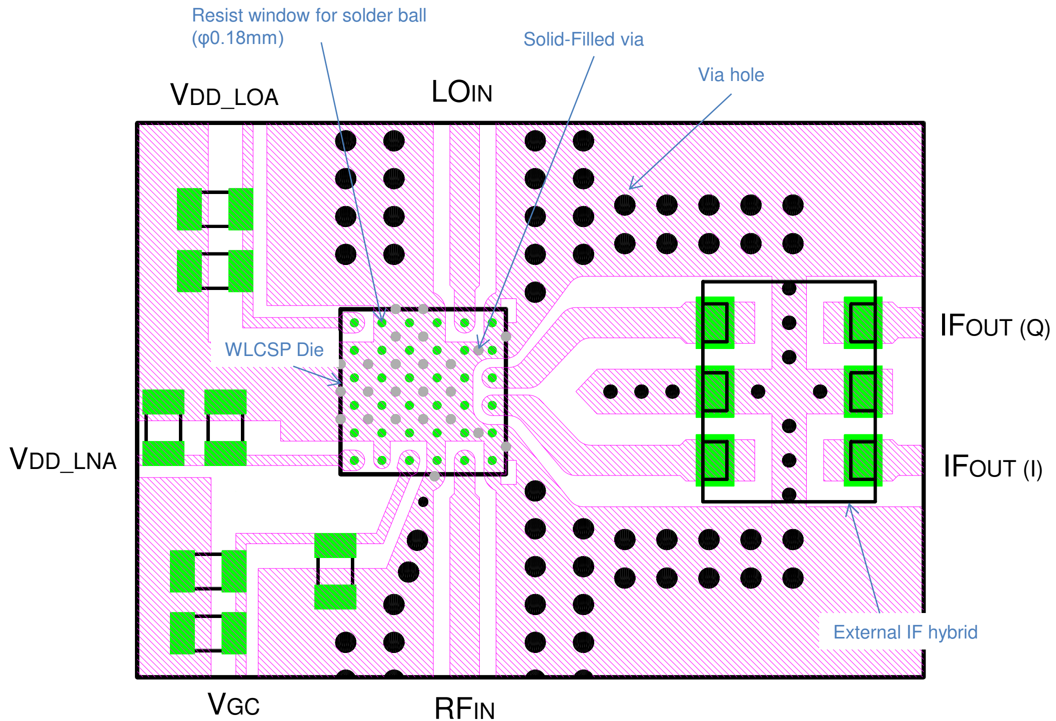
Name	Description	Value
C1	Capacitor	0.1uF
C2	Capacitor	100pF
R1	Resister	50ohm

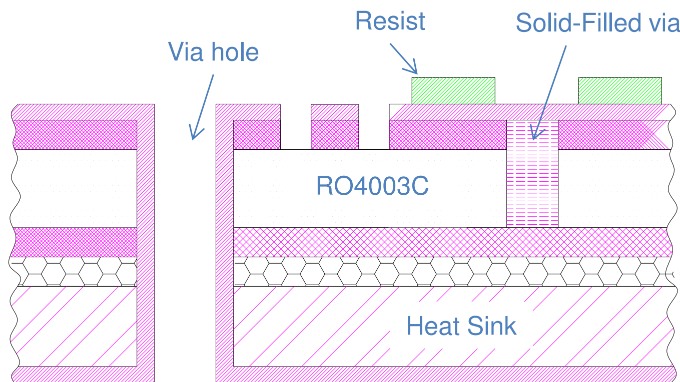
■ **Marking**



Bump Side Down (Die Top View)

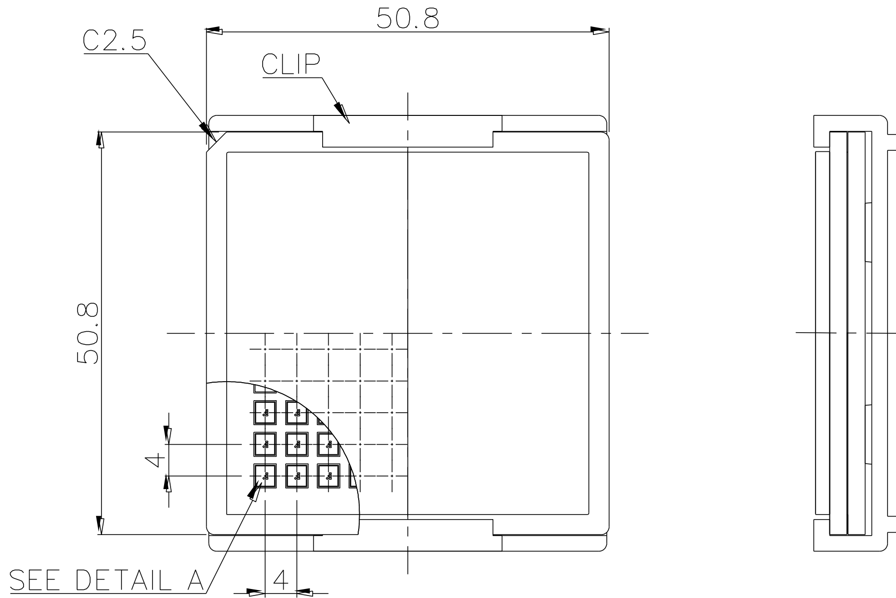
■ PCB and Solder-resist Pattern

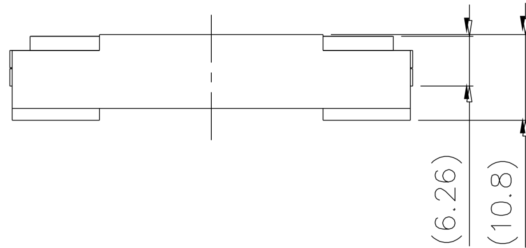


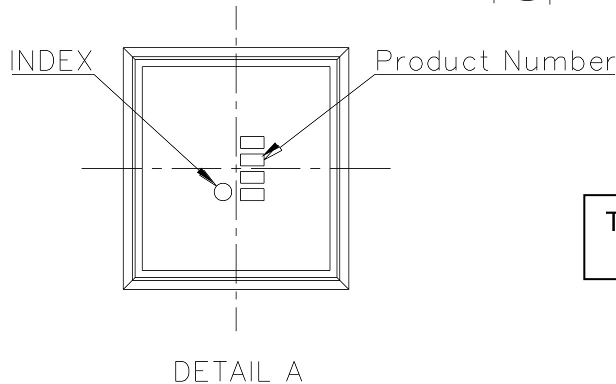


NOTES.
1) Core Material ; Rogers CORP. 4003
Thickness 0.2mm typ. , Er=3.38 typ.
2) Copper Foil Thickness ; 18um typ.
3) Finish Copper Foil ; Ni 1um min. / Au 0.1um max.
4) Resist ; +/- 20um.
5) All Dimensions are in mm.
6) Solid-filled via is used to prevent depletion of the solder from ground pad through via holes

■ **2-inch Tray Packing (Part No. : SMM5146XZ)**







Tray Material : ABS – TP10
Quantity : 100 pcs. / Tray

■ Tape and Reel Packing (Part No. : SMM5146XZT)

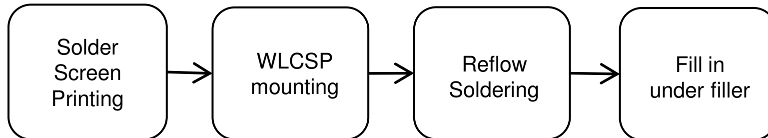
2.0 ±0.1
4.0 ±0.1
Ø1.5 +0.1/0.0
1.75 ±0.1
11.4 ±1.0
9.0 +1.0/0.0
8.0 +0.3/−0.1
Index
3.5 ±0.1
2.5 ±0.05
2.7 ±0.05
Cover tape (Thermal Attachment)
Width 5.5mm
Unwind Direction
Carrier tape
2.0 ±0.5
ϕ 180.0
(ϕ60.0)
0.18 ±0.05
0.5 ±0.1
ϕ 13.0 ±0.5
ϕ 21.0 ±0.8

Tape Material : Conductive Polycarbonate
Reel Material : Conductive Polystyrene
Quantity : 500 pcs. / Reel

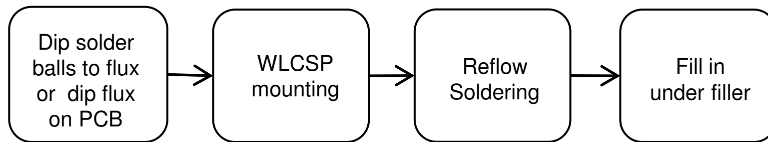
■ Assembly Techniques for WLCSP MMICs

1. WLCSP Assembly Flow

WLCSP MMIC can be handled as a standard SMT component as in the following assembly flow.



One can also make use of C4 (Controlled Collapse Chip Connection) assembly techniques or a flux dip assembly method. In this case lower residue flux is recommended to save cleaning process steps, as liquid cleaning is not recommended.



2. PCB Layout

PCB land patterns are based on SEI's experimental data. The land pattern has been developed and tested for optimized assembly at SEI. Solid-filled via is required to prevent depletion of the solder of solder paste and solder ball from ground pad through via holes during the reflow soldering process. To prevent shorts between solder balls, solder mask resist should be used. A recommended PCB layout is shown on page 12.

3. Stencil Mask

The use of solder mask is required to put WLCSP MMIC on PCB using standard SMT assembly techniques. The stencil mask design is critical. A minimum solder mask space of 0.16mm between solder balls must be used to prevent shorting. To realize stable solder volume, stencil thickness and opening need to be optimized. A recommended stencil mask pattern is shown in Fig. 1.

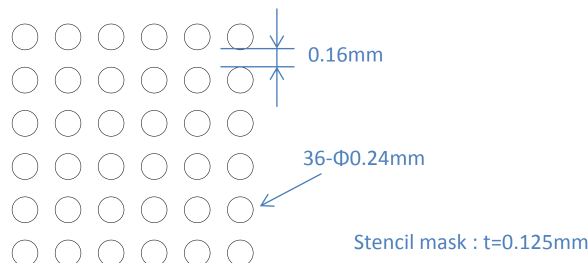


Figure 1

■ Assembly Techniques for WLCSP MMICs

4. Die Mounting

For WLCSP MMIC with fine pitch of 0.4mm, it is recommended to use automated fine-pitch placement. Due to the variety of mounting machines and parameters and surface mount processes vary from company to company, careful process development is recommended.

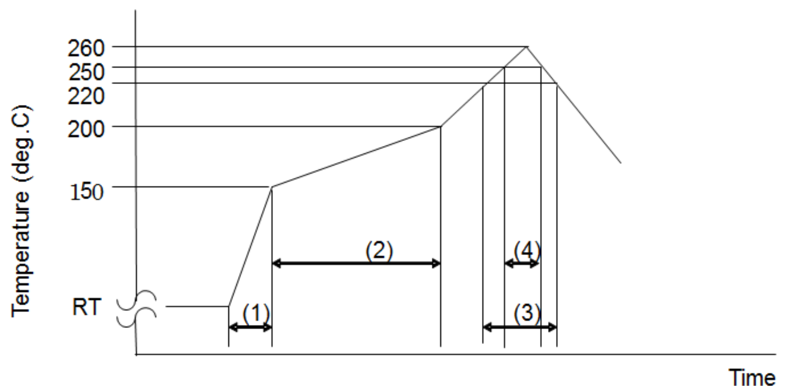
5. Reflow Soldering

The solder reflow condition (infrared reflow/heat circulation reflow/hotplate reflow) shall be optimized and verified by the customer within the condition shown in Fig.2 to realize optimum solder ability. An excessive reflow condition can degrade the WLCSP MMICs that may result in device failure. The solder reflow must be limited to three (3) cycles maximum. The temperature profile during reflow soldering shall be controlled as shown in Fig.2.

Customers must optimize and verify the reflow condition to meet their own mounting method using their own equipment and materials. For any special application, please contact the Sumitomo sales office nearest you for information.

Certain types of PCB expand and contract causing peaks and valleys in the board material during the reflow cycle. The recommended measure to prevent this from occurring is to screw the PCB onto a stiffener board with a small heat capacity prior to the reflow process.

The solder balls of WLCSP MMIC use Pb-free alloy and the melting point of the Sn/Ag/Cu used is 218deg.C The actual profile used depends on the thermal mass of the entire populated board and the solder compound used.



(1) Average Ramp-up Rate: 3deg.C /seconds
(2) Preheating : 150 to 200deg.C, 60 to 180seconds
(3) Main Heating : 220deg.C, 60seconds
(4) Peak Temperature : 260deg.C max., more than 250deg.C, 10seconds max.

Figure 2

■ Assembly Techniques for WLCSP MMICs

6. Cleaning

SEDI does not recommend a liquid cleaning system to clean WLCSP MMIC. If a liquid cleaning system is required, please contact our nearest sales office from the list at http://global-sei.com/Electro-optic/about/office.html.

7. Underfill Process

WLCSP MMIC is connected to PCB by solder balls. A major concern in using WLCSP MMICs is the ability of the solder balls to withstand temperature cycling. It is thought the stress to the solder balls due to the difference of the coefficients of thermal expansion between GaAs and PCB is a potential cause of failure. To reduce this stress, it recommended to use underfill in the gap between the WLCSP die and the PCB. In reliability tests, underfill has beneficial results in temperature cycle, drop test and mechanical stress test. The other side, underfill is undesirable due to the complexity of the process and added assembly cost from the additional process. The end user must decide to whether to use this process from their own test results.

8. ESD Protection

Semiconductor devices are sensitive to static electricity. User must pay careful attention to the following precautions when handling semiconductor devices.
Customers should lay a conductive mat on the bench, and use wrist ground straps.
When handling products with an ESD rating of class 0, customers should lay a conductive mat on the floor, and use foot ground straps. Ionizers are also recommended. All of this equipment must be periodically tested in a recommended process.
Follow ESD precautions to protect against < HBM +/-250V ESD voltage strike.

ESD	Class 0	Up to 250V
Note: Based on JEDEC JESD22-A114-C		

9. RoHS Compliance

RoHS Compliance	Yes

■ Assembly Techniques for WLCSP MMICs

10. Handling of WLCSP MMICs in Tape and Reel From

Peel the carrier tape and the top tape off slowly at a rate of 10 mm/s or less to prevent the generation of electro-static discharge. When peeling the tape off, the angle between the carrier tape and the top tape should be kept at 165 to 180 degrees as shown in Fig. 3.

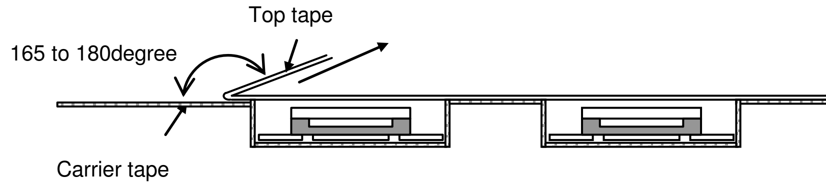


Figure 3

11. Packing

WLCSP products are offered in either the tape and reel or tray shipping configuration. The products are placed with solder bump facing down.

a) Tray Shipment
Each tray contains 100pcs. and minimum order is one tray, and must order in 100pcs. increment

b) Tape and Reel Shipment
Each reel contains 500pcs. and minimum order is one reel, and must order in 500pcs. increment

ORDERING INFORMATION

SMM5146XZ : Tray Shipment : 100pcs. /Tray and, 100pcs. (per Tray) increment.

SMM5146XZT : Tape and Reel Shipment : 500pcs. /Reel, and 500pcs. (per Reel) increment.

Part Number	Order Unit	Packing
SMM5146XZ	100 pcs.	100pcs. / Tray = 100pcs. / Packing
SMM5146XZT	500 pcs.	500pcs. / Reel = 500pcs. / Packing

- NOTE -

This information is described as reference information based on SEI experimental test like assembly process, PCB and stencil design, Temperature cycle test result and so on.

SEI can not guarantee the quality of WLCSP after the customer’s assembly process because assembly and PCB condition is generally different between customer and SEI.

Please check the quality of device (or system) after customer assembles with customer’s PCB and assembly process.

For further information please contact:

http://global-sei.com/Electro-optic/about/office.html

CAUTION

This product contains **gallium arsenide (GaAs)** which can be hazardous to the human body and the environment. For safety, observe the following procedures:

・Do not put these products into the mouth.

・Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.

・Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.