

10Gb/s SFP Optical Transceiver Module

SPP5300SR-GL

(10GBASE-SR, 850nm VCSEL, PIN-PD)

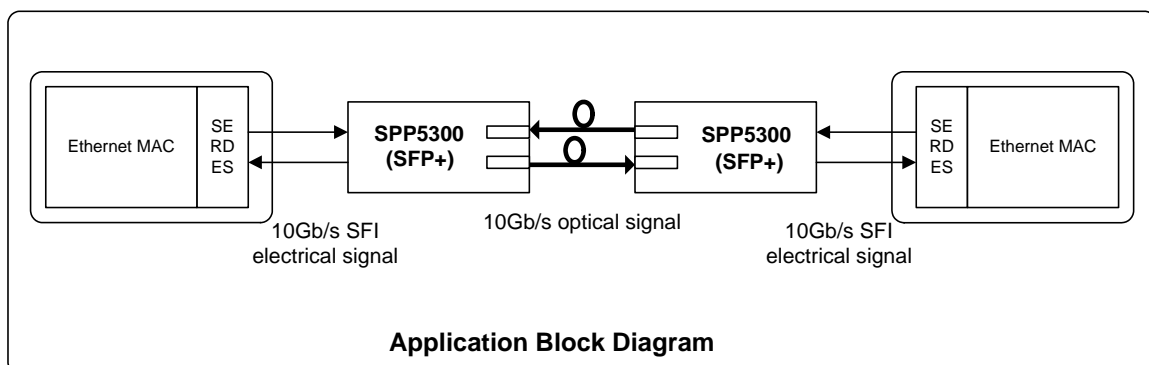
Features

- ◆ 10Gb/s Serial Optical Interface
 - High quality and reliability optical device and sub-assemblies
 - 850nm VCSEL laser for up to 300m over Multi Mode Fiber
 - High sensitivity PIN photodiode and TIA
- ◆ SFP+ MSA Compliant
 - Easy supply management for hot pluggability
 - Duplex LC Receptacle
 - SFP Mechanical Interface for easy removal
 - SFI High Speed Electrical Interface
 - 2-wire interface for management and diagnostic monitor
 - Tx_Disable and Rx_LOS functions
- ◆ Protocol
 - IEEE802.3ae 10 Gigabit Ethernet
 - LAN PHY/WAN PHY
- ◆ Power Supply Consumption
 - Single 3.3V power supply
 - Low power consumption
- ◆ RoHS6 compliant



Applications

- ◆ 10GE Ethernet switches and routers
- ◆ 10GE Storage
- ◆ Inter Rack Connection
- ◆ Other high speed data connections



1. General Description

The SPP5300SR-GL is a very compact 10Gb/s optical transceiver module for serial optical communication applications at 10Gb/s. The SPP5300SR-GL converts a 10Gb/s serial electrical data stream to 10Gb/s optical output signal and a 10Gb/s optical input signal to 10Gb/s serial electrical data streams. The high speed 10Gb/s electrical interface is fully compliant with SFI specification.

The SPP5300SR-GL is designed for Ethernet LAN (10.3Gb/s) applications. The high performance 850nm VCSEL transmitter and high sensitivity PIN receiver provide superior performance for Ethernet applications at up to 300m links.

The fully SFP compliant form factor provides hot pluggability, easy optical port upgrades and low EMI emission.

Table 1. Fiber compliance

SFP+ type	Wavelength [nm]	Cable Type	Core Size (micron)	Modal Bandwidth [MHz*km]	Cable distance
10GB-SR	850	MMF	62.5	160	26m(FDDI-Grade)
			62.5	200	33m(OM1)
			50.0	400	66m
			50.0	500	82m(OM2)
			50.0	2000	300m(OM3)

2. Functional Description

The SPP5300SR-GL contains a duplex LC connector for the optical interface and a 20-pin connector for the electrical interface. Figure 2.1 shows the functional block diagram of SPP5300SR-GL SFP Transceiver.

Transmitter Operation

The transceiver module receives 10Gb/s electrical data and transmits the data as an optical signal.

The transmitter output can be turned off by Tx disable signal, TX_DIS pin. When TX_DIS is asserted High, Transmitter is turned off.

Receiver Operation

The received optical signal is converted to serial electrical data signal.

The RX_LOS signal indicates insufficient optical power for reliable signal reception at the receiver.

Management Interface

A 2-wire interface (SCL, SDA) is used for serial ID, digital diagnostics and other control /monitor functions.

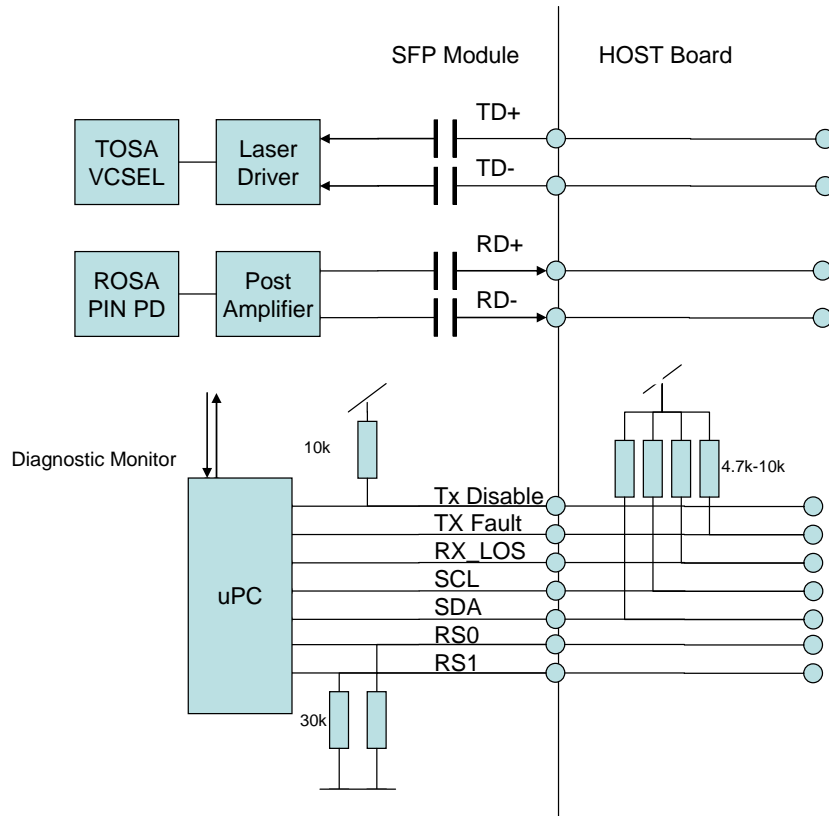


Figure 2.1. Functional Block Diagram

3. Package Dimensions

Figure 3.1. shows the package dimensions of SPP5300SR-GL. SPP5300SR-GL is designed to be compliant with SFP MSA specification. Package dimensions are specified in SFF-8432.

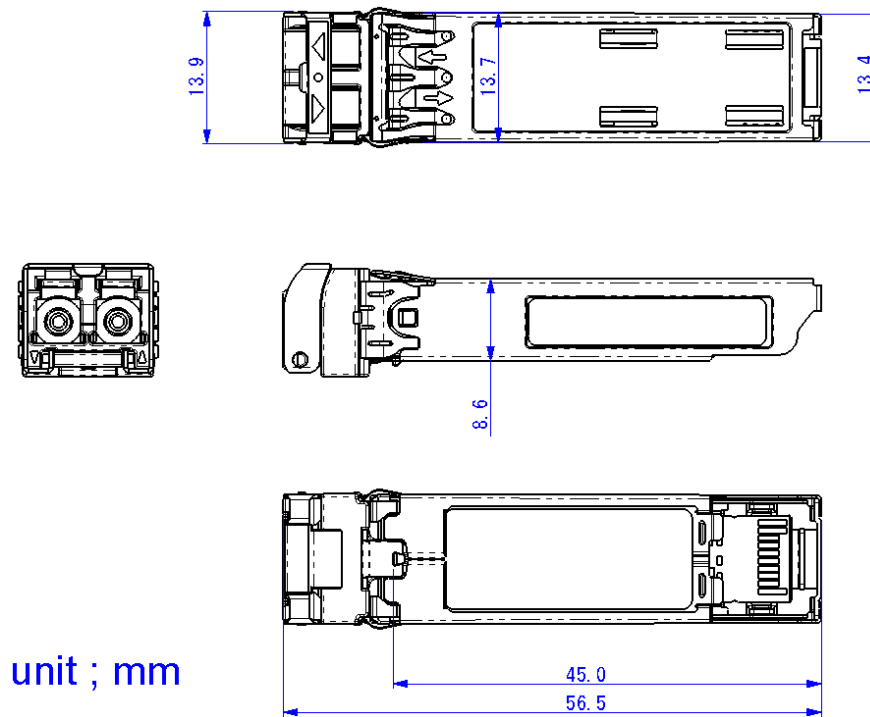


Figure 3.1. Package dimensions

4. Pin Assignment and Pin Description

4.1. SFP Transceiver Electrical Pad Layout

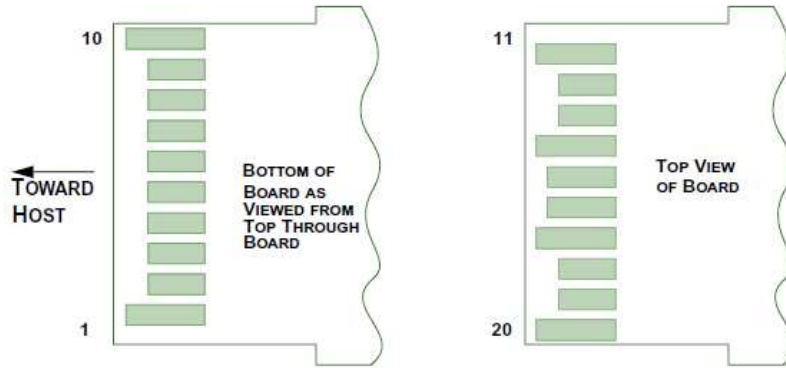


Figure 4.1. SFP Transceiver Electrical Pad Layout

4.2. Host PCB SFP Pinout

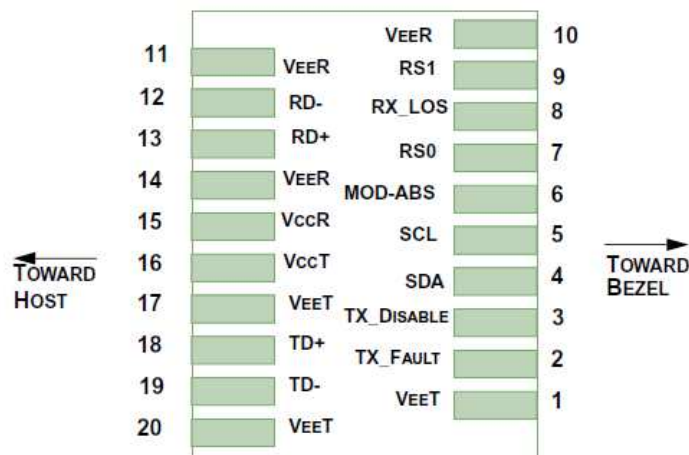


Figure 4.2. Host PCB SFP Pinout

4.3. Pin Descriptions

Table 4.3. Pin Description

Pin#	Name	Logic	Description	Power Sequence Order	Note
1	VeeT		Module Transmitter Ground	1 st	1
2	Tx_Fault	LVTTL-O	Module Transmitter Fault	3 rd	2
3	Tx_Disable	LVTTL-I	Transmitter Disable, Turns off transmitter laser output	3 rd	3
4	SDA	LVTTL-I/O	2 Wire Serial Interface Data Line(Same as MOD-DEF2 as defined in the INF-8074i)	3 rd	
5	SCL	LVTTL-I/O	2 Wire Serial Interface Data Line(Same as MOD-DEF1 as defined in the INF-8074i)	3 rd	
6	MOD_ABS		Module Absent, connected to VeeT or VeeR in the module	3 rd	2
7	RS0	LVTTL-I	Rate Select 0 (not functional for 10GE type)	3 rd	
8	RX_LOS	LVTTL-O	Receiver Loss of Signal Indication	3 rd	2
9	RS1	LVTTL-I	Rate Select 1 (not functional for 10GE type)	3 rd	
10	VeeR		Module Receiver Ground	1 st	1
11	VeeR		Module Receiver Ground	1 st	1
12	RD-	CML-O	Receiver Inverted Data Output	3 rd	
13	RD+	CML-O	Receiver Non-Inverted Data Output	3 rd	
14	VeeR		Module Receiver Ground	1 st	1
15	VccR		Module Receiver 3.3V Supply	2 nd	
16	VccT		Module Transmitter 3.3V Supply	2 nd	
17	VeeT		Module Transmitter Ground	1 st	1
18	TD+	CML-I	Transmitter Non-Inverted Data Input	3 rd	
19	TD-	CML-I	Transmitter Inverted Data Input	3 rd	
20	VeeT		Module Transmitter Ground	1 st	1

Note

- 1: Module ground pins are isolated from the module case and chassis ground within the module.
- 2: Shall be pulled up with 4.7k to 10k ohm to a voltage between 3.15V and 3.45V on the host board.
- 3: Shall be pulled up with 4.7k to 10k ohm to VccT in the module.

5. Absolute Maximum Ratings and Recommended Operating Conditions

Table 5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Operating Case Temperature	Topc	0	70	degC	1
Supply Voltage	VccR/VccT	-0.5	3.6	V	
Voltage on LVTTTL Input	Vilvttl	-0.5	VCC3+0.5	V	
LVTTTL Output Current	Iolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power(Average)	Mip	-	0	dBm	

Note:

1: Ta: TBD(-10 to 60degC with 1.5m/s airflow)

Table 5.2. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	0	70	degC	
Relative Humidity(non-condensing)	Rhop	-	85	%	
Power Supply Voltage	VccR/VccT	3.135	3.465	V	
Total Power Consumption	Pd	-	1.0	W	1

Note:

1: The inrush current is TBD

6. Electrical Interface

6.1. High Speed Electrical Interface

SFI Application Reference model

Figure 6.1.1. shows the high speed electrical interface (SFI) compliance points.

SFI electrical interface is specified for each compliance point in the SFP MSA specification.

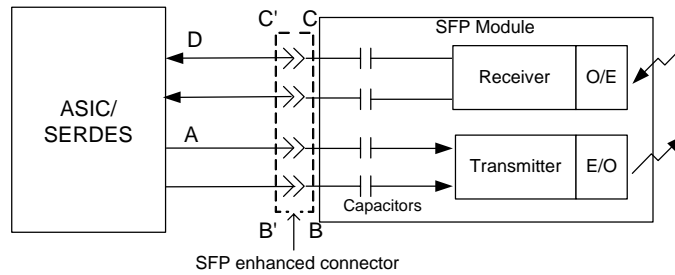


Figure 6.1.1. SFI Application Reference Model

SFI Module Transmitter Input Electrical Interface Specification at B' and Calibrated B''

Table 6.1.1. SFI Transmitter Input Electrical Specification at B'

Parameter B'	Symbol	Condition	Min	Typ.	Max.	Unit
Single Ended Output Voltage Tolerance		Referenced to VeeT	-0.3		4.0	V
AC common Input S-parameter			15			mV
Differential Input S-parameter (note 1)	SDD11	0.01-1GHz			-12	dB
		1-11.1GHz			Note 2	dB
Reflected Differential to Common Mode Conversion (note 3)	SCD11	0.01-11.1GHz			-10	dB

Note 1. Reference differential impedance is 100 ohm

2. Return Loss given by quation $SDD11(dB) = -12.9 + 0.9 * (f/1e9)$, with f in GHz

3. Common mode refernce impedance is 25 ohm

Table 6.1.2. SFI Transmitter Input Electrical Specification at B''

Parameter B''	Symbol	Condition	Min	Typ.	Max.	Unit
AC Common Mode Voltage		Note 1			15	mV(RMS)
Total Jitter	TJ	Note 1		0.28		UIpp
Data Dependant Jitter	DDJ			0.10		UIpp
Pulse Width Shrinkage Jitter	DDPWS			0.055		UIpp
Uncorrelated Jitter	UJ	Note 2		0.023		UIrms
Eye Mask Figure 6.1.2	X1			0.14		UI
	X2				0.35	UI
	Y1			90		mV
	Y2				350	mV

Note 1. Re The tester is not expected to generate this common mode voltage however its output must not exceed this value.

2. It is not possible to have the worst UJ and DDJ simultaneously and meet the TJ specifications if the UJ is all Gaussian.

SFI Module Receiver Output Electrical Interface Specification at C'

Table 6.1.3. SFI Receiver Output Electrical Specification at C'

Parameter – C'	Symbol	Conditions	Min	Typ	Max	Units
Crosstalk source rise/fall time (20% to 80%)	Tr, Tf	Note 1		34		ps
Crosstalk Source Amplitude Differential (p-p)		Note 2		700		mV
Termination Mismatch at 1 MHz	ΔZ_M				5	%
Single Ended Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage					7.5	mV (RMS)
Differential Output S-parameter (Note 3)	SDD22	0.01-1GHz			-12	dB
		1-11.1GHz			Note 4	dB
Common Mode Output Reflection Coefficient (Note 5)	SCC22	0.01-2.5GHz			-6	dB
		2.5-11.1GHz			-3	dB

Note1 : Measured with OMA test pattern. Use of five 1's and four 0's sequence in the PRBS 9 is an acceptable alternative.

- 2 : For dRNx compliance test condition. Crosstalk is not used for dRN.
- 3 : Reference differential impedance is 100 ohm.
- 4 : Differential Output S-parameter given by equation $SDD11(dB) = -12.9 + 0.9 \cdot (f/1e9)$, with f in GHz.
- 5 : Common mode reference impedance is 25 ohm.

Table 6.1.4. SFP+ Limiting Output Jitter and Eye Mask Specification at C'

Parameter – C'	Symbol	Conditions	Min	Typ	Max	Units
Output rise/fall time (20% to 80%)	Tr, Tf	Note 1	28			ps
Total Jitter	TJ	Note 2			0.70	UIpp
Deterministic Jitter	DJ				0.42	UIpp
Eye Mask Figure 6.1.3	X1				0.35	UI
	Y1		150			mV
	Y2				425	mV

Note1 : Measured at B' with Host Compliance Board and Module Compliance Board pair and with OMA test pattern. Use of five 1's and four 0's sequence in the PRBS 9 is an acceptable alternative.

2 : The data pattern for the total jitter measurement is one of IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64B/66B data traffic.

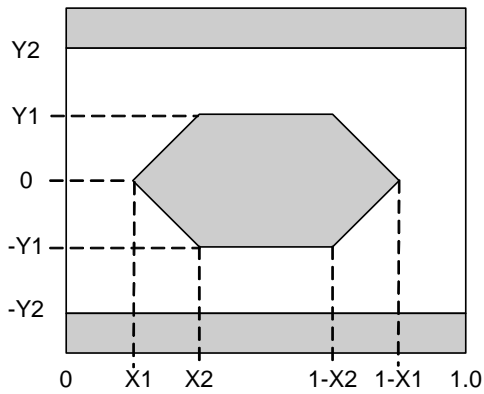


Figure 6.1.2.
Transmitter Input Eye Mask

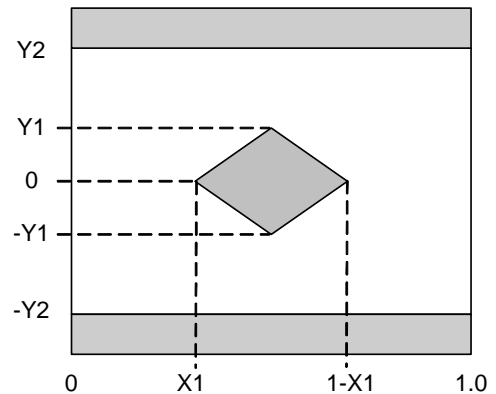


Figure 6.1.3.
Receiver Output Eye Mask

6.2. Low speed Electrical Interface

SPP5300SR-GL low speed interface is based on 2-wire interface. Management memory map is based on SFF-8472.

2-wire Electrical Specifications

Parameter	Symbol	Min	Max	Unit
Host 2-wire Vcc	Vcc_host	3.14	3.46	V
SCL and SDA	V _{OL}	0.0	0.40	V
	V _{OH}	Vcc_host-0.5	Vcc_host+0.3	V
SCL and SDA	V _{IL}	-0.3	VccT*0.3	V
	V _{IH}	VccT*0.7	VccT+0.5	V
Input current on the SCL and SDA contacts		-10	10	uA
Capacitance on SCL and SDA I/O contact			14	pF

2-wire Timing Specifications

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f _{SCL}	0	400	kHz
Clock Pulse Width Low	t _{LOW}	1.3		us
Clock Pulse Width High	t _{HIGH}	0.6		us
Time bus free before new transmission can start	t _{BUF}	20		us
START Hold Time	t _{HD, STA}	0.6		us
START Set-up Time	t _{SU, STA}	0.6		us
Data In Hold Time	t _{HD, DAT}	0		us
Data In Set-up Time	t _{SU, DAT}	0.1		us
Input Rise Time (100kHz)	t _{R, 100}		1000	ns
Input Rise Time (400kHz)	t _{R, 400}		300	ns
Input Fall Time (100kHz)	t _{F, 100}		300	ns
Input Fall Time (400kHz)	t _{F, 400}		300	ns
STOP Set-up Time	t _{SU, STO}	0.6		us
Serial Interface Clock Holdoff "Clock Stretching"	t _{clock_hold}		500	us

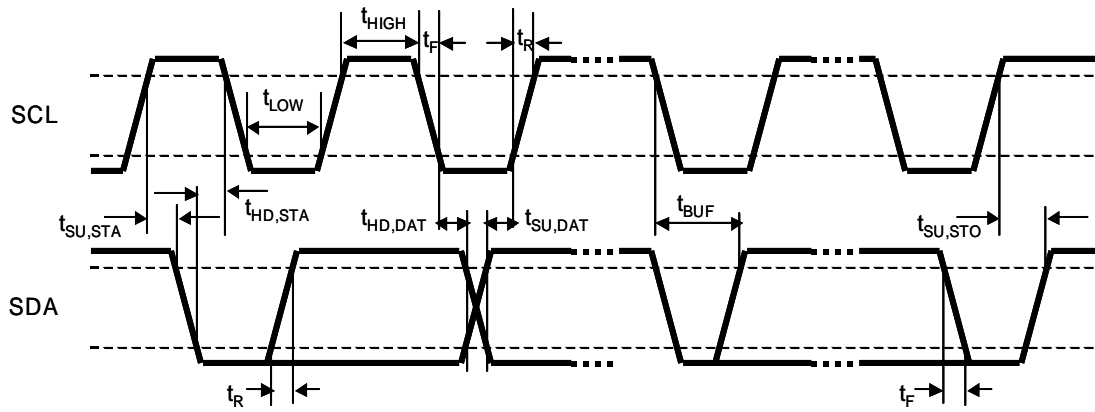


Figure 6.1.4. SFP+ Timing Diagram

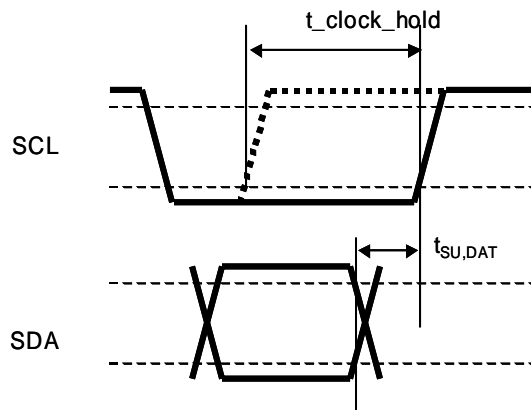


Figure 6.1.5. Detail of Clock Stretching

7. Optical Interface

Optical Interfaces of SPP5300SR-GL are defined in the IEEE802.3ae(10GBASE-SR).

Optical Transmitter

Parameter	Symbol	Min	Typ	Max	Unit
Signaling Speed (LAN PHY) (WAN PHY)		-	10.3125 9.95328		Gb/s
Signaling speed variation from nominal (max)		-100		+100	ppm
Center wavelength		840		860	nm
RMS spectral width	Lrms	Refer to Table 7.1			nm
Average launched power	Pave	-7.3		-1.3	dBm
OMA	Poma	Refer to Table 7.1 and Figure 7.2			dBm
Transmitter and dispersion penalty				3.9	dB
Average launch power of Tx OFF				-30	dBm
Extinction ratio		3.0			dB
RIN OMA				-128	dB/Hz
Optical Return Loss Tolerance				12	dB
Eye mask(X1,X2,X3,Y1,Y2,Y3)	(0.25,0.40,0.45,0.25,0.28,0.40) Note 1				

Trade-offs are available between spectral width, center wavelength and minimum optical modulation amplitude. Refer Table.7.1 and Figure 7.2.

Note 1: Refer to Figure 7.1.

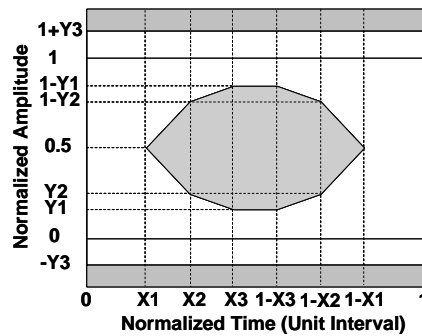


Figure.7.1. Transmission eye mask definition

Table7.1: Minimum OMA as a function of Center Wavelength and Spectral Width

Center Wavelength(nm)	RMS Spectral width (nm)								
	Up to 0.05	0.05 to 0.1	0.1 to 0.15	0.15 to 0.2	0.2 to 0.25	0.25 to 0.3	0.3 to 0.35	0.35 to 0.4	0.4 to 0.45
840 to 842	-4.2	-4.2	-4.1	-4.1	-3.9	-3.8	-3.5	-3.2	-2.8
842 to 844	-4.2	-4.2	-4.2	-4.1	-3.9	-3.8	-3.6	-3.3	-2.9
844 to 846	-4.2	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-2.9
846 to 848	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-2.9
848 to 850	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-3.0
850 to 852	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.4	-3.0
852 to 854	-4.3	-4.2	-4.2	-4.1	-4.0	-3.9	-3.7	-3.4	-3.1
854 to 856	-4.3	-4.3	-4.2	-4.1	-4.0	-3.9	-3.7	-3.4	-3.1
856 to 858	-4.3	-4.3	-4.2	-4.1	-4.0	-3.9	-3.7	-3.5	-3.1
858 to 860	-4.3	-4.3	-4.2	-4.2	-4.1	-3.9	-3.7	-3.5	-3.2

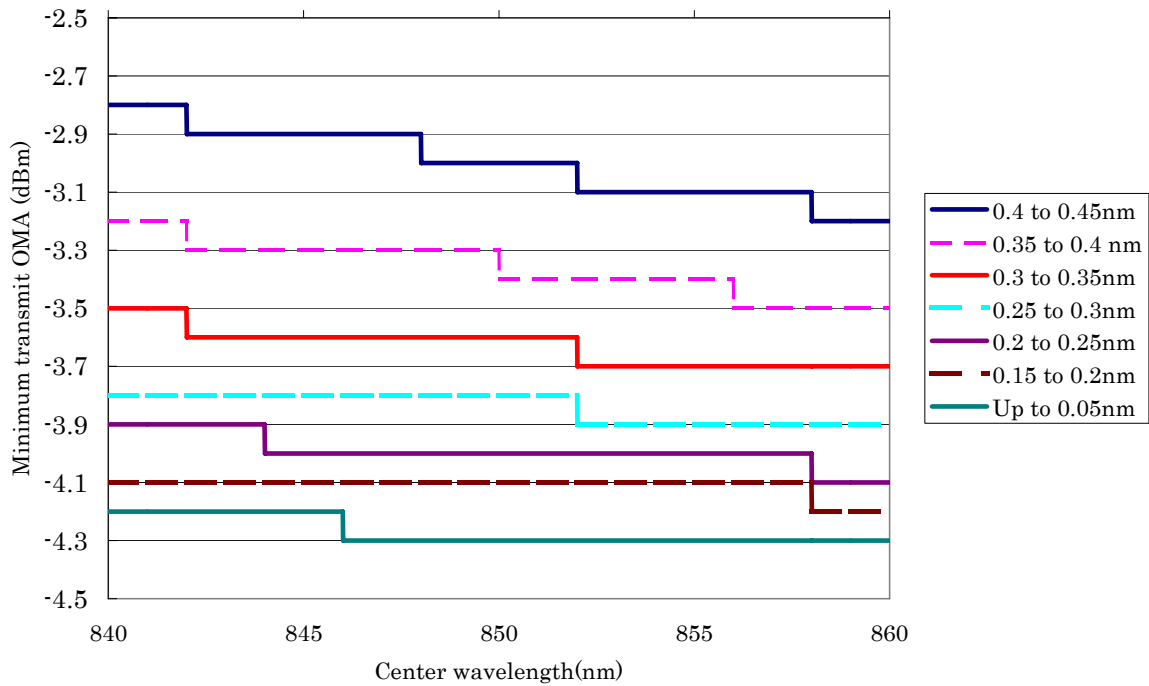


Figure 7.2:Trade-offs OMA-Center wavelength

Optical Receiver

Parameter	Symbol	Min	Typ	Max	Unit
Wavelength		840		860	nm
Signaling Speed (LAN PHY)			10.3125		Gb/s
(WAN PHY)			9.95328		
Signaling speed variation from nominal (max)		-100		+100	ppm
Average receiver power		-9.9		-1.0	dBm
Receiver sensitivity in OMA				-11.1	dBm
Receiver Reflectance				-12	dB
Stressed receiver sensitivity in OMA				-7.5	dBm
Vertical eye closure penalty		3.5			dB
Stressed ey jitter		0.3			UIpp
Receive electrical 3dB upper cutoff frequency				12.3	GHz

Note 1 : Receiver sensitivity is informative. Stressed receiver sensitivity shall be measured with conformance test signal for BER=10⁻¹².

8. Electrical and Optical I/O Signal Relationship

Table.8.1. TX_DIS vs. Optical Output Power

TX_DIS	Optical Output Power
Low ($V_{IL} = -0.3$ to $0.8V$)	Enabled
High ($V_{IH} = 2.0$ to $VCC3+0.3V$)	Disabled ($<-30dBm$)

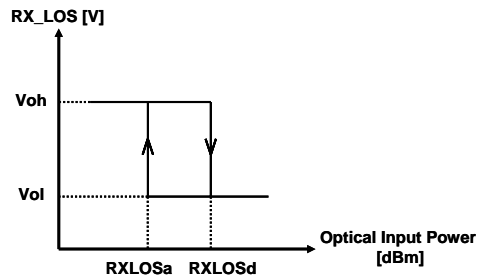


Figure.8.1. Optical Input Power vs. RX_LOS

9. User Interface

9.1. SFP Mechanical Interface

SFP Mechanical Interface is specified in the SFF-8432. Also, bail latch system is adequate for the particular specification.

9.2. Management Interface

SFP 2-Wire Serial Interface Protocol

SFP 2-wire serial interface is specified in the SFF-8472.

The SFP 2-wire serial interface is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all SFP modules.

The 2-wire serial interface address of the SFP module is A0h and A2h. In order to access to a specific module on the 2-wire serial bus, the SFP has a MOD_ABS (module absent pin). This pin, which is pulled down in the module, must be held low to notify a module installation and to allow communication over 2-wire serial interface.

SFP Management Interface

SFP Managed interface is specified in the SFF-8472.

The Figure 9.2. shows the structure of the memory map. The normal 256 Byte address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Byte is always directly available and is used for the diagnostics and control functions that must be accessed repeatedly. Multiple blocks of memories are available in the upper 128

Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. The upper address space tables are used for less frequently accessed functions and control space for future standards definition.

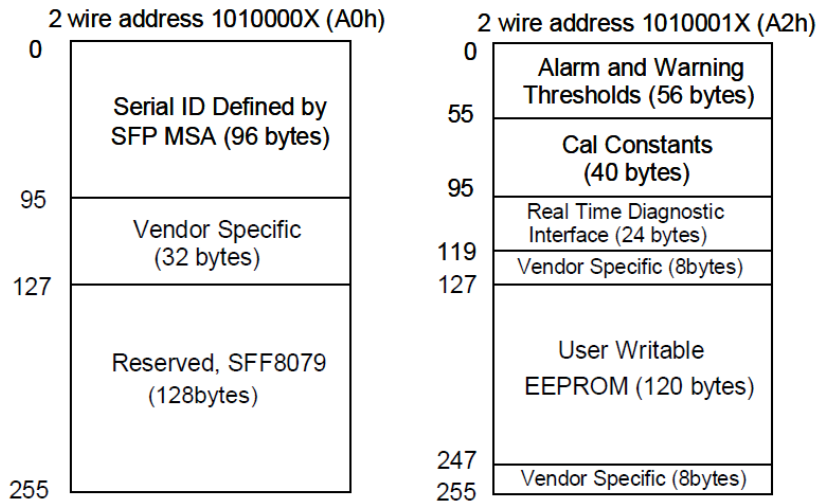


Figure 9.2. 2-wire Serial Interface Memory Map

To identify multi-sourcing OSA, vendor revision byte can be utilized as described memory map table.

9.4. Serial ID Memory Map (Data Field - Address A0h)

Address	Name of Field	Dec	Hex	ASCII	Description of Field
0	Identifier	3	03		SFP+
1	Extended Identifier	4	04		Serial ID modules
2	Connector	7	07		LC
3	Transceiver Codes	16	10		10G Base-SR
4		0	00		
5		0	00		
6		0	00		
7		0	00		
8		0	00		
9		0	00		
10		0	00		
11	Encoding	6	06		64B/66B
12	BR, Nominal	103	67		10.3Gbps
13	Rate Identifier	0	00		Unspecified
14	Length(SMF, km)	0	00		not support SMF
15	Length(SMF)	0	0		not support SMF
16	Length(50um)	8	08		82m for OM2
17	Length(62.5um)	3	03		33m for OM1
18	Length(Cable)	0	00		Copper Cable not supported
19	Length(OM3)	30	1E		300m for OM3
20	Vendor name	83	53	S	
21		117	75	u	
22		109	6D	m	
23		105	69	i	
24		116	74	t	
25		111	6F	o	
26		109	6D	m	
27		111	6F	o	
28		69	45	E	
29		108	6C	l	
30		101	65	e	
31		99	63	c	
32		116	74	t	
33		114	72	r	
34		105	69	i	
35		99	63	c	
36	Transceiver Codes	0	00		
37	Vendor OUI	0	00		
38		0	00		
39		95	5F		
40	Vendor PN	83	53	S	
41		80	50	P	
42		80	50	P	
43		53	35	5	
44		51	33	3	
45		48	30	0	
46		48	30	0	
47		83	53	S	
48		82	52	R	
49		45	2D	-	
50		71	47	G	
51		76	4C	L	
52		32	20		
53		32	20		
54		32	20		
55		32	20		
56	Vendor rev				A to Z in ASCII
57		32	20		
58		32	20		
59		32	20		
60	Wavelength	3	03		850nm Laser
61		82	52		
62	Unallocated	0	00		
63	CC_BASE				Check Code for Address 00x to 62x

Address	Name of Field	Dec	Hex	ASCII	Description of Field
64	Options	0	00		Uncooled LD, Power Level 1, Limiting Rx Output
65		26	1A		TX_DISABLE, TX_FAULT, Loss of Signal
66	BR_max	0	00		
67	BR_min	0	00		
68	Vendor SN				
69					
70					
71					
72					
73					
74					
75					
76					
77					
78					
79					
80					
81					
82					
83					
84	Date code				Year
85					
86					Month
87					
88					Day
89					
90					LOT code
91					
92	Diagnostic Monitoring Type	104	68		DDMI of SFF-8472, Internal Cal., Average Power
93	Enhanced Options	240	F0		Alarm/Warning flags, soft TX_DISABLE, soft TX_FAULT, soft RX_LOS
94	SFF-8472 Compliance	5	05		Rev1.0 of SFF-8472
95	CC_EXT				Check Code for Address 64x to 94x
96	Vendor Specific	0	00		
97		0	00		
98		0	00		
99		0	00		
100		0	00		
101		0	00		
102		0	00		
103		0	00		
104		0	00		
105		0	00		
106		0	00		
107		0	00		
108		0	00		
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119		0	00		
120		0	00		
121		0	00		
122		0	00		
123		0	00		
124		0	00		
125		0	00		
126		0	00		
127		0	00		
128-255	Reserved	0	00		

Note 1. The guaranteed +/- range of transmitter output wavelength under all normal operating conditions.

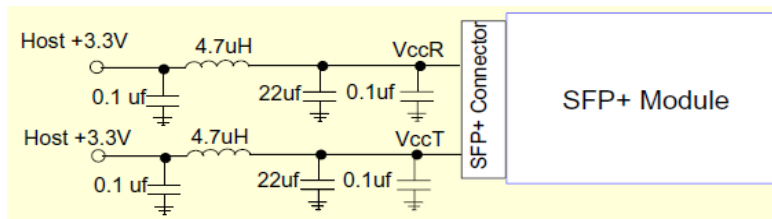


Figure 9.5. Supply Filter

9.5. Alarm/Warming threshold

A2h address	Meaning	Unit	SPP5300SR-GL
0-1	Temperature High Alarm	deg.C	75
2-3	Temperature Low Alarm	deg.C	-5
4-5	Temperature High Warning	deg.C	70
6-7	Temperature Low Warning	deg.C	0
8-9	Voltage High Alarm	V	3.63
10-11	Voltage Low Alarm	V	2.97
12-13	Voltage High Warning	V	3.465
14-15	Voltage Low Warning	V	3.135
16-17	Tx Bias High Alarm	mA	15
18-19	Tx Bias Low Alarm	mA	2
20-21	Tx Bias High Warning	mA	14
22-23	Tx Bias Low Warning	mA	2.5
24-25	Tx Power High Alarm	dBm	1.5
26-27	Tx Power Low Alarm	dBm	-11.3
28-29	Tx Power High Warning	dBm	-1.5
30-31	Tx Power Low Warning	dBm	-7.3
32-33	Rx Power High Alarm	dBm	2
34-35	Rx Power Low Alarm	dBm	-13.9
36-37	Rx Power High Warning	dBm	-1
38-39	Rx Power Low Warning	dBm	-9.9

Note.

- Alarm /Warming flag is linked to TxFault by default setting.
- Tx Bias Alarm/Warming is describing both prime and OSA source.
The parentheses value is second source case.

10. RoHS COMPLIANCY

Compliance versus requirements contained within the following reference document is guaranteed: 'DIRECTIVE 2011/65/EU OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (recast)'.

11. Qualification Testing

SPP5300SR-GL 10Gb/s transceiver is qualified to Sumitomo Electric Industries internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

12. Laser Safety Information

SPP5300SR-GL transceiver uses a semiconductor laser system that is classified as Class 1 laser products per the Laser Safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC60825-1:2007 and IEC60825-1:2001 International standards.

Caution

If this product is used under conditions not recommended in the specification or is used with unauthorized revision, the classification for laser product safety is invalid. Reclassify the product at your responsibility and take appropriate safety measures.

13. Electromagnetic Compatibility

EMI (Emission)

SPP5300SR-GL is designed to meet FCC Class B limits for emissions and noise immunity per CENELEC EN50 081 and 082 specifications.

RF Immunity

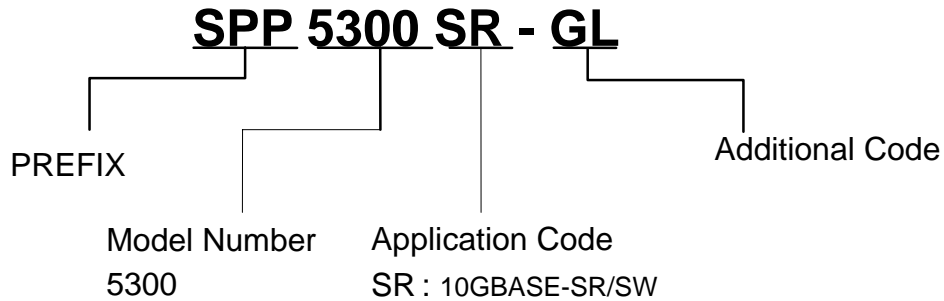
SPP5300SR-GL has an immunity to operate when tested in accordance with IEC 61000-4-3 (80- 1000MHz, Test Level 3) and GR-1089.

Electrostatic Discharge (ESD) Immunity

SPP5300SR-GL has an immunity against direct and indirect ESD when tested accordance with IEC 61000-4-2.

14. Ordering Information

14.1. Part Numbering System



14.2. Ordering Number Code

Table 13-1. SPP5300SR Application Code

P/N	Distance	Fiber	E/O	O/E	ITU-T G.691	Telecordia GR-253	IEEE 802.3ae
SPP5300SR-GL	300m	MMF	850nm VCSEL	PIN	-	-	10GBASE-SR/SW

14.3. Firmware version

This product contains the firmware inside. Sumitomo Electric may upgrade the firmware version without advance notice as far as such would be upper compatible. When customer should prefer to have the current firmware version, Sumitomo Electric will accommodate such request and will assign customized part number for this purpose.

14.4. 2-wire Serial Interface

If the serial clock(SCL) is more than 100kHz, the SCL is held in line low (clock stretching) during an 2-WIRE SERIAL INTERFACE read or write operation.

15. Label information



16. Contact Information

U.S.A.

Sumitomo Electric Device Innovations, U.S.A., Inc.

<West Coast (USA Headquarters)>

2355 Zanker Rd. San Jose, CA 95131-1138, USA

Tel: +1-408-232-9500

Fax: +1-408-428-9111

<East Coast>

4021 Stirrup Creek Drive, Suite 200, Durham, NC 27703, USA

Tel: +1-919-361-1600

Fax: +1-919-361-1619

Email: lw-info@sei-device.com, mw-info@sei-device.com

<http://www.sei-device.com/>

Europe

Sumitomo Electric Europe Ltd.

220 Centennial Park, Elstree, Herts, WD6 3SL UK

Tel: +44-208-953-8681

Fax: +44-208-207-5950

E-mail: photonics@sumielectric.com

<http://www.sumielectric.com>

Asia

Sumitomo Electrics Asia Ltd.

Photonics Department

Room 2624 - 2637, 26F., Sun Hung Kai Center, 30 Harbour Road, Wanchai, Hongkong.

Tel: +852-2576-0080

Fax: +852-2576-6412

Japan

Sumitomo Electric Industries, Ltd.

Device Sales Department

<Tokyo>

3-9-1, Shibaura, Minato-ku, Tokyo 108-8539, Japan

TEL +81-3-6722-3286

FAX +81-3-6722-3284

<Osaka>

4-5-33, Kitahama, Chuo-ku, Osaka 541-0041, Japan

Tel: +81-6-6220-4245

Fax: +81-6-6222-6231

E-mail: optoele-sales-pro-sml@list.sei.jp

<http://www.sei.co.jp/products/index.html>