10Gb/s XFP Optical Transceiver Module

SXP3104EX-M

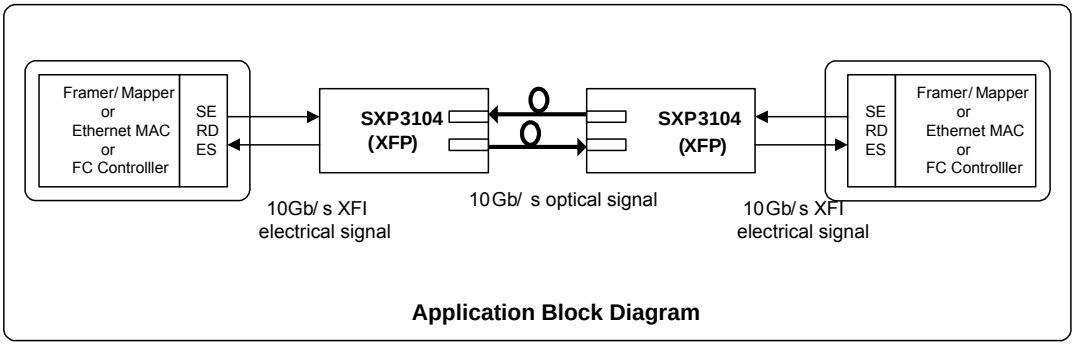
(10GBASE-ER/EW, 1550nm EML, PIN-PD)

Features

- 10Gb/s Serial Optical Interface
  - High quality and reliability optical device and sub-assemblies
  - 1550nm EML for up to 40km over single mode fiber
  - High sensitivity PIN photo diode and TIA
- XFP MSA Revision 4.5 Compliant
  - Easy supply management for hot pluggability
  - Duplex LC Receptacle
  - XFP Mechanical Interface with color coded bail latch for easy removal (Bail color: Red)
  - XFI High Speed Electrical Interface
  - 2-wire interface for management and diagnostic monitor
  - Tx_Disable and Rx_LOS functions
- Protocol
  - IEEE802.3ae 10 Gigabit Ethernet
- Extended Operating temperature range
  - Tc=-5 to 85degC
- Low Power Consumption
  - 3.3V and +5.0V power supply
- RoHS6 Compliant

Applications

- 10GE Etheswitches and routers
- 10GE Core-routers
- 10GE Storage
- Inter Rack Connection
- Other high speed data connections



Application Block Diagram

1. General Description

The SXP3104EX-M is a very compact 10Gb/s optical transceiver module for serial optical communication applications at 10Gb/s. The SXP3104EX-M converts a 10Gb/s serial electrical data stream to 10Gb/s optical output signal and a 10Gb/s optical input signal to 10Gb/s serial electrical data streams. The high speed 10Gb/s electrical interface is fully compliant with XFI specification.

The SXP3104EX-M is designed for Ethernet LAN (10.3Gb/s) and WAN (9.95Gb/s) applications. The high performance cooled 1550nm EML transmitter and high sensitivity PIN receiver provide superior performance for Ethernet applications at up to 40km links.

The fully XFP compliant form factor provides hot pluggability, easy optical port upgrades and low EMI emission.

2. Functional Description

The SXP3104EX-M contains a duplex LC connector for the optical interface and a 30-pin connector for the electrical interface. Figure 2.1. shows the functional block diagram of SXP3104EX-M XFP Transceiver.

Transmitter Operation

The transceiver module receives 10Gb/s electrical data and transmits the data as an optical signal. The transmitter contains a Clock Data Recovery (CDR) circuit that reduces the jitter of received signal and reshapes the electrical signal before the electrical to optical (E-O) conversion. The optical output power is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by Tx disable signal, TX_DIS pin. When TX_DIS is asserted high, transmitter is turned off.

Receiver Operation

The received optical signal is converted to serial electrical data signal. The optical receiver contains a CDR circuits that reshapes and retimes an electrical signal before sending out to the XFI channel (i.e. XFP connector and high speed signal traces).

The RX_LOS signal indicates insufficient optical power for reliable signal reception at the receiver.

Management Interface

A 2-wire interface (SCL, SDA) is used for serial ID, digital diagnostics and other control /monitor functions. The address of XFP transceiver is 1010000x. MOD_DESEL signal can be used in order to support multiple XFP modules on the same 2-wire interface bus.

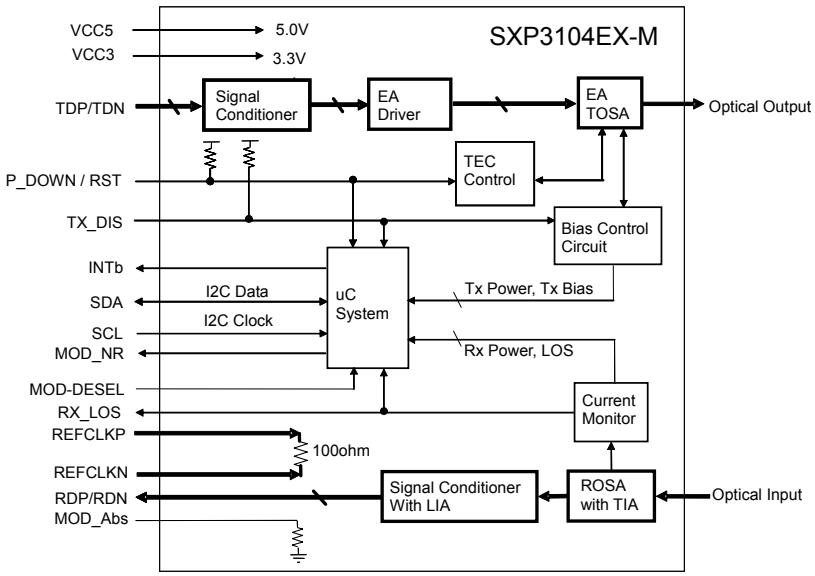
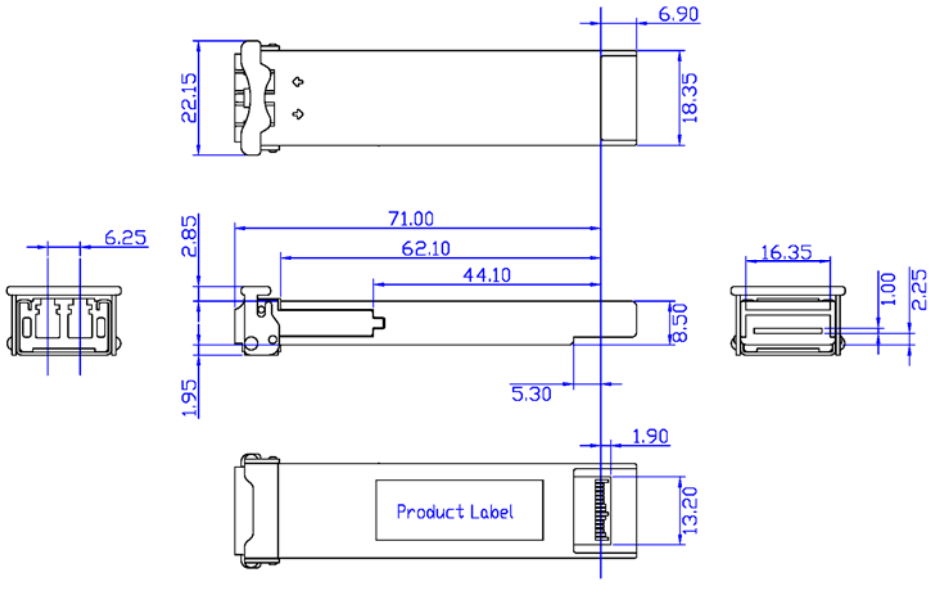


Figure 2.1. Functional Block Diagram

3. Package Dimensions

Figure 3.1. shows the package dimensions of SXP3104EX-M. SXP3104EX-M is designed to be complaint with XFP MSA specification. Package dimensions are specified in section 6.3 of the XFP MSA specification Rev. 4.5.



* Bail color is red. Unit : mm

Figure 3.1. Package dimensions

4. Pin Assignment and Pin Description

4.1. XFP Transceiver Electrical Pad Layout

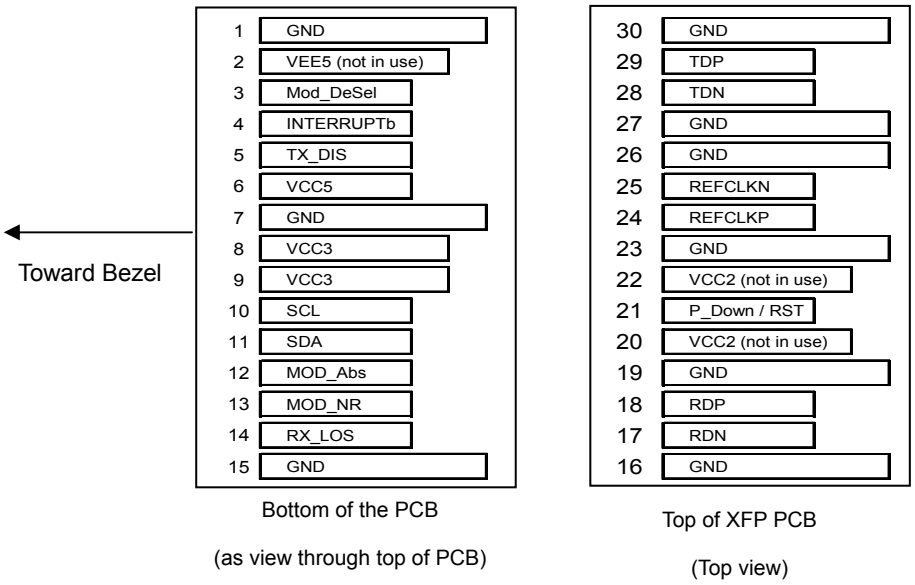


Figure 4.1. XFP Transceiver Electrical Pad Layout

4.2. Host PCB XFP Pinout

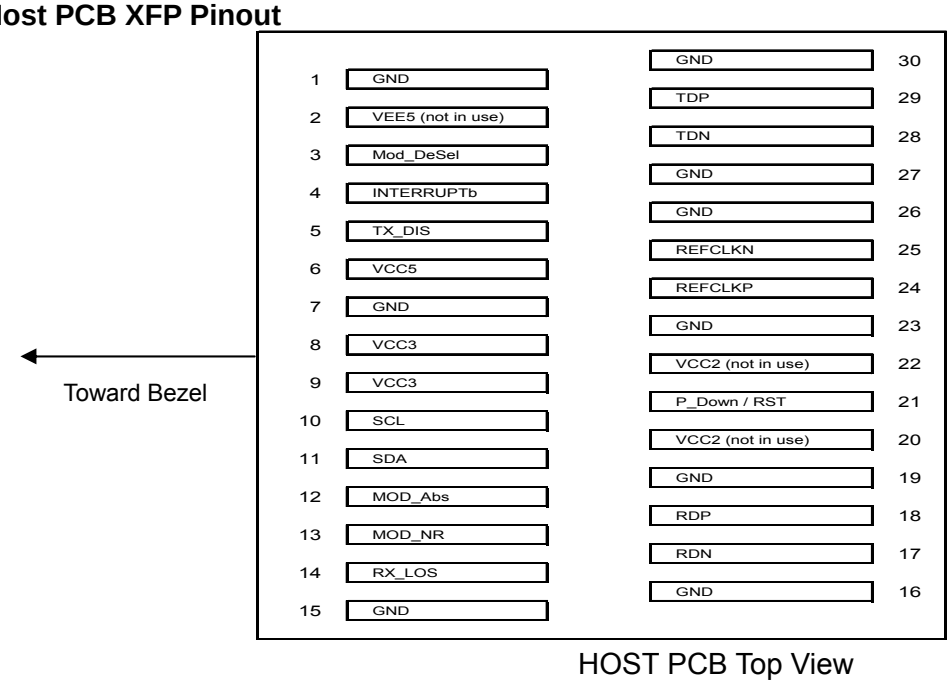


Figure 4.2. Host PCB XFP Pinout

4.3. Pin Descriptions

Table 4.3. Pin Description

Pin#	Name	Logic	Description	Note
1	GND	LVTTL-I	Module Ground	1
2	VEE5		-5.2V Power Supply; **not in use**	3
3	MOD_DeSel	LVTTL-I	Module De-select; When held Low allows module to respond to 2-wire serial interface	
4	INTERRUPTb	LVTTL-O	Indicates presence of an important condition, which can be read over the 2-wire serial interface. This pin is an open collector output and must be pulled up to host_Vcc on the host board.	2
5	TX_DIS	LVTTL-I	Transmitter Disable; When asserted High, transmitter output is turned off. This pin is pulled up to VCC3 in the module	
6	VCC5		+5V Power Supply,	
7	GND		Module Ground	1
8	VCC3		+3.3V Power Supply	
9	VCC3		+3.3V Power Supply	
10	SCL	I/O	2-wire serial interface clock. Host shall use a pull-up resistor connected to host_Vcc of +3.3V.	2
11	SDA	I/O	2-wire serial interface data. Host shall use a pull-up resistor connected to host_Vcc of +3.3V.	2
12	MOD_Abs	LVTTL-O	Indicates Module is not present. Host shall pull up this pin, and grounded in the module. "High" when the XFP module is absent from a host board.	2
13	MOD_NR	LVTTL-O	Module not ready; When High, Indicates Module Operational Fault. This pin is an open collector and must be pulled to host_Vcc on the host board.	2
14	RX_LOS	LVTTL-O	Receiver Loss of Signal; When high, indicates insufficient optical input power to the module. This pin is an open collector and must be pulled to host_Vcc on the host board.	2
15	GND		Module Ground	

Pin#	Name	Logic	Description	Note
16	GND		Module Ground	
17	RDN	CML-O	Receiver Inverted Data Output; AC coupled inside the module.	
18	RDP	CML-O	Receiver Non-Inverted Data Output; AC coupled in side the module.	
19	GND		Module Ground	1
20	VCC2		+1.8V Power Supply; **not in use**	3
21	P_Down/RST	LVTTL-I	Power down; When High, module is limited power mode. Low for normal operation. Reset; The falling edge indicates complete reset of the module. This pin is pulled up to VCC3 in the module.	
22	VCC2		+1.8V Power Supply; **not in use**	3
23	GND		Module Ground	1
24	REFCLKP	PECL-I	Reference clock Non-Inverted Input; **not in use** Internally terminated (100Ohm)	
25	REFCLKN	PECL-I	Reference clock Inverted Input; **not in use** Internally terminated (100Ohm)	
26	GND		Module Ground	1
27	GND		Module Ground	1
28	TDN	CML-I	Transmitter Inverted Data Input; AC coupled in side the module.	
29	TDP	CML-I	Transmitter Non-Inverted Data Input; AC coupled in side the module.	
30	GND		Module Ground	1

Note

1: Module ground pins are isolated from the module case and chassis ground within the module.

2: Shall be pulled up with 4.7k to 10k ohm to a voltage between 3.15V and 3.45V on the host board.

3: Not connected internally.

5. Absolute Maximum Ratings and Recommended Operating Conditions

Table 5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Strage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Supply Voltage	VCC5	-0.3	6.0	V	
Supply Voltage	VCC3	-0.5	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC3+0.5	V	
LVTTL Output Current	Iolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power (Average)	Mip	-	4	dBm	1

Note:
1: PIN Receiver.

Table 5.2. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	-5	85	degC	
Relative Humidity (non-condensing)	Rhop	-	85	%	
Power Supply Voltage	VCC5	4.75	5.25	V	
Power Supply Voltage	VCC3	3.135	3.465	V	
Power Supply Current	ICC5	-	500	mA	1
Power Supply Current	ICC3	-	750	mA	
Total Power Comsumption	Pd	-	3.5	W	

Note:

1: The inrush current is included.

6. Electrical Interface

6.1. High Speed Electrical Interface

XFI Application Reference model

Figure 6.1.1. shows the high speed electrical interface (XFI) compliance points.

XFI electrical interface is specified for each compliance point in the chapter 3 of the XFP MSA specification (Rev.4.5).

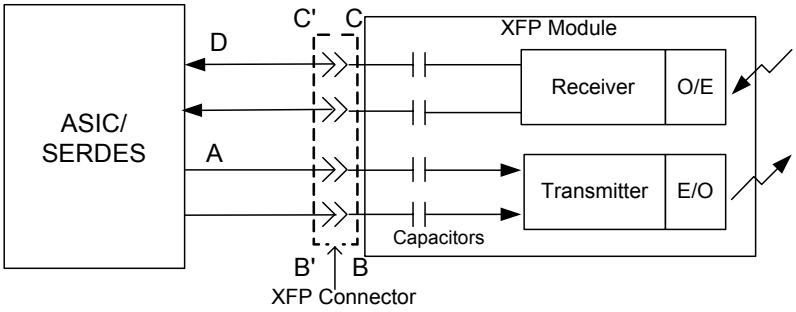


Figure 6.1.1. XFI Application Reference Model

XFI Module Transmitter Input Electrical Interface Specification at B'

Table 6.1.1. XFI Transmitter Input Electrical Specification at B'

Parameter -B'	symbol	Min	Typ	Max	Units	Note
Reference differential Input Impedance	Zd	-	100	-	Ohm	
Termination Mismatch	dZm	-		5	%	
Input AC Common mode Voltage		-		25	mV(RMS)	
Differential Input Return Loss	SDD11	20		-	dB	1
		8		-	dB	2
		See 3		-		3
Common Mode Input Return Loss	SCC11	3		-	dB	4
Differential to Common Mode Conversion	SCD11	10		-	dB	4
Total Input Non-DDJ Jitter	TJtnd	-		0.41	UIp-p	
Total Input Jitter	TJ	-		0.61	UIp-p	
Eye Mask	X1	-		0.305	UI	5
	Y1	60		-	mV	
	Y2	-		410	mV	

Note

1: 0.05 to 0.1 GHz

2: 0.1 to 5.5GHz

3: 5.5 to 12GHz, SDD11(dB)=8-20.66Log10(f/5.5), with f in GHz

4: 0.1 to 15GHz

5: Eye Mask is defined in Figure 6.1.2.

XFI Module Receiver Output Electrical Interface Specification at C'

Table 6.1.2. XFI Receiver Output Electrical Specification at C'

Parameter -C'	symbol	Min	Typ	Max	Units	Note
Reference differential Output Impedance	Zd	-	100	-	Ohm	
Termination Mismatch	dZm	-		5	%	
Output AC Common mode Voltage		-		15	mV(RMS)	
Output Rise and Fall time (20%-80%)	trh, tfh	24		-	ps	
Differential Output Return Loss	SDD22	20		-	dB	1
		8		-	dB	2
		See 3		-		3
Common Mode Input Return Loss	SCC22	3		-	dB	4
Determinstic Jitter	TJtnd	-		0.18	UIp-p	
Total Jitter	TJ	-		0.34	UIp-p	
Eye Mask	X1	-		0.17	UI	5
	X2	-		0.42	UI	
	Y1	170		-	mV	
	Y2	-		425	mV	

Note

1: 0.05 to 0.1 GHz

2: 0.1 to 5.5GHz

3: 5.5 to 12GHz, SDD11(dB)=8-20.66Log10(f/5.5), with f in GHz

4: 0.1 to 15GHz

5: Eye Mask is defined in Figure 6.1.3.

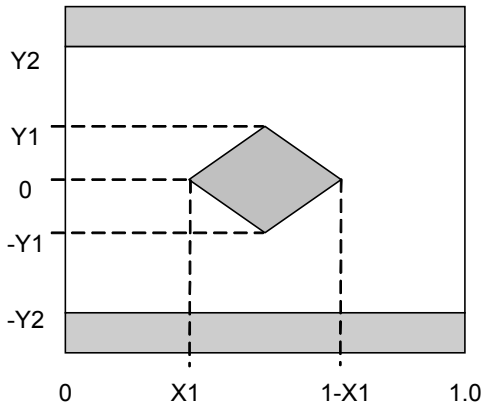


Figure 6.1.2.
Transmitter Input Eye Mask

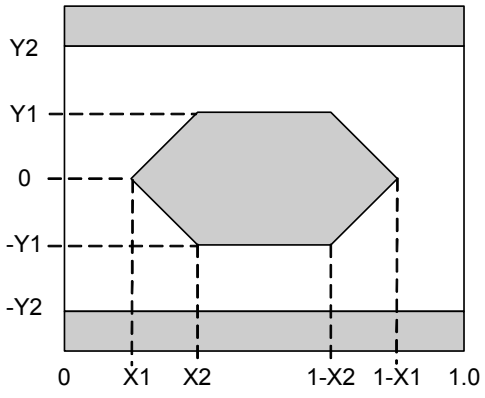


Figure 6.1.3.
Receiver Output Eye Mask

XFI Reference Clock Specification

Note that the reference clock is not needed for SXP3104EX-M. The differential reference clock signals if used are internally terminated across 100ohm as shown in Figure 2.1.

6.2. CDR Specification

Transmitter CDR

Table 6.2.1. Transmitter CDR Specification

Parameter	symbol	Min	Typ	Max	Units	Note
Jitter Transfer Bandwidth	BW	-		8	MHz	1
Jitter Transfer Peaking	Jp1	-		0.1	dB	2
	Jp2	-		1	dB	3

Note

1: In order to meet SONET/SDH jitter transfer requirement, de-jitter PLL will be needed on the host board SerDes.

2: Frequency ≤ 120kHz

3: Frequency ≥ 120kHz

Receiver CDR

Table 6.2.2. Receiver CDR specification

Parameter	symbol	Min	Typ	Max	Units	Note
Jitter Transfer Bandwidth	BW	-		12	MHz	
Jitter Transfer Peaking	Jp1	-		0.1	dB	1
	Jp2	-		1	dB	2

Note

1: Frequency ≤ 120kHz

2: Frequency ≥ 120kHz

6.3. Low Speed Electrical Interface

Table 6.3.1. Low Speed Control and Alarm Signals Electrical Interface

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
XFP Interrupt, Mod_NR, RX_LOS	Vol	0		0.4	V	1
	Voh	Vcc-0.5		Vcc+0.3		2
XFP TX_DIS, P_DOWN/RST	Vil	-0.3		0.8	V	3
	Vih	2		Vcc3+0.3		4
XFP SCL and SDA Output	Vol	0		0.4	V	1
	Voh	Vcc-0.5		Vcc+0.3		2
XFP SCL and SDA Input	Vil	-0.3		Vcc3*0.3	V	5
	Vih	Vcc3*0.7		Vcc3+0.5		6
Capacitance for XFP SCL and SDA I/O pin	Ci	-		14	pF	
Total bus capacitance load for SCL and SDA	Cb	-		100	pF	7
		-		400	pF	8

Note

1: Pull-up resistor must be connected to host_Vcc on the host board.
Iol(max)=3mA

2: Pull-up resistor must be connected to host_Vcc on the host board.

3: Pull-up resistor connected to VCC3 within XFP module. Iil(max)= -10μA.

4: Pull-up resistor connected to VCC3 within XFP module. Iih(max)= 10μA.

5: Pull-up resistor must be connected to host_Vcc on the host board.
Iol(max)= -10μA.

6: Pull-up resistor must be connected to host_Vcc on the host board.
Iol(max)= 10μA.

7: at 400KHz, 3.0kohms, at 100kHz 8.0kohms max.

8: at 400KHz, 0.8kohms, at 100kHz 2.0kohms max.

7. Optical Interface

Table 7.1. Optical Interface

Transmitter Optical Interface						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Note**
Operating Data Rate	-	9.95		10.31	Gb/s	1
Output Center Wavelength	ltc	1530		1565	nm	
SMSR	SMSR	30		-	dB	
Average Output Power	Po	-4.7		4.0	dBm	2
Disabled Power	Poff			-30	dBm	2
Extinction Ratio	ER	3.0		-	dB	3
Optical Modulation Amplitude	OMA	-1.7		-	dBm	
Transmitter and Dispersion Penalty	TDP	-		3.0	dB	3
OMA-TDP	OMAtdp	-2.1		-	dBm	
Optical Return Loss Tolerance	-			21	dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}	-	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}				4
$RIN_{21}OMA$	RIN			-128	dB/Hz	
Receiver Optical Interface						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Note**
Operating Data Rate	-	9.95		10.31	Gb/s	1
Input Center Wavelength	lrc	1260		1565	nm	
Overload	Rovl	-1.0		-	dBm	
Sensitivity in OMA	OMA0	-		-14.1	dBm	3
Stressed Sensitivity in OMA	OMAst	-		-11.3	dBm	
RX_LOS Assert Level	RLOSa	-30		-25	dBm	
RX_LOS Deassert Level	RLOSd	-		-22	dBm	
RX_LOS Hysteresis	RLOSh	1		5	dB	
Optical Return Loss	ORL	-		-26	dB	

Note1: Data rate tolerance 10GBASE-ER : typ.+/-100ppm
Note2: Measured at 9.95328Gbps, Framed PRBS2^31-1, NRZ
Note3: Measured at 10.3125Gbps, Non-framed PRBS2^31-1, NRZ
Note4: Refer to Fig.7.1.

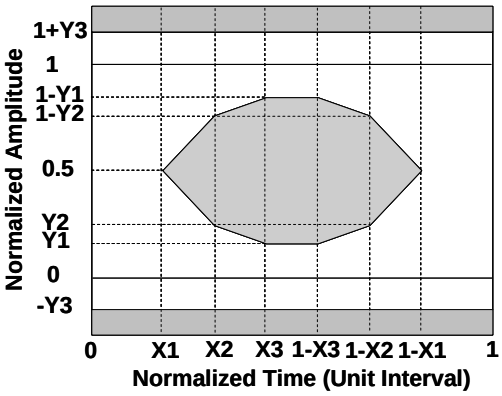


Figure.7.1. Transmission eye mask definition

8. Electrical and Optical I/O Signal Relationship

Table.8.1. TX_DIS vs. Optical Output Power

TX_DIS	Optical Output Power
Low (V_{IL}=-0.3 to 0.8V)	Enabled
High (V_{IH} =2.0 to VCC3+0.3V)	Disabled (<-30dBm)

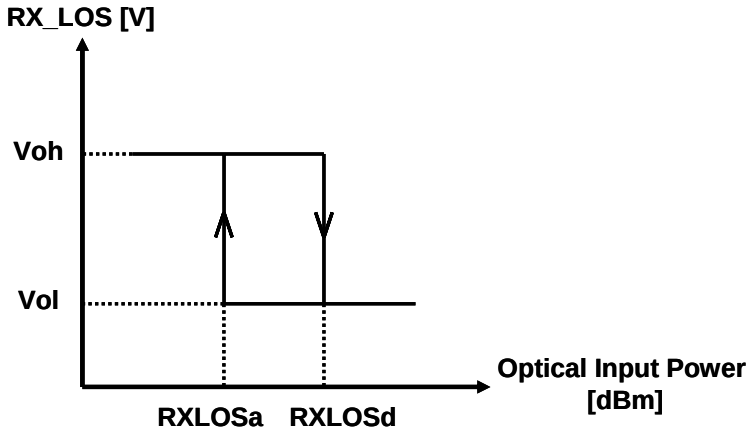


Figure.8.1. Optical Input Power vs. RX_LOS

9. User Interface

9.1. XFP Mechanical Interface

XFP Mechanical Interface is specified in the chapter 6 in the XFP MSA specification.

XFP Mechanical Components

Figure 9.1.1. shows the XFP transceiver concept and mechanical components.

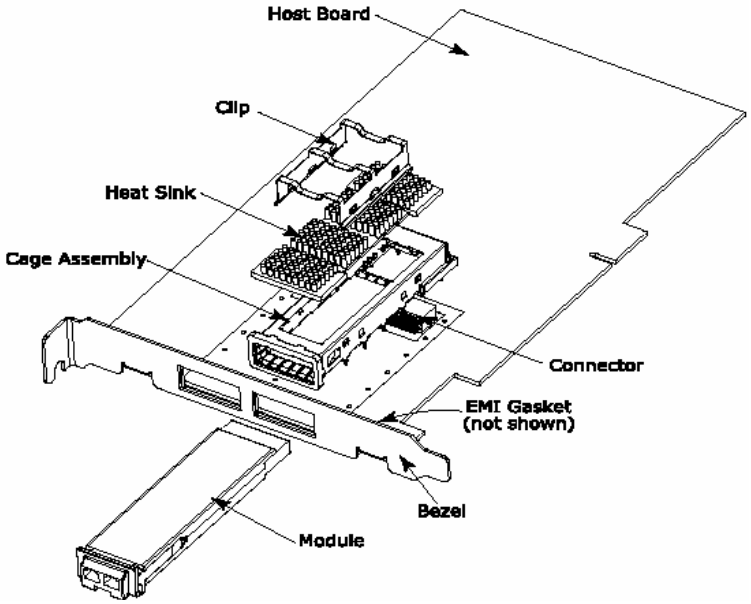


Figure 9.1.1. XFP Mechanical Interface Concept and Components

XFP Host board Mechanical Layout

XFP Host Board Layout is specified in the Figure 35 of the XFP MSA specification (Rev. 4.5).

Host Board XFP Connector Footprint and Layout

Host board XFP connector layout is specified in the Figure 36 of the XFP MSA Specification (Rev. 4.5).

XFP Datum Alignment and Bezel Design

XFP datum alignment (depth) is specified in the Figure 30 of the XFP MSA specification (Rev. 4.5).

The recommended bezel design is specified in the Figure 37 of the XFP MSA specification (Rev. 4.5).

XFP Connector and XFP Cage Assembly

The XFP 30-contact connector mechanical specification is shown in Figure 39 of the XFP MSA specification (Rev. 4.5)

The XFP Cage Assembly mechanical specification is shown in the Figure 41 of the XFP MSA specification (Rev. 4.5).

9.2. Management Interface

XFP 2-Wire Serial Interface Protocol

XFP 2-wire serial interface is specified in the Chapter 4 of the XFP MSA specification.

The XFP 2-wire serial interface is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all XFP modules.

The 2-wire serial interface address of the XFP module is 1010000X(A0h). In order to access to multiple modules on the same 2-wire serial bus, the XFP has a MOD_DESEL (module deselect pin). This pin (which is pull high or deselected in the module) must be held low by the host to select of interest and allow communication over 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

XFP Management Interface

XFP Managed interface is specified in the Chapter 5 of the XFP MSA specification.

The Figure 9.2.2. shows the structure of the memory map. The normal 256 Byte address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Byte is always directly available and is used for the diagnostics and control functions that must be accessed repeatedly. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. The upper address space tables are used for less frequently accessed functions and control space for future standards definition.

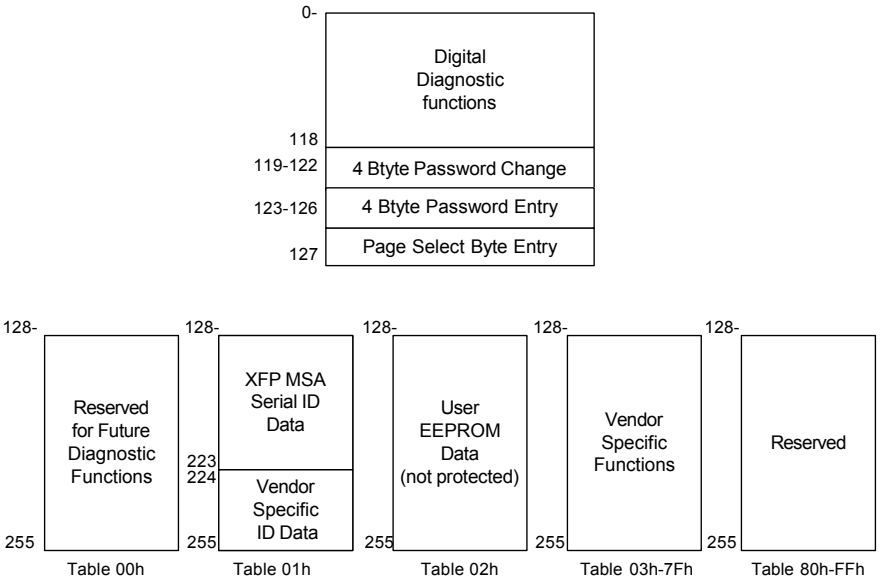


Figure 9.2. 2-wire Serial Interface Memory Map

9.3. A/D Accuracy and Values

Table 9.3.1. A/D Accuracy

Data Address	Parameter	Accuracy	Relative accuracy	Units Display	Note
96-97	Temperature	+/-3degC	NA	Signed 2's complement integer degC	Junction temperature of monitoring IC.
98-99	Reserved				
100-101	Tx Bias	+/-10%	NA	×2μA	Specified by nominal value
102-103	Tx Power	+/-2dB@BOL (Note1) (Range: -1 to +2dBm)	+/-1dB (Note2)	×0.1μW	Average Power
104-105	Rx Power	+/-2dB@BOL (Note1) (Range: -16 to +2dBm)	+/-1dB (Note2)	×0.1μW	At specified transmitter wavelength.
106-107	Vcc3	+/-3%	NA	×100μV	3.3V Only

Table 9.3.2. A/D Values

Byte	Bit	Name	Description
96	All	Temperature MSB	Signed 2's complement integer temperature (-40 to +125degC) based on internal temperature measurement
97	All	Temperature LSB	Fractional part of temperature(count/256)
98-99	All		Reserved
100	All	Tx Bias MSB	Measured Laser Bias Current in mA. Bias current is full 16 bit value *2μA. (Full range of 0 to 131mA)
101	All	Tx Bias LSB	
102	All	Tx Power MSB	Measured Tx output power in mW. Tx power is full 16 bit value *0.1μW. (Full range of -40 to +8.2dBm)
103	All	Tx Power LSB	
104	All	Rx Power MSB	Measured Rx input power in mW. Tx power is full 16 bit value *0.1μW. (Full range of -40 to +8.2dBm)
105	All	Rx Power LSB	
106	All	Vcc3 MSB	Internally measured transceiver supply voltage. Vcc is full 16 bit value*100μV. (Full range of 0 to +6.55 Volts)
107	All	Vcc3 LSB	
108	All	AUX 2 MSB	TBD
109	All	AUX 2 LSB	

Note1. Over specified temperature and voltage.

Note2. Over specified temperature and voltage range over the life of the product into a fixed measurement system.

9.4. Serial ID Memory Map (Data Field – Page 01h)

Address	Name of Field	Dec	Hex	ASCII	Description of Field
128	Identifier	6	06		XFP
129	Extended Identifier	144	90		Level 3(3.5W), with CDR, TX Ref CLK not required, No CLEI in Table 02h
130	Connector	7	07		LC
131	Transceiver	34	22		10GBASE-ER, 10GBASE-EW
132		0	00		
133		0	00		
134		0	00		
135		0	00		
136		0	00		
137		0	00		
138		0	00		
139	Encoding	144	90		64B/66B, NRZ
140	BR, Nominal	100	64		9953Mbps
141	BR, Maximum	103	67		10312.5Mbps
142	Length(SMF)-km	40	28		40km
143	Length(E-50um)	0	0		
144	Length(50um)	0	0		
145	Length(62.5um)	0	0		
146	Length(Copper)	0	0		
147	Device Technology	116	74		1550nm EML, No wavelength control, Cooled TX, PIN, Non-tunable TX
148	Vendor name	83	53	S	
149		117	75	u	
150		109	6D	m	
151		105	69	i	
152		116	74	t	
153		111	6F	o	
154		109	6D	m	
155		111	6F	o	
156		69	45	E	
157		108	6C	l	
158		101	65	e	
159		99	63	c	
160		116	74	t	
161		114	72	r	
162		105	69	i	
163		99	63	c	
164	CDR Support	240	F0		CDR Support for 9.95Gbps, 10.3Gbps, 10.5Gbps, 10.7Gbps
165	Vendor OUI	0	0		
166		0	0		
167		95	5F		
168	Vendor PN	83	53	S	
169		88	58	X	
170		80	50	P	
171		51	33	3	
172		49	31	1	
173		48	30	0	
174		52	34	4	
175		69	45	E	
176		88	58	X	
177		45	2D	-	
178		77	4D	M	
179		32	20		
180		32	20		
181		32	20		
182		32	20		
183		32	20		
184	Vendor rev	65	41	A	
185		32	20		
186	Wavelength	120	78		1547.5[nm]
187		230	E6		
188	Wavelength Tolerance	13	0D		17.5[nm]
189		172	AC		
190	Maximum Case Temperature	85	55		85[degC]
191	CC_BASE	212	D4		Check code from byte 128x to byte 190x

Address	Name of Field	Dec	Hex	ASCII	Description of Field
192	Power Supply	175	AF		3.5[W]
193		150	96		1.5[W]
194		168	A8		Max current; 500[mA] for +5V, 750[mA] for +3.3V
195		0	00		Max current; 0[mA] for +1.8V, 0[mA] for -5.2V
196	Vendor SN				
197					
198					
199					
200					
201					
202					
203					
204					
205					
206					
207					
208					
209					
210					
211					
212	Date Code and Lot code				Year
213					
214					Month
215					
216					Day
217					
218					Lot Code
219					
220	Diagnostic Monitoring Type	8	08		No BER Support, Average Power
221	Enhanced Options	96	60		soft TX_DISABLE, soft P_down
222	AUX Monitoring	118	76		+3.3V Supply Voltage for AUX1, +5V Supply Voltage for AUX2
223	CC_EXT				Check code from byte 192x to byte 222x
224	Vendor Specific	255	FF		
225		255	FF		
226		255	FF		
227		255	FF		
228		255	FF		
229		255	FF		
230		255	FF		
231		255	FF		
232		255	FF		
233		255	FF		
234		255	FF		
235		255	FF		
236		255	FF		
237		255	FF		
238		255	FF		
239		255	FF		
240		255	FF		
241		255	FF		
242		255	FF		
243		255	FF		
244		255	FF		
245		255	FF		
246		255	FF		
247		255	FF		
248		255	FF		
249		255	FF		
250		255	FF		
251		255	FF		
252		255	FF		
253		255	FF		
254		255	FF		
255		255	FF		

9.5. Alarm and warning threshold (Lower Table memory map)

Address	Name of Field	Dec	Hex	ASCII	Description of Field
2	Temperature High Alarm	95	5F		95[degC]
3		0	00		
4	Temperature Low Alarm	241	F1		-15[degC]
5		0	00		
6	Temperature High Warning	90	5A		90[degC]
7		0	00		
8	Temperature Low Warning	246	F6		-10[degC]
9		0	00		
10	Reserved A/D Flag Thresholds	0	00		
11		0	00		
12	Reserved A/D Flag Thresholds	0	00		
13		0	00		
14	Reserved A/D Flag Thresholds	0	00		
15		0	00		
16	Reserved A/D Flag Thresholds	0	00		
17		0	00		
18	Bias High Alarm	253	FD		130[mA]
19		232	E8		
20	Bias Low Alarm	0	00		0[mA]
21		0	00		
22	Bias High Warning	234	EA		120[mA]
23		96	60		
24	Bias Low Warning	0	00		0[mA]
25		0	00		
26	TX Power High Alarm	123	7B		5[dBm]
27		134	86		
28	TX Power Low Alarm	15	0F		-4[dBm]
29		141	8D		
30	TX Power High Warning	77	4D		3[dBm]
31		240	F0		
32	TX Power Low Warning	24	18		-2[dBm]
33		165	A5		
34	RX Power High Alarm	87	57		3.5[dBm]
35		115	73		
36	RX Power Low Alarm	0	00		-100[dBm]
37		0	00		
38	RX Power High Warning	55	37		1.5[dBm]
39		45	2D		
40	RX Power Low Warning	1	01		-15[dBm]
41		60	3C		
42	AUX 1(VCC3.3V) High Alarm	141	8D		3.63[V]
43		204	CC		
44	AUX 1(VCC3.3V) Low Alarm	116	74		2.97[V]
45		4	04		
46	AUX 1(VCC3.3V) High Warning	135	87		3.465[V]
47		90	5A		
48	AUX 1(VCC3.3V) Low Warning	122	7A		3.135[V]
49		118	76		
50	AUX 2(VCC5V) High Alarm	214	D6		5.5[V]
51		216	D8		
52	AUX 2(VCC5V) Low Alarm	175	AF		4.5[V]
53		200	C8		
54	AUX 2(VCC5V) High Warning	205	CD		5.25[V]
55		20	14		
56	AUX 2(VCC5V) Low Warning	185	B9		4.75[V]
57		140	8C		

9.6. Supply filter

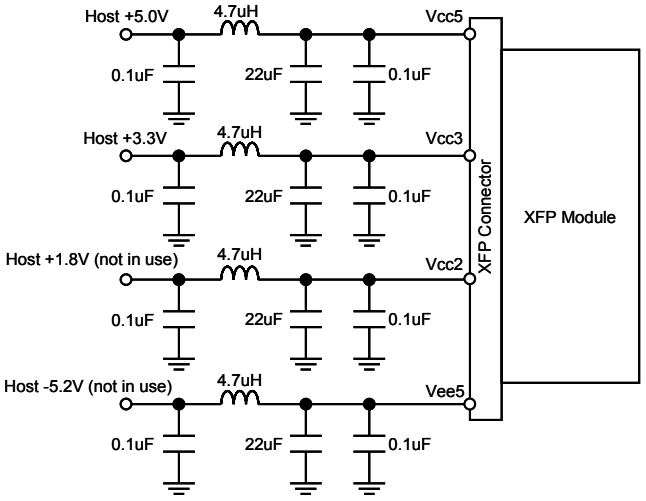


Figure 9.6. Supply Filter

9.7. Recommended Electrical Interface

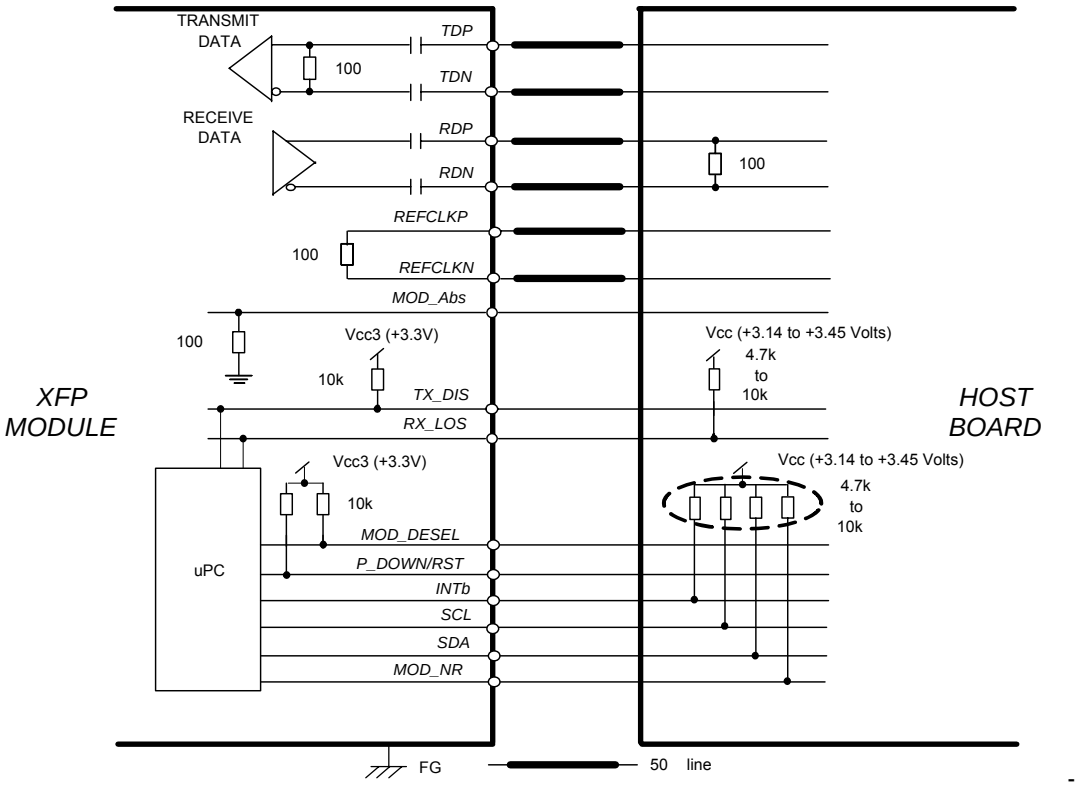


Figure 9.7. Recommended Electrical Interface

10. Qualification Testing

SXP3104EX-M 10Gb/s transceiver is qualified to Sumitomo Electric Industries internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

11. Laser Safety Information

SXP3104EX-M OC-192 transceiver uses a semiconductor laser system that is classified as Class 1 laser products per the Laser Safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC60825-1:2007 and IEC60825-1:2001 International standards.

Caution

If this product is used under conditions not recommended in the specification or is used with unauthorized revision, the classification for laser product safety is invalid. Reclassify the product at your responsibility and take appropriate safety measures.

12. Electromagnetic Compatibility (Pending)

EMI (Emission)

SXP3104EX-M is designed to meet FCC Class B limits for emissions and noise immunity per CENELEC EN50 081 and 082 specifications.

RF Immunity

SXP3104EX-M has an immunity to operate when tested in accordance with IEC 61000-4-3 (80- 1000MHz, Test Level 3) and GR-1089.

Electrostatic Discharge (ESD) Immunity

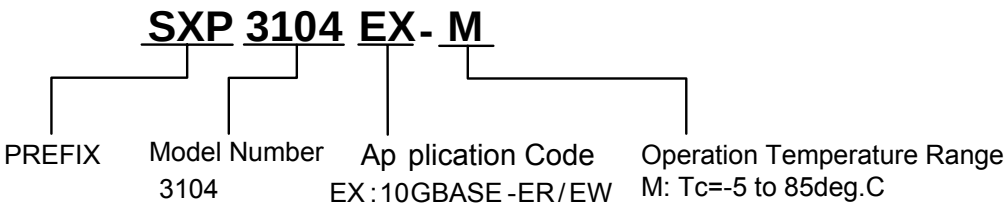
SXP3104EX-M has an immunity against direct and indirect ESD when tested accordance with IEC 61000-4-2.

13. RoHS COMPLIANCY

Compliance versus requirements contained within the following reference document is guaranteed: 'DIRECTIVE 2011/65/EU OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (recast)'.

14. Ordering Information

14.1. Part Numbering System



14.2. Evaluation Board Kit

For test purposes, Evaluation Board model number SK3101A and SP3101A may be ordered to use with the SXP3104 Series transceivers.

SK3101A : SXP3104 XFP evaluation board

SP3101A : XFP 2-wire serial interface evaluation kit

14.3. Ordering Number Code

Table 13. SXP3104 Application Code

P/N	Distance	Fiber	E/O	O/E	ITU-T G691	Telecordia GR-253	IEEE 802.3ae
SXP3104EX-M	40km	STD-SMF	1.55um EML	PIN	-	-	10GBASE-ER/EW

14.4. Firmware version

This product contains the firmware inside. Sumitomo Electric may upgrade the firmware version without advance notice as far as such would be upper compatible. When customer should prefer to have the current firmware version, Sumitomo Electric will accommodate such request and will assign customized part number for this purpose.

14.5. I2C Interface

If the serial clock(SCL) is more than 100kHz, the SCL is held in line lpw(clock stretching) during an I2C read or white operation.

15. Label Information

(Bottom Label)

(Case Label)

16. Contact Information

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