nRF2460

2.4 GHz wireless mono audio streamer

Product Specification v1.0

Features

- World-wide 2.4 GHz ISM band operation
- 6x6 mm 36 pin QFN package
- 4 Mbps on-air data rate
- Mono 32 kHz audio rate
- 16 bit resolution
- I2S interface for audio support
- SPI or 2-wire interface to transfer bi-directional control data
- On-chip voltage regulators
- Few external components
- Programmable latency
- Quality of Service engine
- Option to synchronize two pairs of audio receivers

Applications

- Wireless microphone
- Subwoofer

2011-6-28

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Datasheet status	
Objective Product Specification	This product specification contains target specifications for product development.
Preliminary Product Specification	This product specification contains preliminary data, supplementary data may be published from Nordic Semiconductor ASA later.
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Revision History

Date	Version	Description
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Contents

1 Introduction

The nRF2460 provides a solution for mono 16 bit 32 kHz LPCM audio streaming. The I2S interface is supported for audio- input or output. The device features seamless interfacing of low cost A/D and D/A for analog audio input and output. An external microcontroller controls the nRF2460 through a slave SPI or 2-wire (I2C compatible) control interface.

1.1 Prerequisites

In order to fully understand this product specification, a good knowledge of electronic- and software engineering is necessary.

1.2 Writing Conventions

This document follows a set of typographic rules to make the document consistent and easy to read. The following writing conventions are used:

- Pin names are written in **`Courier New bold.`**
- Commands, bit state conditions, and register names are written in `Courier New`.
- File names and User Interface components are written in regular **bold**.
- Cross references are underlined and highlighted in blue.

2 Product overview

The nRF2460 is a 4 Mbps single-chip RF transceiver that operates in the worldwide, 2.4 GHz license-free ISM band. The nRF2460 is based on the ShockBurst™ link layer from Nordic Semiconductor.

2.1 Features

The device offers a wireless channel for seamless streaming of mono LPCM in parallel with a low, data rate control channel. To enable this, the device has the following features:

- Standard digital audio interface (I2S)
- SPI or 2-wire slave control interfaces
- Fully embedded Quality of Service engine handling all RF protocol and RF link tasks

As all processing related to audio I/O, RF protocol, and RF link management are embedded, the device offers a transparent audio channel with a capacity of 512 kbits, with no true time processing needed. The nRF2460 is used in conjunction with a microcontroller that only needs to handle low speed tasks through the control interface (for example: volume up/down).

2.2 Block diagram

Figure 1. is a block schematic of a typical nRF2460 based system.

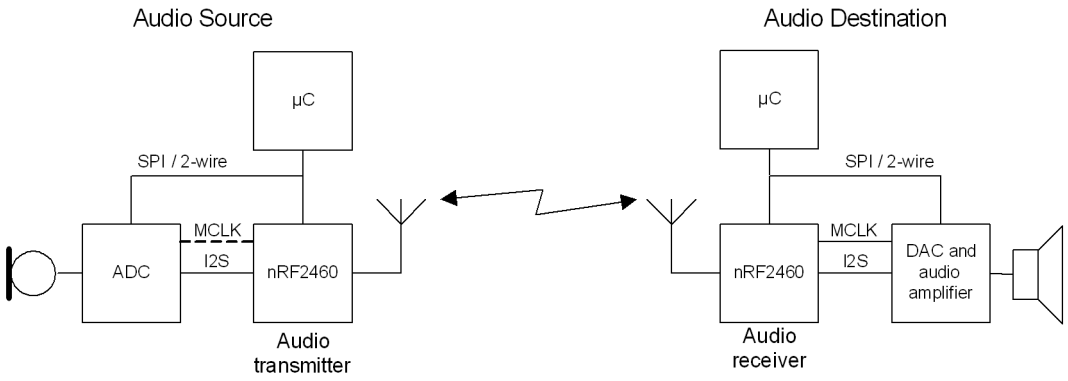


Figure 1. Typical audio application using nRF2460

In this system a microphone is connected to an nRF2460 by way of an ADC using standard audio format (I2S). An nRF2460 pair transfers audio data from the source and presents it to a DAC on the receiving side. Application-wise, the nRF2460 link will appear as a transparent channel (like a cable).

Initial configuration of nRF2460 is done by the microcontroller through an SPI or 2-wire control interface. The microcontrollers on both sides are also able to monitor link status and turn the link on and off. When a link is established, there is also a low data-rate reliable control link between the two microcontrollers.

2.2.1 Pin assignments

Table 1. on page 10 shows the nRF2460 pin functions. Note that pin functions depend on the operational mode of the device and the slave interface of choice.

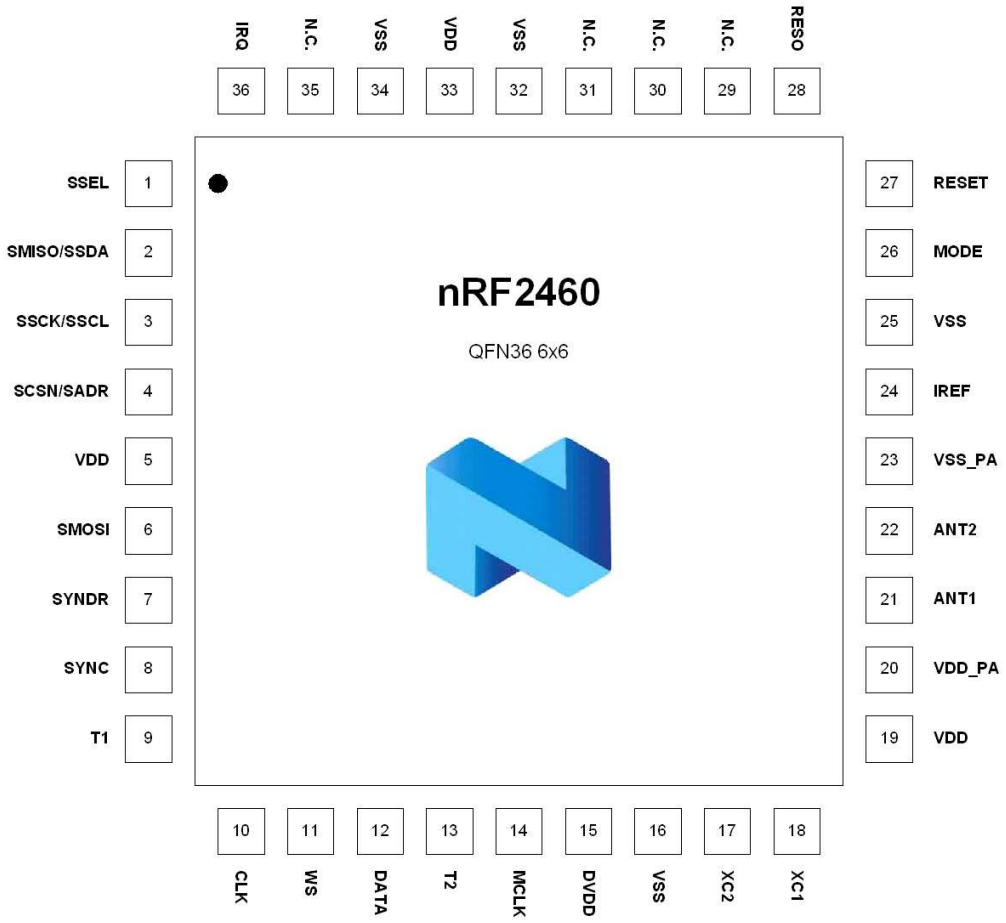


Figure 2. Pin assignment nRF2460

2.3 Pin functions

The nRF2460 can be set up as either an audio transmitter (ATX) or audio receiver (ARX), controlled by the logic level of the **MODE** pin.

Serial slave interface is controlled by the logic level of the **SSEL** pin. See Table 1. on page 10.

Pin no.	Pin name	Pin function	Description
1	SSEL	Digital input	Slave interface select 0: SPI, 1:2-wire
2	SMISO SSDA	Digital output Digital I/O	Slave SPI serial out (SSEL=0) Slave 2-wire data (SSEL=1)
3	SSCK SSCL	Digital input Digital I/O	Slave SPI clock (SSEL=0) Slave 2-wire clock (SSEL=1)
4	SCSN SADR	Digital input Digital input	Slave SPI slave select (SSEL=0) Address select 2-wire slave (SSEL=1)
5	VDD	Power	Power supply
6	SMOSI	Digital input	Slave serial in (SSEL=0) Connect to ground (0V) (SSEL=1)
7[1]	SYNDR	Digital input	Select SYNC direction 0: Output, 1: Input
8	SYNC	Digital output Digital input	No synchronization (default) SYNDR=0 Optional signal to synchronize 2 ARX (SYNDR=1)
9	T1	Digital input	Reserved, connect to ground (0V)
10	CLK	Digital I/O Digital output	I2S bit clock (MODE=1) I2S bit clock (MODE=0)
11	WS	Digital I/O Digital output	I2S word clock (MODE=1) I2S word clock (MODE=0)
12	DATA	Digital input Digital output	I2S data signal (MODE=1) I2S data signal (MODE=0)
13	T2	Digital Input	Reserved, connect to ground(0V)
14	MCLK	Digital Output	256X sample rate clock to ADC or DAC
15	DVDD	Regulator output	Internal voltage regulator output for decoupling
16	VSS	Power	Ground (0V)
17	XC2	Analog output	Crystal connection for 16 MHz crystal oscillator
18	XC1	Analog input	Crystal connection for 16 MHz crystal oscillator
19	VDD	Power	Power supply
20	VDD_PA	Regulator output	Power supply output (+1.8V) for on-chip RF Power amplifier
21	ANT1	RF	Differential antenna connection (TX and RX)

Pin no.	Pin name	Pin function	Description
22	ANT2	RF	Differential antenna connection (TX and RX)
23	VSS_PA	Power	Ground (0V)
24	IREF	Analog output	Device reference current output. To be connected to reference resistor on PCB
25	VSS	Power	Ground (0V)
26	MODE	Digital Input	Mode 1:audio transmitter (ATX), 0:audio receiver (ARX)
27	RESET	Digital Input	Active high reset, connect to ground(0V) if not used
28	RESO	Digital Output	Optional RESET pulse for ADC
29	NC	Digital Output	Reserved, leave unconnected
30	NC	Digital Input	Reserved, connect to ground(0V)
31	NC	Digital Output	Reserved, leave unconnected
32	VSS	Power	Ground (0V)
33	VDD	Power	Power Supply
34	VSS	Power	Ground (0V)
35	NC	Digital Output	Reserved, leave unconnected
36	IRQ	Digital Output	Interrupt request

1. Must be connected to ground (0V) if synchronization is not required.

Table 1. nRF2460 pin functions

2.3.1 Modes of operation

A wireless system streaming audio will have an asymmetrical load on the RF link as audio data is fed from an audio source (as in a microphone) to a destination (as in loud speakers). From the destination back to the audio source, only service- and control communication are needed.

The nRF2460 is used both on the audio source side (for example in a microphone) transmitting audio data, and on the destination side (for example in a loudspeaker) receiving audio data.

Due to the asymmetry, nRF2460 has two operational modes set by the external pin **MODE**, depending on whether it represents the transmitter or the receiver. The two modes show significant differences both in internal and I/O functionality. The operational mode is selected by the logic level on the **MODE** pin:

MODE	Description
0	Audio destination
1	Audio source

*Table 2. Operation modes set by **MODE** pin*

The **MODE** pin is read during power-up and reset only.

In this context, the abbreviations ATX (for audio transmitter) and ARX (for audio receiver) refer to the directional flow of the audio, while the nRF2460 radio transceiver always operates in half-duplex (bi-directional) mode.

2.3.2 Communication and data transfer principle

To differentiate between audio data and other control and status information, we have organized the information about the data traffic between the ATX/ARX in this document, into two data channels.

The audio channel is defined as the communication channel sourcing audio data from the ATX to the ARX. The audio data is divided into two categories; real time data from the audio source and retransmitted audio information.

If there is audio information lost, the ARX requests re-transmission of the lost packets. The real-time audio bit rate is constant, whereas the amount of retransmitted audio varies across time.

The control channel is a two-way, low data rate channel superimposed on the audio stream.

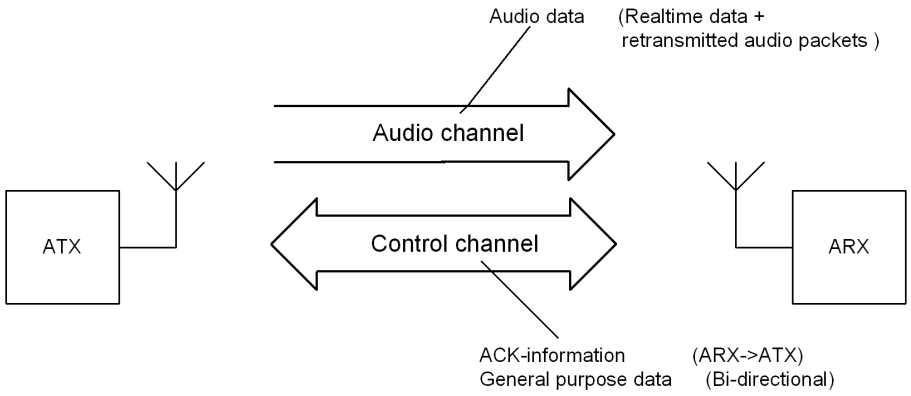


Figure 3. nRF2460 communication channel concept

2.3.3 Mode- and interface alternatives

A number of interfaces are available for the nRF2460 device. The available interfaces depend on the nRF2460 mode of operation and the type of data to be transferred. Data is divided into two categories; audio data (audio channel) and configuration/status data (control channel). Figure 4. illustrates the available data interfaces for the various modes of operation. Interface options are illustrated by grey circles, whilst functionality / operation modes are shown in white. Relevant configuration settings are shown in the lines drawn between the circles.

Note: A choice about interface is made by a combination of pin and register settings. Refer to Chapter 4 on page 21 for details.

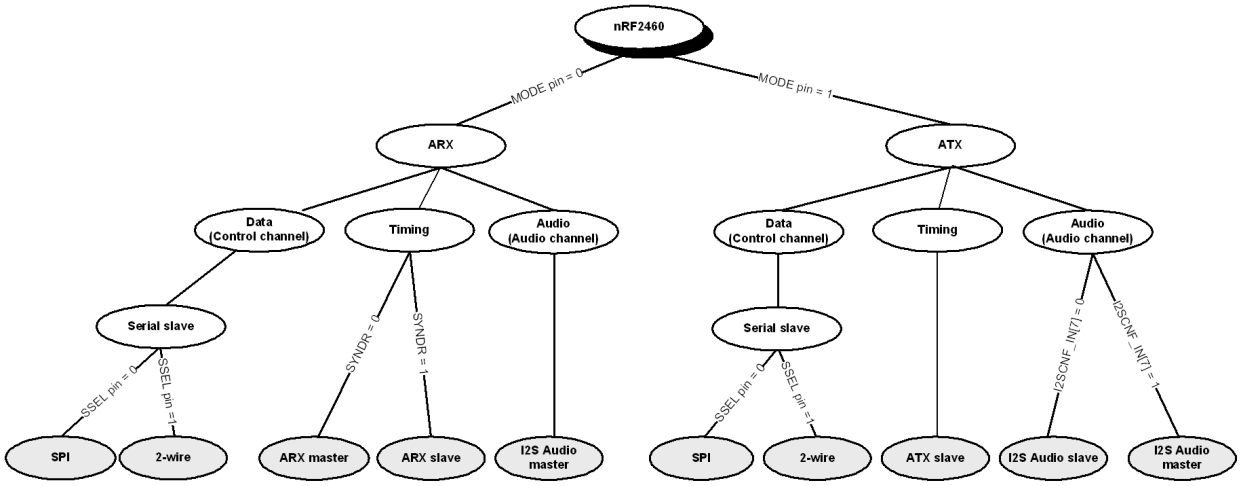


Figure 4. nRF2460 functional modes and interface alternatives

2.3.4 Audio transmitter (ATX)

When an nRF2460 is applied at the audio source side of the RF link, the **MODE** pin must be set high and nRF2460 will become an audio transmitter. The block schematic of nRF2460 in ATX mode can be seen in Figure 5.

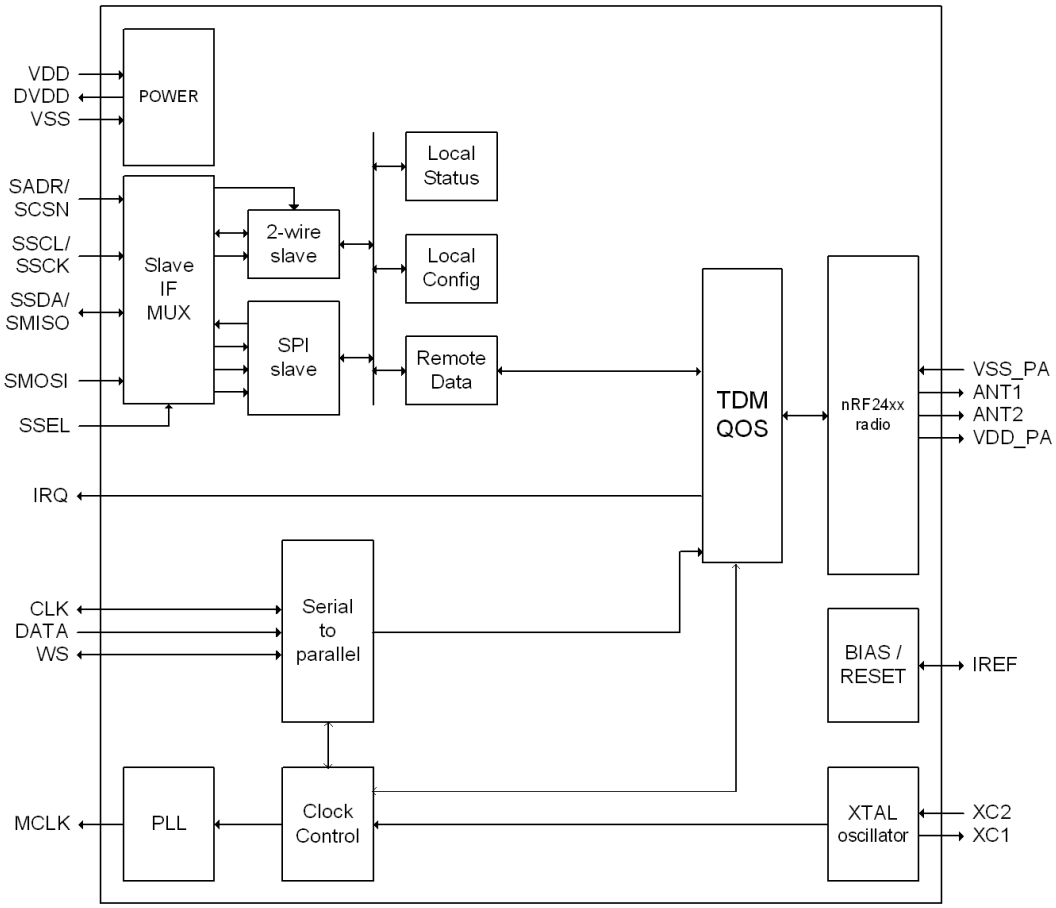


Figure 5. nRF2460 ATX mode block diagram

2.3.4.1 I2S audio input

I2S is the audio interface to the nRF2460. The I2S interface consists of pins **CLK**, **DATA** and **WS**. This interface supports a sampling rate of 32 kHz.

I2S may be used with an external stereo or mono ADC for analog audio sources. The nRF2460 offers a sampling rate clock (f_S) of 256 times the audio sampling rate. The sample rate clock is available on the **MCLK** pin and may be used as system clock for the ADC. Only mono 32 kHz audio is streamed from ATX to ARX. Data is in a 16-bit format.

2.3.5 Audio Receiver (ARX)

When nRF2460 is put at the destination side of the RF link, MODE must be low and nRF2460 becomes the audio receiver (ARX). A block schematic of nRF2460 in ARX mode can be seen in Figure 6. I2S is now used for audio real time data output.

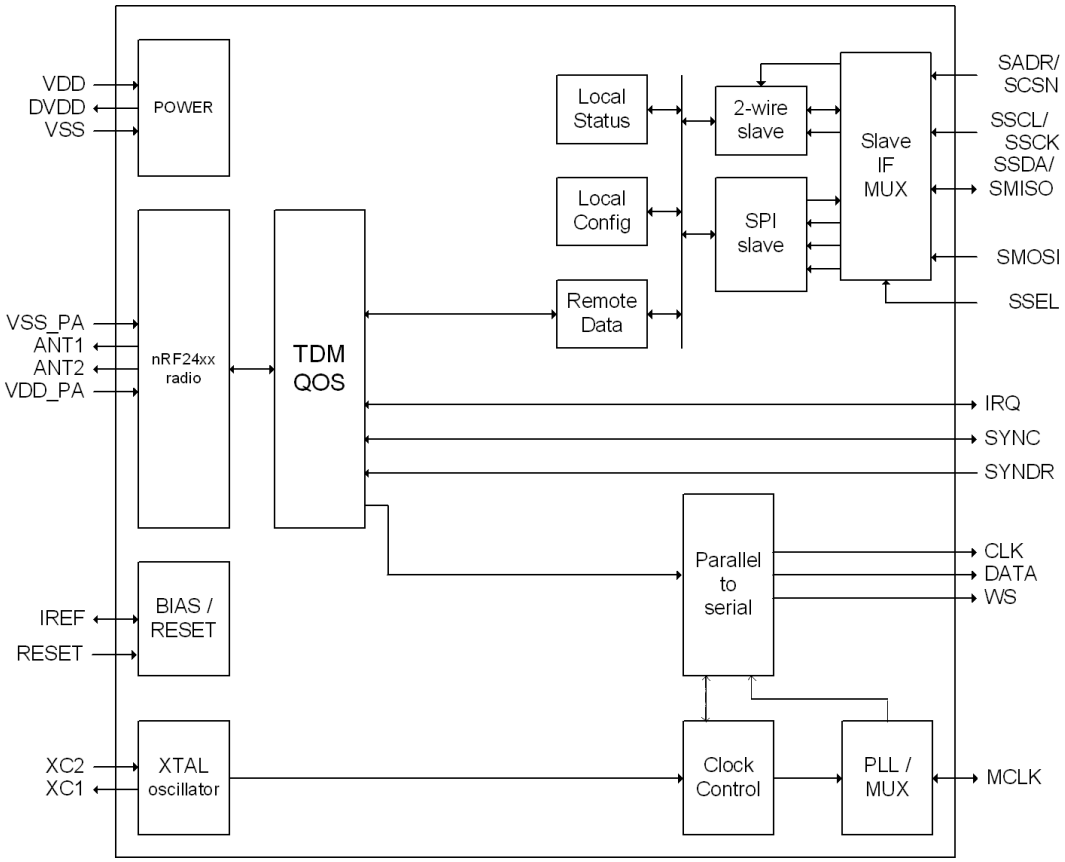


Figure 6. nRF2460 ARX mode block diagram

2.3.5.1 I2S audio output

The audio output (typically a DAC) is driven by the I2S output (pins **CLK**, **DATA** and **WS**). In audio receiver mode, the **MCLK** pin provides a sampling rate clock (f_S) of 256 times the audio sampling rate for an external DAC.

2.3.6 Blocks and functionality common to ATX and ARX

2.3.6.1 Serial control (slave) interfaces

Both ATX and ARX are controlled by an external MCU, and configuration and control data may be entered through a 2-wire or SPI slave serial interface. The same interface is used for reading back status information. The register map is identical to both interfaces, but only one of the interfaces (selected by the **SSEL** pin) may be used in a given application:

SSEL	Description
0	SPI (pin functions **SCSN**, **SSCK**, **SMISO**, **SMOSI**)
1	2-wire (pins **SADR**, **SSCL** and **SSDA**)

*Table 3. Serial interface set by **SSEL** pin*

The **SSEL** pin is read during power-up and reset only.

Pin **SADR** is not part of a standard 2-wire interface, but selects one of two possible bus addresses for the nRF2460.

2.3.6.2 Interrupt output

The nRF2460 can interrupt the external application through pin **IRQ** based on a number of sources. Once **IRQ** has triggered the external MCU, interrupt status can be read through the serial slave interface.

2.3.6.3 XTAL oscillator

The crystal oscillator will provide a stable, reference frequency with low phase noise for the radio and audio functions. See section 15.1 on page 51.

2.3.6.4 Radio transceiver

The RF transceiver part of the circuit is a member of the nRF family of low power highly integrated 2.4 GHz ShockBurst™ transceivers. The transceiver interface is optimized for high speed streaming of up to 4 Mbps. Output power and some radio protocol parameters can be controlled by the user through the Quality of Service (QoS) module.

2.3.6.5 Quality of Service (QoS) engine

The primary function of the QoS engine is to ensure robust communication between the ATX and the ARX in an audio streaming application.

Various data streams with different properties are handled. The available bandwidth is shared among audio data, service data and remote data.

Data integrity is ensured through a number of RF protocol features:

1. Packets of data are organized in frames with each packet consisting of an RF address, payload and CRC.
2. Packets that are lost or received with errors are handled by the error correction level of the QoS engine; a two way, acknowledge protocol: When a packet is received by ARX, it is registered and CRC is verified. After ARX has received a frame, it sends a packet back to ATX acknowledging the packets successfully transferred. Packets lost or received with errors, are re-transmitted from ATX in the next frame.
3. The information (audio data) is dispersed across the 2.4 GHz band by use of an adaptive frequency hopping algorithm. This enables the nRF2460 link to cope with RF propagation

challenges like reflections, multi-path fading and avoid heavily trafficked areas of the 2.4 GHz band. Handling co-existence scenarios with contemporary RF systems such as *Bluetooth*, WLAN as well as other nRF applications, is increasingly important.

The main function of the QoS is to constantly monitor the quality of the RF link.

The secondary function of the QoS module is to run a link initialization algorithm which manages initial connect and re-connect if link is lost (ex: out of range) between paired nRF2460s.

2.3.6.6 Power-supply regulators

The nRF2460 has an internal, linear-regulated, power supply to all internal parts of the device. This makes it very robust with respect to external voltage supply noise and isolates (audio) devices (in an application) from any noise generated by the nRF2460.

2.3.6.7 Bias reference

The **IREF** pin sets up the bias reference for the nRF2460 by use of an external resistor. See section 15.2 on page 51.

3 Operation overview

3.1 Power on / RESET sequence

When a power supply voltage is connected, nRF2460 performs a power-on reset. Reset is held until the supply voltage has been above the minimum supply voltage for a few milliseconds. Pulling **RESET** pin high also puts the device into reset.

After reset (power on or RESET high) is released, the device needs to be configured. An external microcontroller must configure the nRF2460 ATX and ARX through the slave SPI or 2-wire serial interface. The nRF2460 will then start a link initialization procedure based on the link configuration data. The value of the **MODE** pin determines whether it will be in ATX or ARX mode.

It is important that all configuration data are set before the RF transceiver is enabled, by writing to the TXMOD (for the ATX) or RXMOD (for the ARX) registers.

3.2 RF link initialization

The process of establishing a communication link between the ATX and the ARX is referred to as RF link initialization. This involves the ATX systematically probing the frequency band in search for an active ARX with the identical address. Once found, the ATX and ARX are synchronized before audio transmission starts.

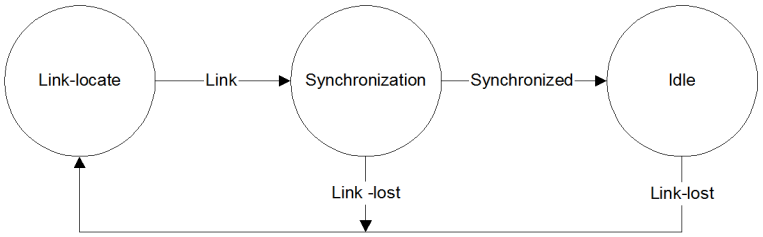


Figure 7. Link initialization algorithm

3.2.1 Idle state

The nRF2460 link initialization algorithm will be in idle state when a link is established. Once established, the frequency hopping engine is initiated and synchronized.

3.2.2 Link-locate state

A special link-locate routine is initiated on both sides in order to (re-)establish a link, see Figure 7. During initialization, nRF2460 uses the NLCH first positions of the frequency hopping table.

3.2.2.1 Link-locate state on ATX

The ATX tries to establish a link with ARX by iteratively sending short search packets on all available channels until an acknowledge signal is received from the ARX. The ATX will send one packet on each channel and wait for acknowledge long enough to secure that the ARX has time to respond. The accumulated time used by the ATX while looping through all available channels, is defined as the ATX-loop-time. After receiving an acknowledge packet from the ARX, the ATX will enter the synchronization state as illlustrated in Figure 7. on page 17 . The dwell time for linking is approximately 600 µs. The dwell time is defined as the time duration for which the ATX is active at a given frequency before changing frequency position.

3.2.2.2 Link-locate state on ARX

The ARX tries to establish a link with the ATX by listening for incoming search packets on all available channels. When a search packet is received, the ARX will proceed by sending one acknowledge packet to confirm a feasible link. The ARX will listen for incoming search packets on each channel for a fixed time longer than the ATX-loop-time. This guarantees at least one search packet to get through on each available channel used by the ARX, as long as this channel is not being occupied by another radio device. After sending the acknowledge packet, the ARX will enter the synchronization state. The dwell time for ARX is approx. (NLCH+1)× 600 µs.

3.2.3 Synchronization state

This state synchronizes the frequency hopping engine on ATX and ARX, ensuring that both units follow the same hopping sequence. The initial start frequency is found in link-locate mode.

3.3 Audio channel

The input audio data can be one of the following common digital audio formats:

- Left justified
- I2S

In the ATX, the input audio stream format is converted to the nRF2460 RF protocol and transferred over the air.

Upon reception in the ARX, the received data is validated and converted to the specified audio output format and fed to the audio output interface.

3.3.1 Audio receiver clock rate generation

The ARX will lock MCLK to its XC1 clock input and derive CLK and WS by dividing the MCLK by the appropriate divisor for the audio rate.

3.3.2 Audio transmitter clock rate generation

Maintaining equal data rates on both sides of the RF link is crucial in any RF system streaming true-time data. This implies keeping the master clock frequency (MCLK) for the ADC on the transmitting side equal to the clock frequency used to output audio samples from the RF device on the receiver side.

If these two clocks are not identical, the receiving end will either run out of samples for the DAC (ARX clock frequency > ATX clock frequency) or overflow (ARX clock frequency < ATX clock frequency), skipping samples.

This problem is solved in the nRF2460 device without the need for a tight tolerance crystal or extensive digital filtering.

As long as the nRF2460 QoS engine is able to maintain the RF link, the ATX locks its master clock output (MCLK) to the rate of the incoming audio stream. The MCLK signal on the ATX side is locked to the reference (crystal) of the ARX side.

3.4 Control channel

A two-way, low bit rate, control and signaling channel runs in parallel with the audio stream. This control channel is a part of the QoS overhead, meaning the difference between on- the- air data rate (4 Mbits) and

the nominal audio data rate 0.5 Mbps. Hence the data channel rate cannot be traded for higher audio data rate. The functionality of the control channel is illustrated in Figure 8.

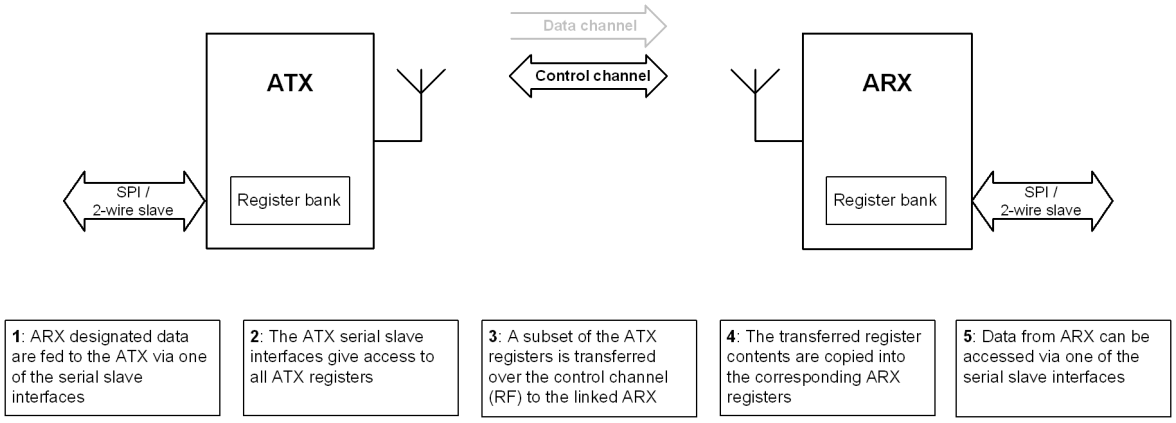


Figure 8. nRF2460 control channel transfer principle

3.5 Register map

The nRF2460 control and status registers are listed in Table 4. on page 20. The registers may be accessed by an external MCU through the slave interface (SPI or 2-wire). The registers are organized functionally into six groups. All registers are present both in audio transmitter and audio receiver. Registers are functional on both sides and the values should match on both sides of the link. DATA channel registers are also functional on both sides, thus creating a bi-directional data channel between the two microcontrollers.

Address HEX	Register	R/W	Initial value	Description
ATX				
0x01	TXSTA	R/W	0x50	Table 8. on page 23
0x02	INTSTA	R/W	0x00	Table 22. on page 39
0x5A	TXMOD	R/W	0x03	Table 8. on page 23
0x52	TXLAT	R/W	0x06	Table 19. on page 37
0x53	INTCF	R/W	0x00	Table 22. on page 39
0x54	I2SCNF_IN	R/W	0x80	Table 8. on page 23
0x56	TXPWR	R/W	0x03	Table 20. on page 37
0x50	TXRESO	R/W	0x08	Table 23. on page 40
LINK status				
0x03	LNKSTA	R/W	0x00	Table 17. on page 36
LINK control				
0x0C-0x31	CH[0:37]	R/W		Table 15. on page 34
0x32	BCHD	R/W	0x0A	Table 16. on page 35
0x33	NBCH	R/W	0x12	Table 16. on page 35
0x34	NACH	R/W	0x26	Table 16. on page 35
0x35	NLCH	R/W	0x26	Table 16. on page 35
0x36	LNKMOD	R/W	0x00	Table 17. on page 36
0x0B	MDUR	R/W	0x00	Table 18. on page 36
0x39-0x3D	ADDR[0:4]	R/W	0x98-38-A2-34-85	Table 14. on page 33
0x3E	LNKCSTATE	R/W	0x00	Table 25. on page 42
DATA channel				
0x4E	DTXSTA	R	0x00	Table 25. on page 42
0x5B	RXCOUNT	R	0x00	Table 13. on page 31
0x5C	TXCOUNT	R/W	0x00	Table 13. on page 31
0x5D-0x5f	RXBUF[0:2]	R	0x00	Table 13. on page 31
0x65-0x67	TXBUF[0:2]	R/W	0x00	Table 13. on page 31
ARX				
0x4A	RXMOD	R/W	0x00	Table 9. on page 24
0x44	I2SCNF_OUT	R/W	0x00	Table 9. on page 24
0x49	RXPWR	R/W	0x03	Table 20. on page 37
0x37	SYNCDL	R/W	0x77	Table 21. on page 38
Test				
0x7E	TESTREG	R/W	0x00	Table 27. on page 44
0x7F	TESTCH	R/W	0x00	Table 27. on page 44
0x7D	REVBYT	R	0x05	Revision byte

Table 4. nRF2460 register listing

4 Digital I/O

This chapter describes the digital I/O pins, control registers and important interface timing of the nRF2460.

The digital I/O pins are divided into two groups:

- Audio interface
- Serial slave interfaces

4.1 Digital I/O behavior during RESET

During RESET, all digital pins are set as inputs to avoid driving conflicts with external devices. All pins will maintain their respective directions until any of the configuration read routines described in section 3.1 on page 17 are completed. The I/O pins are then set according to the new configuration data.

4.2 Audio interface

The audio interfaces consist of the I2S interface plus the **MCLK** pin.

Pin name	Function
CLK	bit clock
WS	word sync clock
DATA	audio data
MCLK	256 x CLK

Table 5. Serial audio port pins

4.2.1 I2S audio interface

The nRF2460 has a three-wire serial audio interface which can be configured to be compatible with various serial audio formats. In ATX mode, the audio interface is in slave or master input mode. In ARX mode, the audio interface is in master output mode. The audio interface consists of 4 pins in total, see Table 5.

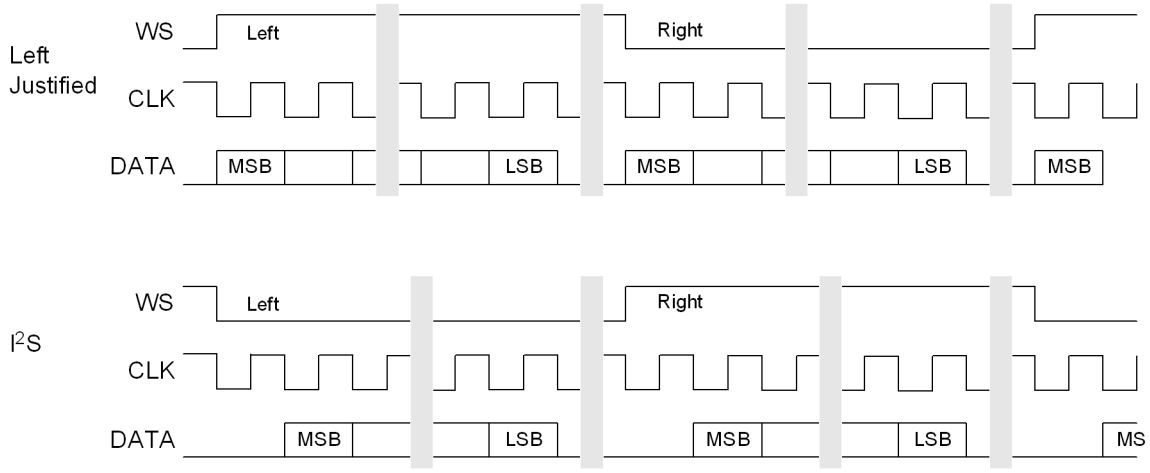


Figure 9. Serial audio formats I2S and left-justified

Audio format	I2SCNF[3:0] value
Left justified	0xA
I2S	0x0

Table 6. Settings for two common serial audio formats

4.2.2 Audio interface functionality

The functionality and direction of the pins in the audio interfaces are listed in Table 7.

Pin number	Pin name	ARX direction	ATX direction (I2SCNF_IN[7]=1)	ATX direction (I2SCNF_IN[7]=0)
10	CLK	OUT	OUT	IN
11	WS	OUT	OUT	IN
12	DATA	OUT	IN	IN
14	MCLK	OUT	OUT	OUT

Table 7. nRF2460 operational modes and audio interface pin functions

4.2.3 ATX audio interface control

The audio interfaces in ATX mode are controlled by the registers listed in Table 8. on page 23.

Address HEX	Register	R/W	Description		
0x01	TXSTA	R/W	ATX audio input rate register		
			Bit	**Interpretation**	
			7:5	Reserved. Must be “010”	
			4:3	Value	Description
				00	Reserved
				01	Reserved
				10	32 kHz
				11	Reserved
			2:0	Reserved, MBZ	
0x5A	TXMOD	R/W	ATX modes of operation		
			7	RF transceiver enable	
			6	Audio transmitter power down	
			5:2	Reserved, MBZ	
			1:0	MCLK output control	
				00	MCLK off (logic 0)
				01	Reserved
				10	Reserved
				11	Output 256 × 32 kHz
0x54	I2SCNF_IN	R/W	ATX I2S interface configuration. See Table 6. on page 22		
			7	I2S audio in clock mode	
				0	Slave mode, WS, CLK, DATA are input (needs to be coherent with MCLK)
				1	Master mode, WS, CLK are output, DATA is input
			6:5	Reserved, MBZ	
			4	Mono sample location	
				0	Use left channel samples
				1	Use right channel samples
			3	WS polarity	
				0	WS=0 for left sample
				1	WS=1 for left sample
			2	Reserved, MBZ	
			1	WS to MSB delay	
				0	1 clock cycle
				1	0 clock cycle
			0	Reserved, MBZ	

Table 8. ATX audio interface control registers

The nRF2460 offers a 256 x clock output on pin **MCLK**. Clock frequency is set in register TXMOD [1:0]. This clock shall be used as master clock to the device that drives the I2S data input on the ATX side.

4.2.4 ARX audio interface control

In ARX mode the audio interfaces are controlled by registers `RXMOD` and `I2SCNF_OUT` listed below.

Address HEX	Register	R/W	Description	
0x4A	`RXMOD`	R/W	ARX modes of operation	
			Bit	**Interpretation**
			7	Audio receiver power down
			6	Reserved, MBZ
			5	RF transceiver enable
			4:0	Reserved, MBZ
0x44	`I2SCNF_OUT`	R/W	ARX I2S interface configuration for audio output. See Table 6. on page 22	
			Bit	**Interpretation**
			7	Reserved, MBZ
			6	Mute sound output
			5:4	Reserved, MBZ
			3	WS polarity
			0	WS=0 for left sample
			1	WS=1 for left sample
			2	Data to Bit Clock relation (data valid at clock edge)
			0	Rising edge
			1	Falling edge
			1	WS to MSB delay
			0	1 clock cycle
			1	0 clock cycle
			0	Reserved, MBZ

Table 9. ARX audio interface control registers

The Mute bit holds the last audio sample and holds it until the Mute bit is cleared again. Then a simple three-sample interpolation scheme is applied between the last sample value and the first unmuted sample value. The same mute behavior is also applied to audio packet loss. Mute on and off is synchronized to the next audio packet boundary.

4.2.5 I2S audio interface timing

4.2.5.1 I2S input (ATX) timing

The I2S input protocol may be configured in register `I2SCNF_IN` to handle various I2S formats. This section describes the detailed bit-, clock- and word timing requirements for audio slave and audio master mode (as set by `I2SCNF_IN` [7]).

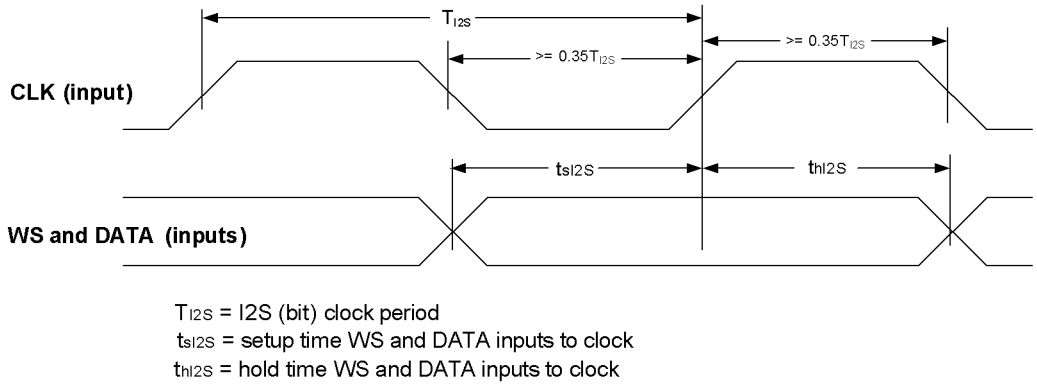


Figure 10. I2S input timing in audio slave mode (I2SCNF_IN[7]=0)

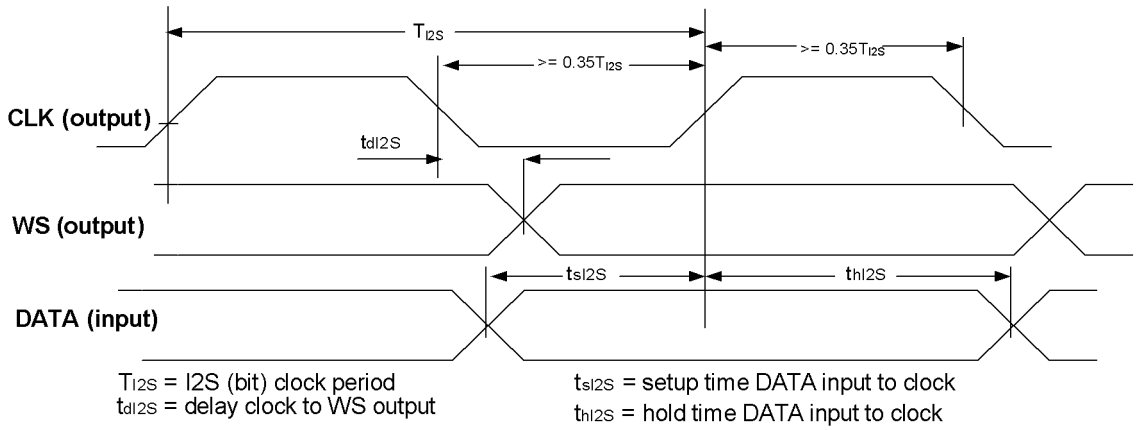


Figure 11. I2S input timing in audio master mode (I2SCNF_IN[7]=1)

4.2.5.2 I2S output (ARX) timing

The I2S output protocol is configurable in register `I2SCNF_OUT` and is compatible with most I2S DACs and CODECs.

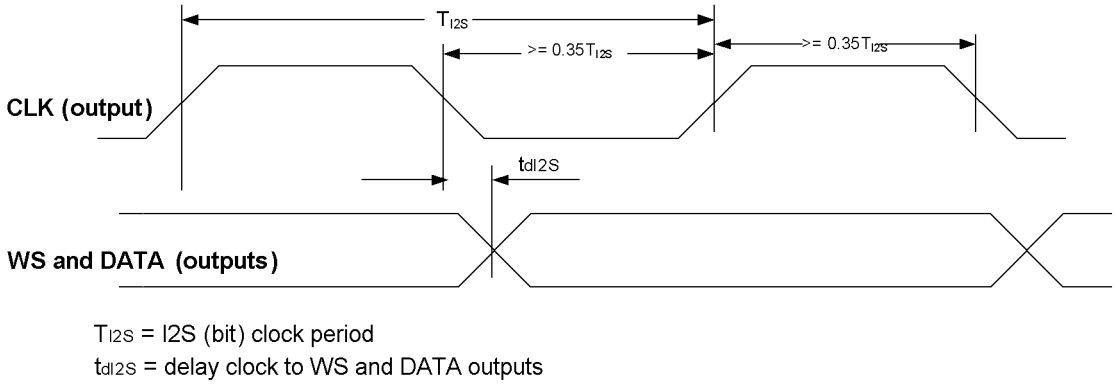


Figure 12. I2S output timing

Refer to Table 28. on page 46 for values.

4.3 Control interfaces

Both ATX and ARX are setup with SPI or 2-wire slave interfaces.

4.3.1 Slave interface and pin configuration

One of two interfaces can be chosen (set by input pin **SSEL**):

nRF2460 serial slave interface pins		Device control: SPI mode (SSEL=0)		Device control: 2-wire mode (SSEL=1)	
Pin number	Name	Function	Direction	Function	Direction
1	**SSEL**	SSEL	IN	SSEL	IN
2	**SMISO/SSDA**	SMISO	OUT	SSDA	IN/OUT
3	**SSCK/SSCL**	SSCK	IN	SSCL	IN/OUT
4	**SCSN/SADR**	SCSN	IN	SADR	IN
6	**SMOSI**	SMOSI	IN	-	Ground(0V)
36	**IRQ**	IRQ	OUT	IRQ	OUT

Table 10. Control pins functionality

4.3.2 SPI slave interface

The first byte of the SPI transaction specifies the address for the register and whether it has a read or a write access. The seven least significant bits in the first byte are the nRF2460 register address, while the most significant bit is the read/write indicator (read=1, write=0), see Table 11.

B7	B6	B5	B4	B3	B2	B1	B0
R/W	Register address						

Table 11. SPI command byte encoding

4.3.2.1 Write transaction

The next byte on **SMOSI** will be put into the register with the address specified in the first byte. Writing additional bytes will increment the register address automatically.

4.3.2.2 Read transaction

The next byte on SMISO will be the contents of the register with the address as specified in the first byte. Reading more bytes will increment the register address automatically.

4.3.2.3 SCSN active low

Consecutive accesses with SCSN low will auto-increment the address.

4.3.3 2-wire slave interface

This interface is similar to what is found on serial memories and data converter devices. The seven-bit device address of nRF2460 is 'a101001', where 'a' is the logic level of the **SADR** input pin (read during power-up and reset only).

Each 2-wire transaction is started with the "Start condition" followed by the first byte containing the seven-bit-long device address and one read/write bit. This byte is hereafter referred to as the "address/read command byte" or the "address/write command byte" depending on the state of the read/write bit (read=1, write=0).

The second byte contains the register address, specifying the register to be accessed. This address will be written into the nRF2460, and it is therefore necessary that the first byte after the first start condition is an address/write command. Further actions on the 2-wire interface depend on whether the access is a read or write access. The 2-wire command byte is illustrated in Table 12.

B7	B6	B5	B4	B3	B2	B1	B0
a	1	0	1	0	0	1	R/W

Table 12. 2-wire command byte encoding

4.3.3.1 2-wire write access

Figure 13. illustrates a simple write operation, where one byte is written to the nRF2460.

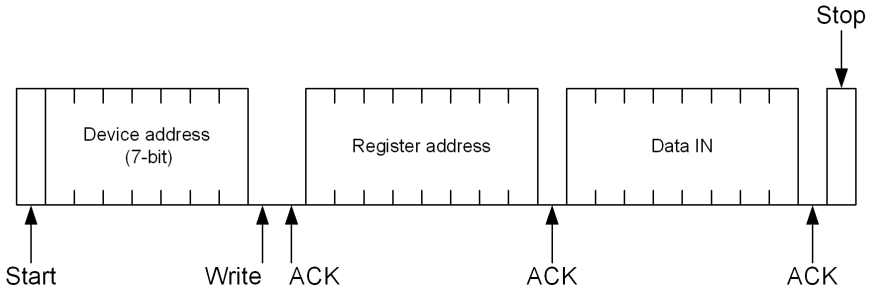


Figure 13. 2-wire write operation example

A write access is composed by a start condition, an address/write command byte, a register address byte and the corresponding data byte. Each byte will be acknowledged by the 2-wire slave by pulling the data

line (SDA) low. To stop the write access, a stop condition is applied on the 2-wire interface. See Figure 15. for an example. Consecutive write access is performed by postponing the stop condition.

4.3.3.2 2-wire read access

Figure 14. illustrates a simple read operation, where one byte is read back from the nRF2460.

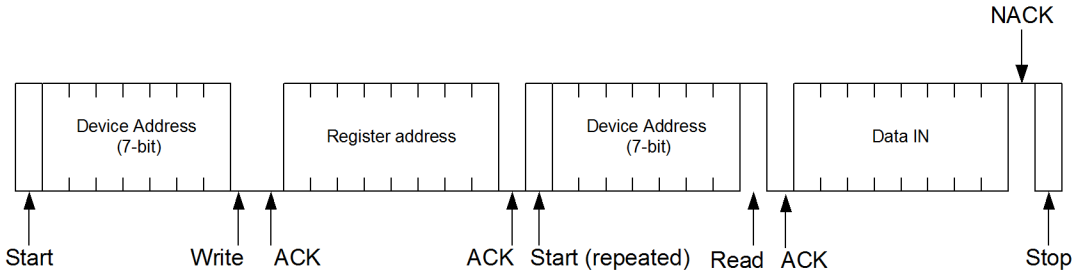


Figure 14. 2-wire read operation

A read access is composed by a start condition, an address/write command byte and a register address byte. These two bytes are acknowledged by the 2-wire slave. This scenario is followed by a repeated start condition and an address/read control byte. This byte is also acknowledged by the 2-wire slave. After the acknowledge bit has been sent from the 2-wire slave, the register value corresponding to the register address byte is supplied by the 2-wire slave. This byte must be acknowledged by the 2-wire master if consecutive register read operations are intended. The read access is stopped by not acknowledging the last byte read, followed by a stop condition. See Figure 15.

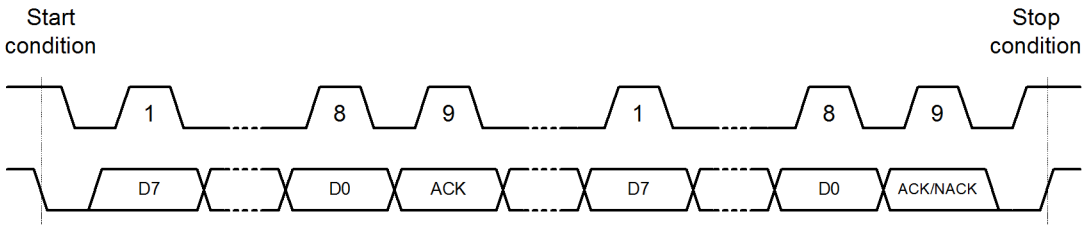


Figure 15. 2-wire waveform example

4.3.4 Control interface timing

4.3.4.1 2-wire slave timing

The interface supports data transfer rates of 100 kHz, 400 kHz and 1 MHz.

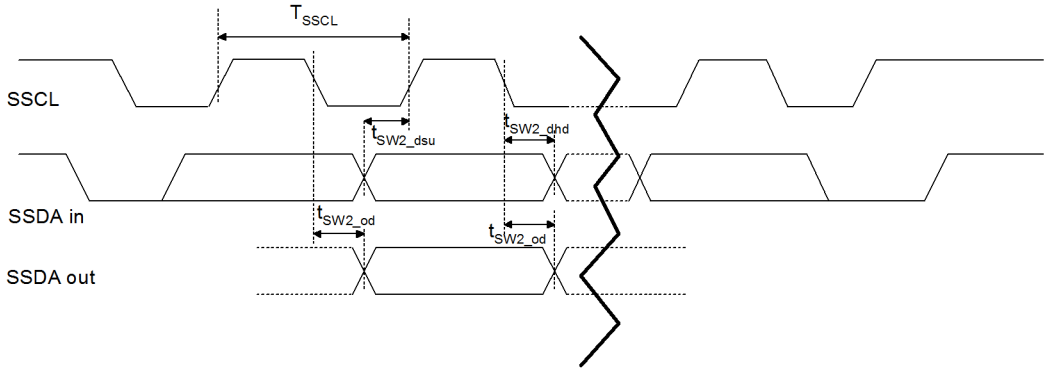


Figure 16. 2-wire slave timing diagram

Refer to Table 28. on page 46 for values.

4.3.4.2 SPI slave timing

Normal SPI slave clock frequency is up to 8 MHz. Note the minimum pause interval t_{SRD} between writing/ reading of a byte.

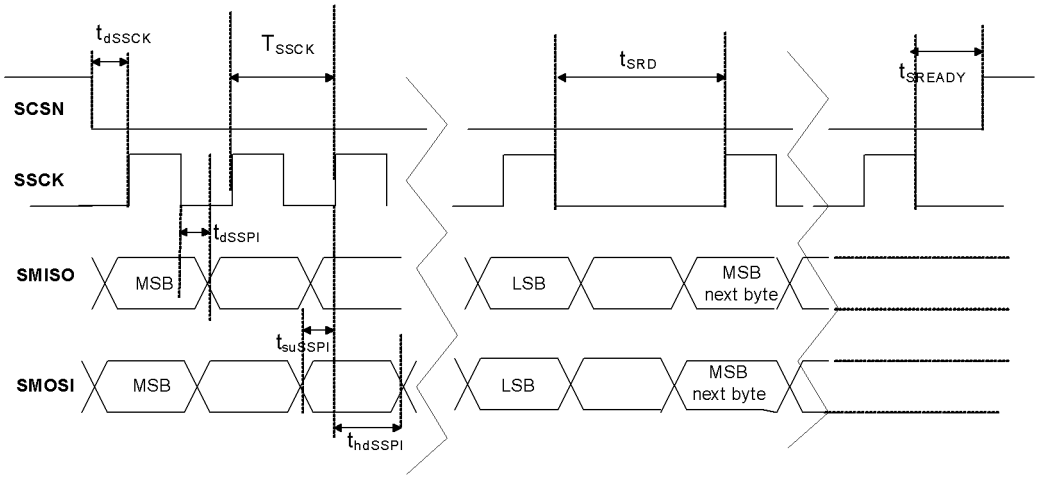


Figure 17. SPI slave timing diagram

T_{SSCK}: SSCK cycle time
t_{dSSCK}: time from SCSN active to first SSCK pulse
t_{dSSPI}: delay from negative edge SSCK to new SMISO output data
t_{suSSPI}: SMOSI setup time to positive edge SSCK
t_{hdSSPI}: SMOSI hold time to positive edge SSCK
t_{SRD}: minimum pause between each byte read from or written to slave SPI
t_{SREADY}: time from SSCK negative edge to SCSN rising edge

Refer to Table 28. on page 46 for values.

4.4 Data channel

The nRF2460 data channel is implemented by the data channel registers TXCOUNT, TXBUF, RXCOUNT, RXBUF and DTXSTA. The MCU on the ATX side can control its set of the registers, and the MCU on the ARX side can control its set of the registers.

Transfer can occur in both directions, and at the same time.

Address HEX	Register	R/W	Description
0x5C	TXCOUNT	R/W	Number of bytes to be transmitted (max 3), from ATX to ARX or from ARX to ATX. Writing to this register will start transmission of the bytes in TXBUF. The TXCOUNT register in ATX and ARX respectively may be written at the same time.
0x5B	RXCOUNT	R	Number of bytes received by ATX or ARX respectively. RXCOUNT received bytes are now ready to be read from the RXBUF registers. An interrupt (flag INTSTA[3]) may be delivered upon successful reception of RXCOUNT bytes.
0x4E	DTXSTA	R	Data transfer status register. An interrupt (flag INTSTA[4]) may be delivered upon successful completion of the TXCOUNT command. Returned values are : 0 : idle, last transfer was successful 1 : busy with on-going transfer 2 : timeout error, last transfer was unsuccessful
0x5D-0x5F	RXBUF[0:2]	R	Received bytes (maximum 3), local buffers in ATX and ARX respectively.
0x65-0x67	TXBUF[0:2]	R/W	Bytes to be transferred (maximum 3) from ATX to ARX or from ARX to ATX. Local buffers in ATX and ARX respectively.

Note: Data transferred by TXCOUNT may be lost even though transfer finished is received. Data transfer should be hand-shaken by application firmware if data transfer is critical.

Table 13. Data channel registers

4.4.1 Typical transfer of data from ATX to ARX

The ATX MCU *must*:

- Write up to three data bytes into TXBUF [0:2]
- Write value 3 to TXCOUNT (this starts the transfer)

If enabled (INTCF[4]), an ATX interrupt will come when the transfer of the three bytes is finished, or the DTXSTA register may be polled. DTXSTA will be 1 until the transfer is finished. Another three bytes may be sent in the same way.

The ARX MCU *may*:

- Enable data receive interrupt, INTCF [3]=1
- If enabled, an ARX interrupt will come when three bytes are received, or alternatively the INTSTA [3] bit may be polled.
- Read the three bytes from RXBUF [0:2]

4.4.2 Typical transfer of data from ARX to ATX

The ARX MCU *must*:

- Write up to three data bytes into TXBUF [0:2]
- Write value three to TXCOUNT (this starts the transfer)

If enabled (INTCF [4]), an ARX interrupt will come when the transfer of the three bytes is finished, or the DTXSTA register may be polled. DTXSTA will be 1 until the transfer is finished.

Another three bytes may be sent in the same way.

The ATX MCU *may*:

- Enable data receive interrupt, INTCF [3]=1. If enabled, an ATX interrupt will come when three bytes are received, or alternatively the INTCF [3] bit may be polled.
- Read the three bytes from RXBUF [0:2]

5 Quality of Service (QoS) and RF protocol

The purpose of the QoS-engine is to maintain audio quality across time during normal operation. This involves:

- Ensuring that corrupt or lost information sent from the ATX is automatically detected and retransmitted to the ARX
- Monitoring and avoiding channels used by other 2.4 GHz equipment or which have poor radio propagation properties (for example fading effects)
- Reducing the audible effect of corrupt data when retransmission fails within the latency time frame
- Establishing a new link in case of communication loss

The control channel is used to monitor radio link status information.

It should be noted that at some point, the QoS-engine is unable to maintain a flawless audio link. This may be the result of stretched range, excessive interference noise or both.

The RF-protocol is an integral part of the QoS-engine and is therefore not subject to user modification.

5.1 Link establishment

The procedure for establishing a link is fully managed on-chip.

5.2 RF protocol

The RF-protocol is controlled on-chip. The only parameter configurable by the application is the address. This enables separate nRF2460 devices to be identified and accessed independently in the same physical area. The RF protocol address length is five bytes and the address bytes are set in registers ADDR [0:4], listed in Table 14.

Address Hex	Register	R/W	Description
0x39	ADDR[0]	R/W	Address byte #0 (LSB)
0x3A	ADDR[1]	R/W	Address byte #1
0x3B	ADDR[2]	R/W	Address byte #2
0x3C	ADDR[3]	R/W	Address byte #3
0x3D	ADDR[4]	R/W	Address byte #4 (MSB)

Table 14. RF protocol address

The contents of ADDR [0:4] are sent to the ARX when 0x01 is written to LNKCSTATE. To enable the new ADDR [0:4] a force reconfiguration must be performed by writing to LNKMOD [4], this will make the ATX and ARX re-link with the new address.

5.3 Adaptive Frequency Hopping (AFH)

Adaptive Frequency Hopping is an integral part of the QoS-engine functionality. The audio data is split into packets which are transmitted at different frequencies known by the transmitter and receiver. The frequencies used change across time as active noise sources in the frequency band appear and disappear. AFH also enables the nRF2460 link to handle challenges such as signal cancellation due to multi-path fading effects. The frequencies used by the AFH-algorithm are specified in up to 38 frequency registers shown in Table 15. on page 34. The contents of CH0-37 cannot be sent from the ATX to the ARX. Register values of CH0-37 must be configured locally by the MCU.

Address Hex	Register	R/W	Initial value	Description
0x0C	CH0	R/W	0x06	Frequency positions for the hopping sequence. The frequency position frequency is equal to the position number multiplied by 1 MHz relative to 2400 MHz. Example: To define a frequency hopping scheme starting at f=2420 MHz, and then hopping to f=2440 MHz, the following values must be set: CH0=0x14, CH1=0x28.
0x0D	CH1	R/W	0x1C	
0x0E	CH2	R/W	0x34	
0x0F	CH3	R/W	0x4C	
0x10	CH4	R/W	0x18	
0x11	CH5	R/W	0x30	
0x12	CH6	R/W	0x48	
0x13	CH7	R/W	0x14	
0x14	CH8	R/W	0x2C	
0x15	CH9	R/W	0x44	
0x16	CH10	R/W	0x10	
0x17	CH11	R/W	0x28	
0x18	CH12	R/W	0x40	
0x19	CH13	R/W	0x0C	
0x1A	CH14	R/W	0x24	
0x1B	CH15	R/W	0x3C	
0x1C	CH16	R/W	0x08	
0x1D	CH17	R/W	0x20	
0x1E	CH18	R/W	0x38	
0x1F	CH19	R/W	0x04	
0x20	CH20	R/W	0x1E	
0x21	CH21	R/W	0x36	
0x22	CH22	R/W	0x4E	
0x23	CH23	R/W	0x1A	
0x24	CH24	R/W	0x32	
0x25	CH25	R/W	0x4A	
0x26	CH26	R/W	0x16	
0x27	CH27	R/W	0x2E	
0x28	CH28	R/W	0x46	
0x29	CH29	R/W	0x12	
0x2A	CH30	R/W	0x2A	
0x2B	CH31	R/W	0x42	
0x2C	CH32	R/W	0x0E	
0x2D	CH33	R/W	0x26	
0x2E	CH34	R/W	0x3E	
0x2F	CH35	R/W	0x0A	
0x30	CH36	R/W	0x22	
0x31	CH37	R/W	0x3A	

Table 15. Frequency hopping table registers

5.3.1 Adapting to the RF environment

In an environment without other 2.4 GHz applications or noise sources, the nRF2460 will use all the frequency positions listed in Table 15. on page 34. In the presence of an active RF system, occasional packet collisions are likely, resulting in RF packets being lost.

When an operating frequency resulting in unacceptable packet loss is detected, the ATX may remove it from the list of frequency positions used by the AFH algorithm. The corresponding list in the ARX is synchronized by use of the control channel, and as a consequence this method cannot be applied during link initialization.

Frequency positions removed from the frequency hopping sequence are added to a FIFO list of frequencies temporarily banned for use by the AFH-algorithm. The length of the list of banned frequencies is configurable (see Table 16.) The maximum number of banned channels is 18. A banned channel will remain in the list of banned frequencies until it is pushed out by a new candidate or as defined by `BCHD` register.

Note: The list of hopping positions does not need to contain solely non-overlapping channels in order to achieve optimal effect. Generally, the frequency positions should be distributed over the available frequency band.

Address Hex	Register	R/W	Description
0x32	`BCHD`	R/W	Banned channel duration. The duration of transmission ban, in number of frequency hops. The time before a banned channel is earliest released from the banned list, is (`BCHD`+1)×NBCH×3.0 ms
0x33	`NBCH`	R/W	Number of banned channels. The number of frequency positions subject to ban at any time. Maximum register value is 18.
0x34	`NACH`	R/W	Number of frequency positions used in normal audio streaming mode. The frequency locations used are the first NACH-locations of Table 15. on page 34.
0x35	`NLCH`	R/W	Number of link channels used in link mode. The frequency locations used are the first NLCH-locations of Table 15. on page 34.

Table 16. Frequency hopping configuration registers

To minimize linking time, the same basic frequency hopping scheme must be set on the ATX and ARX side.

5.4 Link registers

The link functional status is reported in register LNKSTA. Registers LNKSTA and LNKMOD are listed in Table 17.

Address Hex	Register	R/W	Description	
0x03	LNKSTA	R/W	Link status register	
			Bit	**Interpretation**
			7:1	Reserved, MBZ
			0	1:Link established
0x36	LNKMOD	R/W	Link status register	
			Bit	**Interpretation**
			7	Reserved, MBZ
			6	1: ATX and ARX reset to initial (reset) register contents if no counterpart is found on the next link initialization.
			5	Reserved, MBZ
			4	1: Force reconfiguration with new configuration data
			3	Reserved, MBZ
			2	1: Disables adaptive frequency hopping
			1	Reserved, MBZ
			0	1: Enables use of Mute duration feature, see MDUR register

Table 17. Link status/mode registers

5.4.1 Mute behavior

There is an option to set the minimum mute interval length, to avoid fast toggling between audio and muted audio during audio loss.

Address Hex	Register	R/W	Description
0x0B	MDUR	R/W	Mute duration feature. After muting, the ARX must wait MDUR × 24 consecutive audio packets without errors before un-muting. This feature is enabled by LNKMOD bit 0.

Table 18. Mute duration register

5.4.2 RF link latency

Link robustness may be traded with link latency. In systems where latency is not critical, the high latency option should be used. Latency is set in the TXLAT register as shown in Table 20.

Address Hex	Register	R/W	Description		
0x52	TXLAT[1]	R/W	ATX to ARX latency in milliseconds		
			Value	**Description**	**Latency**
			4	Medium	20 ms
			6	High	26 ms

1. Latency values listed are without ADC/DAC delay digital in/out

Table 19. TXLAT register

5.5 RF output power

The only configurable parameter in the RF subsystem is the RF transmitter output power. ATX output power is set in register TXPWR. ARX output power is set in register RXPWR.

Address Hex	Register	R/W	Description	
0x56	TXPWR	R/W	ATX output power	
			Value	**Interpretation**
			0	-20 dBm
			1	-10 dBm
			2	-5 dBm
			3	0 dBm
0x49	RXPWR	R/W	ARX output power	
			Value	**Interpretation**
			0	-20 dBm
			1	-10 dBm
			2	-5 dBm
			3	0 dBm

Table 20. TXPWR and RXPWR registers

5.6 Sync delay signal

The nRF2460 supports synchronization of two ARX placed on the same PCB. The synchronization is achieved by setting the logic level of the **SYNDR** pin and by connecting the **SYNC** pins together. A typical setup is shown below.

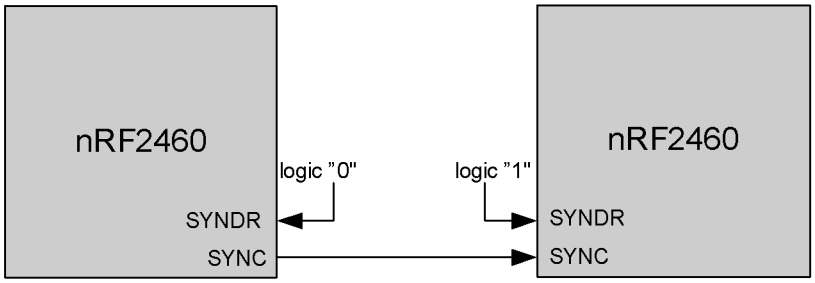


Figure 18. Typical connection for synchronizing two ARX

For best performance the two ARX should be set up with different RF addresses and hopping tables.

The SYNCDL register can be used to change the timing of the SYNC signal. The default value is 119 (decimal) which gives approximately zero delay. Values below 119 give negative delay, while values higher than 119 give positive delay, in steps of approximately 16 µs.

SYNCDL (decimal)	SYNC signal delay	Comment
119	0	Default value
255	2.2 ms	Maximum positive delay
0	-1.9 ms	Maximum negative delay

Table 21. Configurable sync delay between ARX pairs

The SYNCDL value must be set before RXMOD[5] is set.

6 Interrupts

The nRF2460 can be configured to deliver interrupts to any external system connected to pin **IRQ**. Interrupt sources are defined by register INTCF. Interrupt status flags are available in register INTSTA (0x02). After interrupt initiation, the IRQ will stay active (logic 0 with INTCF [7] = 0, logic 1 with INTCF [7] = 1) until a logic 1 is written to the corresponding interrupt flag in the INTSTA register. All interrupt flags may be cleared by writing 0x7F to INTSTA.

Address Hex	Register	R/W	Description	
0x02	INTSTA	R/W	Interrupt status register. Register contents and interrupt are cleared upon writing a “1” to the respective bit. See register INTCF for interrupt enabling.	
			Bit	**Interpretation**
			7	Reserved MBZ
			6	Link broken status flag
			5	Reserved, MBZ
			4	Remote transfer done status flag, set upon completion of a TXCOUNT or LNKCSTATE command
			3	Data received, RXCOUNT bytes available in RXBUF[0:2]
			2	Reserved, MBZ
			1	Reserved, MBZ
			0	Reserved, MBZ
0x53	INTCF	R/W	Interrupt configuration. Select events that can generate interrupt on the **IRQ** pin.	
			Bit	**Interpretation**
			7	**IRQ** pin polarity, 1 is active high, 0 is active low
			6	Enable link broken interrupt
			5	Reserved, MBZ
			4	Enable remote transfer done interrupt
			3	Enable data received interrupt
			2	Reserved, MBZ
			1	Reserved, MBZ
			0	Reserved, MBZ

Table 22. Registers INTCF and INTSTA

7 RESET output

An nRF2460 in ATX mode has a configurable RESET output pin **RESO**, which may be used to provide a RESET pulse to peripherals such as an ADC. The RESET pulse is executed as a part of the configuration routine performed immediately after power-on-reset and after device reconfiguration.

RESO pin behavior is controlled by register TXRESO for the ATX. This function is not available for the ARX.

Address Hex	Register	R/W	Description	
0x50	TXRESO	R/W	Enabling of optional RESET pulse output from ATX	
			Bit	**Interpretation**
			7:4	Reserved, MBZ
			3:1	0: no RESET output 1,2,3: Reserved, MBZ 4: RESET output on pin 28 **RESO** 5,6,7: Reserved, MBZ
			0	ATX RESET output polarity 0: active low 1: active high Reset pulse duration is approximately 285 µs.

Table 23. TXRESO register

8 Power-down control

8.1 Activation of power-down mode

Power-down mode can only be activated by the external microcontroller. The ATX power-down mode is initiated by setting register TXMOD [6]=1. The ARX power-down mode is initiated by setting register RXMOD [7]=1. Register TXMOD is described in Table 8. on page 23 and register RXMOD is described in Table 9. on page 24.

8.2 Wake up from power down

The device will wake you up again upon a negative transition on pin 2 (**SSDA**) or pin 4 (**SCSN**), depending on which slave interface is selected. See Table 24.

SSEL	Description	Wake up pin
0	SPI slave interface selected	Pin 4, **SCSN**
1	2-wire interface selected	Pin 2, **SSDA**

Table 24. Wake-up pin selection

All register content will be kept during power down.

8.3 Power down current

The power down current depends on the direction of the audio interface pins, so to achieve minimum power down current, the pins which are configured as inputs, must not be left floating by the external audio circuitry. Whether the pins are left floating or not depends on how the device is configured.

After power on, all audio interface pins are default configured as input pins and will remain so until an audio link is established.

When in audio-streaming mode, the direction of the audio interface pins is as shown in Table 7. on page 22.

9 Register update over the control channel

The LNKCSTATE register can be used by the ATX MCU to update the ARX link control registers through the control channel. Writing to LNKCSTATE from the ARX MCU is illegal, and LNKCSTATE must not be written to, if it is not idle.

When LNKCSTATE is set to 0x01, the ATX will send all the link control registers, except the CH-registers, to the ARX. LNKCSTATE is then automatically reset to 0x00 after all register values have been successfully transferred. When LNKCSTATE reads 0x01, the ATX is busy sending the register values to the ARX. When LNKCSTATE reads 0x02, that means the last transfer was unsuccessful. A value of 0x02 may indicate a radio link problem.

Address Hex	Register	R/W	Description
0x3E	LNKCSTATE	R/W	Controls when to send ATX side link control registers over the data link to the ARX. Status values are: 0 : idle, last transfer was successful 1 : busy, registers may not be accessed 2 : idle, last transfer was unsuccessful When idle, data may be written to the link control registers. Setting LNKCSTATE = 1 triggers the ATX to send link control register values to the ARX. LNKCSTATE will be reset to 0 by the ATX upon successful transfer to the ARX. The external MCU should poll this register before accessing any link control registers.

Table 25. Register update registers

9.1 Register update and device relink

Some register updates can only be changed while the RF transceiver is disabled, or require a force reconfiguration, if changed.

The ATX and ARX will always be reconfigured after a link has been established. They can also be reconfigured by forcing a re-link if any of the following registers change value. This can be done by setting "Force reconfiguration" by LNKMOD [4] = 1.

Register category	Register name	Comment
ATX registers	TXLAT TXSTA TXMOD[1:0] I2SCNF_IN	Must be set locally, with identical values in ATX and ARX
LINK registers	ADDR0, ADDR1, ADDR2, ADDR3, ADDR4, NBCH,NACH, NLCH,BCHD	Can be set locally, with identical values in ATX and ARX; or ATX values may be transferred to ARX by use of LNKCSTATE
ARX registers	I2SCNF_OUT [3:1]	Must be set locally, with identical values in ATX and ARX
Test registers	TESTREG TESTCH	Must be set locally

Table 26. Registers requiring device re-configuration, if changed

10 Test mode

An nRF2460 test mode is initiated by writing to test registers TESTREG and TESTCH, followed by setting bit 4 of the LNKMOD register. This will force the device to restart in test mode according to the TESTREG and TESTCH register settings.

The nRF2460 will remain in test mode until it is reset. Test mode can only be aborted by the use of reset. Moreover, test mode changes can only be performed upon device reset. This applies to both the ATX and ARX.

The test registers can be accessed through the SPI- or 2-wire slave interface.

Address Hex	Register	R/W	Description	
0x7E	TESTREG	W	Test mode register: Code 1: 0110 0011 – Single channel test. Code 2: 0111 0011 – Channel sweep test. Sweeps all channels from frequencies from 2400 MHz to 2480 MHz in steps of 1 MHz.	
0x7F	TESTCH	W	**Bit**	**Interpretation**
			7	1: TX, 0: RX Initiates the mode described in TESTREG in RX/TX mode.
			6:0	Channel number when TESTREG is set to Code 1 (single channel), number is in 1 MHz step relative to 2400 MHz.

Table 27. Test mode registers

Output power in test mode is always 0dBm, and any other setting in TXPWR and RXPWR registers is ignored in test mode.

To enable test mode, the “Force reconfiguration” bit in LNKMOD [4] must be set after writing TESTREG and TESTCH.

11 Electrical specifications

Symbol	Parameter (condition)	Notes	Min.	Nom.	Max.	Units
	Operating conditions					
VDD	Supply voltage		2.2	3.0	3.3	V
TEMP	Operating temperature		0	27	60	ºC
	Digital input pins					
V_{IH}	HIGH level input voltage		0.7×VDD		VDD	V
V_{IL}	LOW level input voltage		VSS		0.3×VDD	
	Digital output pins					
V_{OH}	HIGH level output voltage (I_{OH}= - 0.5mA)		VDD - 0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		VSS		0.3	V
	General electrical specification					
I_{PD}	Supply current in power down mode			5		µA
	General RF conditions					
f_{OP}	Operating frequency	1	2400	2404 to 2478	2521	MHz
Δf	Frequency deviation			+/- 640		kHz
R_{GFSK}	GFSK data rate			4000		kbps
BW_{MOD}	Modulation bandwidth				4	MHz
f_{XTAL}	Crystal frequency	2		16		MHz
C_{load}	Crystal load capacitance	2	8	12	16	pF
Δf_{XTAL}	Crystal frequency tolerance	2			+/-50	ppm
	RF transmit mode					
P_{RF} 0dBm	Maximum output power (TXPWR=3)	3		0	3	dBm
P_{RF} -5dBm	Maximum output power (TXPWR=2)	3		-5	0	dBm
P_{RF} -10 dBm	Maximum output power (TXPWR=1)	3		-10	-5	dBm
P_{RF}-20dBm	Maximum output power (TXPWR=0)	3		-20	-12	dBm
P_{RFC}	RF power control range		16	20		dB
P_{RFCR}	RF power control range resolution				+/-3	dB
P_{BW}	20 dB bandwidth for modulated carrier			2500	4000	kHz
	RF receive mode					
RX_{SENS}	Sensitivity at 0.1% BER			-80		dBm
RX_{MAX}	Maximum received signal		0			dBm
	ATX current consumption					
I_{ATX} 0dBm	Average supply current in audio streaming mode @ 0dBm output power	4 5		13		mA
I_{ATXmax}	Peak supply current in audio streaming mode	5		34		mA
$I_{ATX\ -5dMm}$	Average supply current at -5dBm output power			12		mA

Symbol	Parameter (condition)	Notes	Min.	Nom.	Max.	Units
$I_{ATX\ -10dMm}$	Average supply current at -10dBm output power			12		mA
$I_{ATX-20dBm}$	Average supply current at -20dBm output power			12		mA
	ARX current consumption					
I_{ARX} link	Average supply current in link mode			33		mA
I_{ARX} au	Average supply current in audio streaming mode	5		32		mA
	I2S interface timing (See Figure 10. on page 25, Figure 11. on page 25 and Figure 12. on page 26)					
T_{I2S}	I2S clock period		150			ns
T_{sI2S}	DATA and WS (input) setup time to CLK		20			ns
T_{hI2S}	DATA and WS (input) hold time from CLK		20			ns
T_{dI2S}	DATA and WS (output) delay from CLK				40	ns
	MCLK (256 x 32 kHz)					
Δf_{MCLK}	Locking range versus nominal MCLK frequency		-500		+500	ppm
J_{RMS}	RMS jitter 0 to 25 kHz			250	310	ps
	Slave SPI interface timing (See Figure 17. on page 30)					
T_{SSCK}	SSCK clock period		124			ns
t_{suSSPI}	SMOSI setup time to SSCK		10			ns
t_{hdSSPI}	SMOSI hold time from SSCK		10			
tdSSPI	SMISO delay from SSCK				55	ns
t_{dSSCK}	SCSN setup time to SSCK		500			µs
t_{SRD}	SPI slave ready		500			µs
t_{SREADY}	SCSN hold time to SSCK		500			µs
	Slave 2-wire interface timing (See Figure 16. on page 29)					
T_{SSCL}	2-wire clock period		1000			ns
$t_{SW2\ dsu}$	SSDA setup time to SSCL		50			ns
$t_{SW2\ dhd}$	SSDA hold time from SSCL		65			ns
$t_{SW2\ od}$	SSDA 1 ->0 delay from SSCL				170	ns

1. Usable band is determined by local regulations.
2. For further details on crystal specifications, see section 15.1 on page 51.
3. Antenna load impedance=100Ω + j175Ω , see chapter 15 on page 51.
4. With a good quality link and little retransmission
5. $C_{MCLK} \approx 8pF$

Table 28. nRF2460 electrical specifications

12 Absolute maximum ratings

Parameter	Minimum	Maximum	Unit
Supply voltages			
VDD	-0.3	+3.6	V
VSS		0	V
Input voltage			
V_I	-0.3	VDD+0.3	V
V_O	-0.3	VDD+0.3	V
Temperatures			
Operating temperature	0	60	°C
Storage temperature	-40	+125	°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Attention!
Observe precaution for handling
Electrostatic Sensitive Device.

HBM (Human Body Model): Class 1A

13 Mechanical specifications

The nRF2460 is packaged in a 36 pin 6 by 6 QFN.

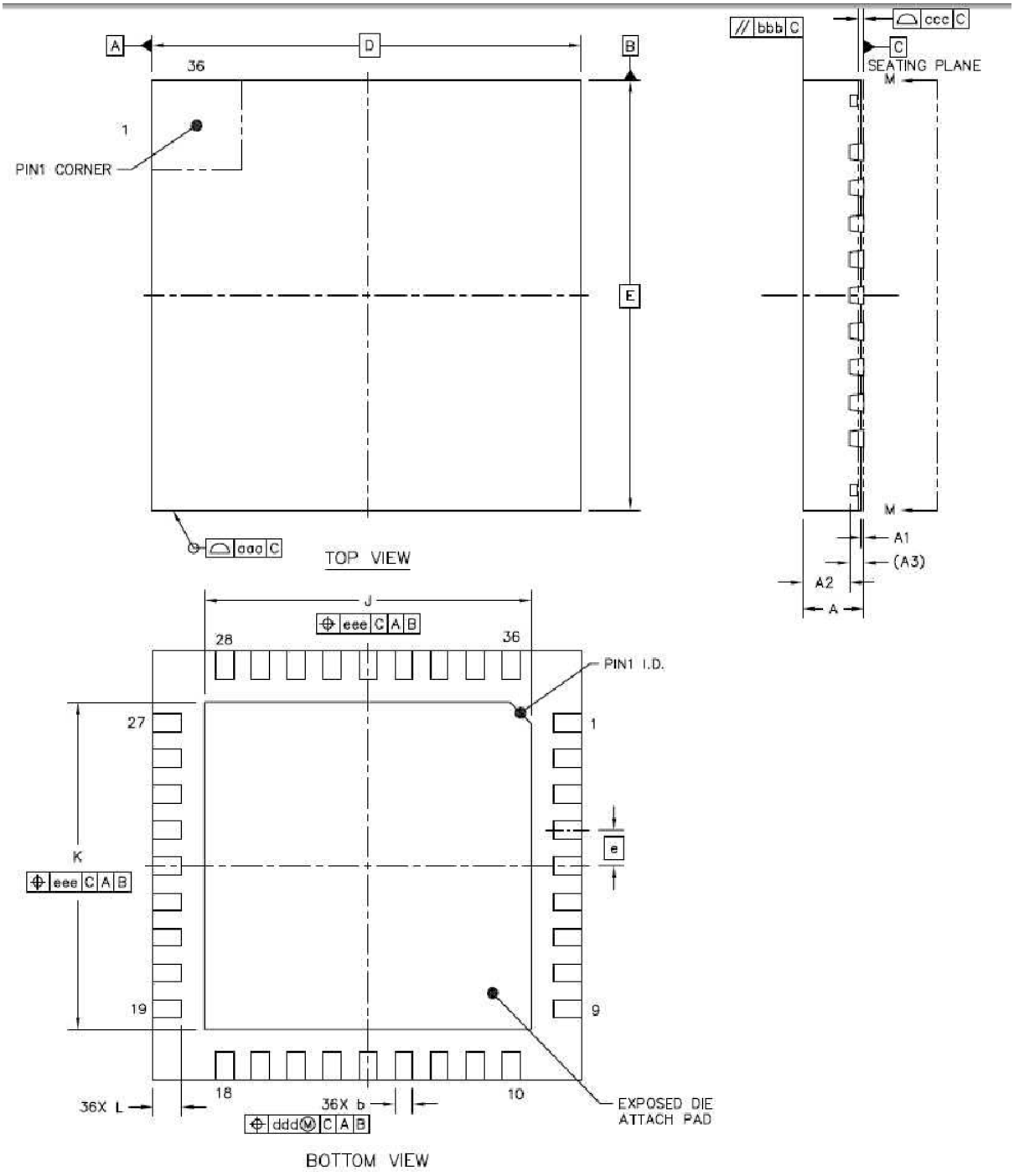


Figure 19. QFN36 pin 6x6

Package		A	A_1	A_2	A_3	b	D/E	e	J/K	L	aaa/ bbb/ ddd/ eee	ccc
QFN36 (6x6mm)	Min	0.8	0	-	0.203 REF	0.2	6 BSC	0.5 BSC	4.47	0.35	0.1	0.08
	Nom	0.85	0.035	0.65	0.203 REF	0.25	6 BSC	0.5 BSC	4.57	0.4	0.1	0.08
	Max	0.9	0.05	0.67	0.203 REF	0.3	6 BSC	0.5 BSC	4.67	0.45	0.1	0.08

Table 29. QFN36 dimensions in mm

14 Ordering information

14.1 Package marking

n	R	F		*B*	*X*
2	4	6	0		
Y	Y	W	W	L	L

Figure 20. nRF2460 package marking layout

14.2 Abbreviations

Abbreviation	Definition
2460	Product number
B	Build code, that is, unique code for production sites, package type and test platform. Variable.
X	"X" grade, that is, Engineering Samples (optional)
YY	Two-digit year number
WW	Two-digit week number
LL	Two-letter wafer-lot number code

Table 30. Abbreviations

14.3 Product options

14.3.1 RF silicon

Ordering code	Package	Container	MOQ[1]	MSL level[2]
nRF2460-R	6x6mm 36-pin QFN	Tape-and-reel	2500	2
nRF2460-T	6x6mm 36-pin QFN	Tray	490	2

1. Minimum Order Quantity
2. The Moisture Sensitivity Level rating according to the JEDEC industry standard classification

Table 31. nRF2460 silicon options

14.3.2 Development tools

Type Number	Description
nRF6700	nRFgo Starter Kit
nRF2460-DK	nRFgo Development Kit for nRF2460
nRF6915	nRFready Microphone Reference Design

Table 32. nRF2460 solution options

15 Application information

To ensure optimal performance it is essential that you follow the schematics- and layout references closely. Especially in the case of the antenna matching circuitry (components between device pins **ANT1**, **ANT2**, **VDD_PA** and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50Ω single end antenna.

15.1 Crystal specification

Tolerance includes initial accuracy and tolerance over temperature and aging.

Frequency	C_L	ESR	C_{0max}	Tolerance
16 MHz	8pF to 16pF	100	7.0pF	+/-50 ppm

Table 33. Crystal specification for nRF2460

In order to obtain a crystal setup with low power consumption and fast start-up time, a crystal with low crystal load capacitance is recommended.

The crystal load capacitance, C_L, is given by:

$$C_L = \frac{C_1' \cdot C_2'}{C_1' + C_2'}, \quad where\ C_1' = C_1 + C_{PCB1} + C_{I1}\ and\ C_2' = C_2 + C_{PCB2} + C_{I2}$$

C_1 and C_2 are SMD capacitors as shown in the application schematic. C_{PCB1} and C_{PCB2} are the layout parasitic on the circuit board. C_{I1} and C_{I2} are the capacitance seen into the **XC1** and **XC2** pin respectively, the value is typical 1pF.

15.2 Bias reference resistor

A resistor between pin **IREF** (pin 24) and ground sets up the bias reference for the nRF2460. A 22 kΩ (1%) resistor is to be fitted. Changing the value of this resistor will degrade nRF2460 performance.

15.3 Internal digital supply de-coupling

Pin **DVDD** (pin15) is a regulated output of the internal digital power supply of nRF2460. The pin is purely for de-coupling purposes and only a 33nF (X7R) capacitor is to be connected. The pin must not be connected to external **VDD** and cannot be used as power supply for external devices.

15.4 PCB layout and de-coupling guidelines

A well-designed PCB is especially necessary in order to achieve good RF performance. Keep in mind that a poor layout may lead to loss of performance, or even functionality if due care is not taken. A fully qualified RF-layout for the nRF2460 and its surrounding components, including antenna matching network, can be downloaded from www.nordicsemi.com.

A PCB with a minimum of two layers with ground planes is recommended for optimum performance. The nRF2460 DC supply voltage must be de-coupled as close as possible to the **VDD** pins, see chapter 16 on page 53. A large value capacitor (for example 4.7µF to 10µF) should be placed in parallel with the smaller value capacitors. The nRF2460 supply voltage must be filtered and routed separately from the supply voltages of other circuitry. When the nRF2460 is used in combination with A/D and D/A converters, it is very important to avoid power supply noise generated by the nRF2460 from reaching the analogue supply pins of the A/D and D/A converters. Hence, star-routing directly from a low-noise supply source (for example a linear voltage regulator) is highly recommended, and where the nRF2460 has its own power supply line from the supply source and also the A/D and D/A converters have their own separate digital and analogue supply lines.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF2460 IC. For a PCB with a topside RF ground plane, the **VSS** pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to place Via holes as close as possible to the **VSS** pins. A minimum of one Via hole should be used for each **VSS** pin.

Full swing digital data or control signals should not be routed close to the reference crystal or the power supply lines.

16 Reference circuits

This chapter shows a typical schematic and reference layout for both ATX and ARX.

16.1 Schematic

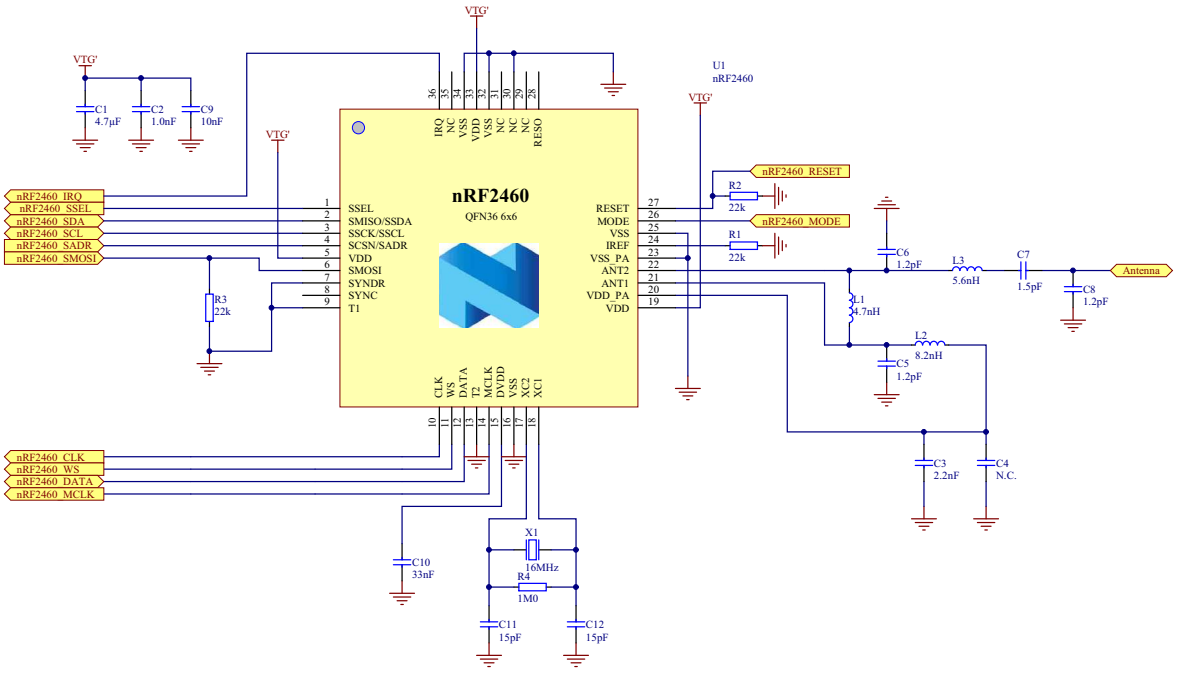
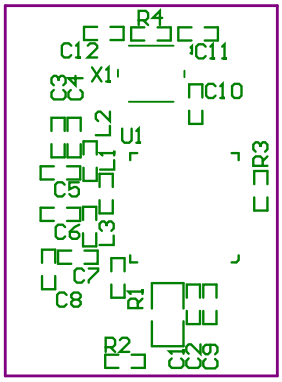


Figure 21. nRF2460 schematic

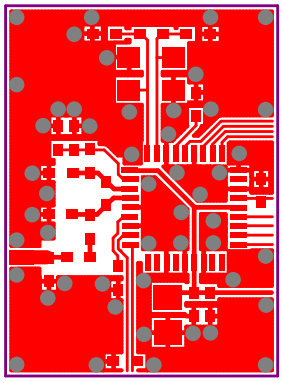
Resistor R3 is not necessary for device functionality. R3 is added to guarantee that no nRF2460 register is written to if the external MCU is resetting.

16.2 Layout

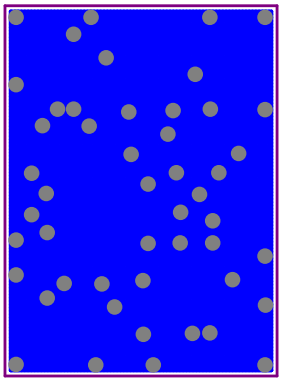


Top silk screen

No components
in bottom layer



Top view



Bottom view

Figure 22. nRF2460 PCB layout

16.3 Bill of Materials

Designator	Value	Footprint	Description
C1	4.7µF	0805	X7R+/-10%
C2	1.0 nF	0402s	X7R+/-10%
C3	2.2nF	0402s	X7R+/-10%
C5, C6, C8	1.2pF	0402s	NP0 +/-0.1pF
C7	1.5pF	0402s	NP0 +/-0.1pF
C9	10nF	0402s	X7R+/-10%
C10	33nF	0402s	X7R+/-10%
C11, C12	15pF	0402s	NP0 +/-2%
L1	4.7nH	0402s	High frequency chip inductor +/-5%
L2	8.2nH	0402s	High frequency chip inductor +/-5%
L3	5.6nH	0402s	High frequency chip inductor +/-5%
R1	22kΩ	0402s	1%
R2, R3	22kΩ	0402s	5%
R4	1M0	0402s	5%
U1	nRF2460	QFN36	6x6mm package
X1	16 MHz	3.2x2.5mm	SMD-3225, 16 MHz, CL=9pF, +/-50 ppm

Table 34. nRF2460 BOM

17 Glossary

Term	Description
ADC	Analog to Digital Converter
AFH	Adaptive Frequency Hopping
ARX	Audio Receiver
ATX	Audio Transmitter
BER	Bit Error Rate
BOM	Bill Of Materials
CD	Carrier Detect
CPHA	SPI Clock Phase
CLK	Clock
CPOL	CSPI Clock Polarity
CRC	Cyclic Redundancy Check
CSN	Chip Select Not
DAC	Digital to Analog Converter
FIFO	First In First Out
Flash	Flash memory
GFSK	Gaussian Frequency Shift Keying
GPIO	General Purpose In Out
I2S	Three-wire audio serial interface
ISM	Industrial Scientific Model
Latency	Audio delay from ATX input to ARX output
LPCM	Linear PCM (pulse code modulation)
LSB	Least Significant Bit
Mbps	Megabits per second
MBZ	Must Be Zero (0)
MSB	Most Significant Bit
PCB	Printed Circuit Board
QoS	Quality of Service
SPI	Serial Peripheral Interface
2-wire	2-wire serial interface compatible with I2C

Figure 23. Glossary of terms