# SM9501A

## Radio Controlled Clock Receiver IC

## OVERVIEW

The SM9501A is a BiCMOS RCC*1 receiver IC. It accepts low frequency standard wave input received from an external antenna, amplifies it, detects the data signal, and outputs a digital time code signal.

*1: Radio controlled clock

## FEATURES

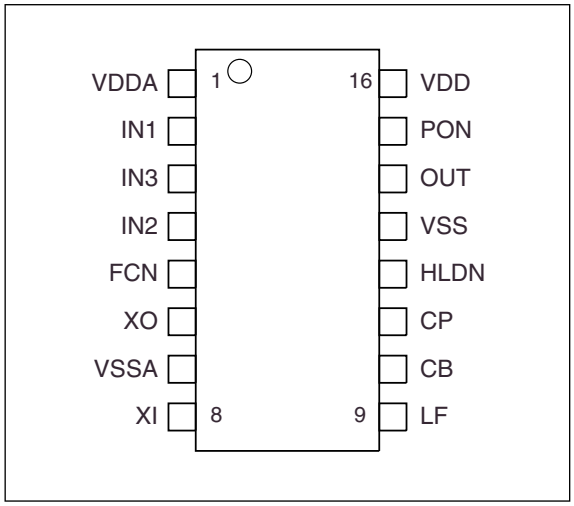
- Operating supply voltage range: 2.4 to 3.6V
- Operating current consumption: 55µA (typ) @3V
- Standby current consumption: 0.1µA (max) @3V
- High sensitivity: 0.5µVrms input
- Wide frequency range (35kHz to 80kHz)
- Include analog switch for antennatuning capacitors change
- AGC gain hold function
- External crystal filter connection
- BiCMOS process
- Package:16-pin VSOP, Chip form

## ORDERING INFORMATION

| Device | Package |
|---|---|
| SM9501AV | 16-pin VSOP |
| CF9501A | Chip form |

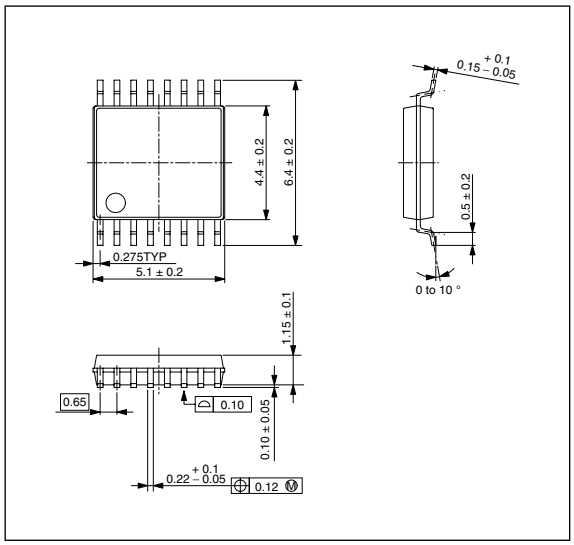
## PINOUT

(Top view)



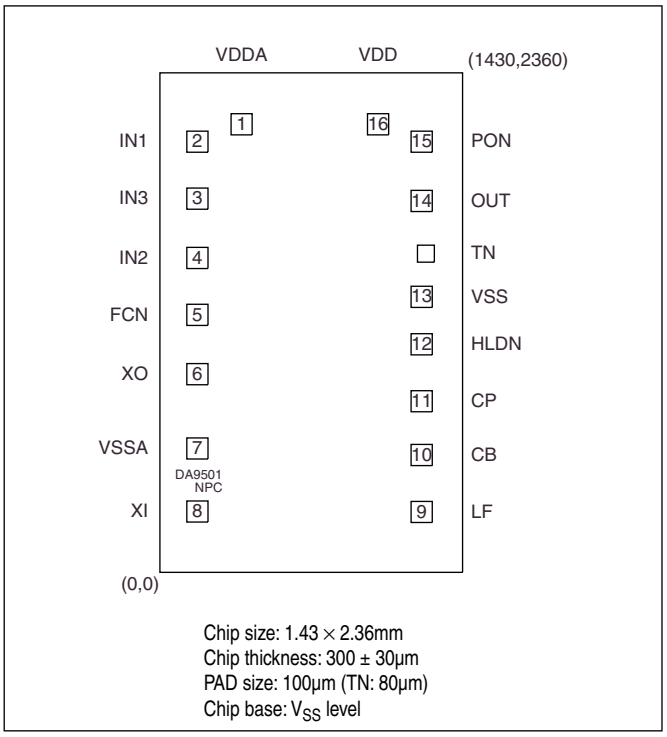

## PACKAGE DIMENSIONS

(Unit: mm)



## PAD LAYOUT (CF9501A)

(Unit: µm)

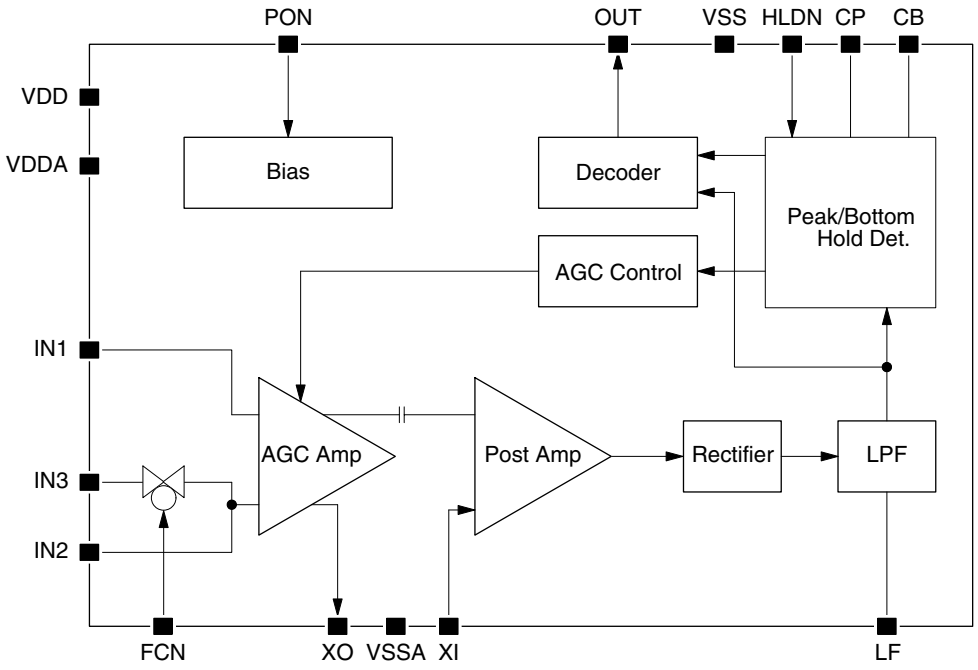



## PAD NAME and DIMENSIONS (CF9501A)

| Pad number | Pad name | Pad dimensions [µm] | |
|---|---|---|---|
| | | X | Y |
| 1 | VDDA | 386 | 2117 |
| 2 | IN1 | 177 | 2035 |
| 3 | IN3 | 177 | 1766 |
| 4 | IN2 | 177 | 1486 |
| 5 | FCN | 177 | 1217 |
| 6 | XO | 177 | 937 |
| 7 | VSSA | 177 | 586 |
| 8 | XI | 177 | 288 |
| 9 | LF | 1237 | 286 |
| 10 | CB | 1237 | 555 |
| 11 | CP | 1237 | 809 |
| 12 | HLDN | 1237 | 1078 |
| 13 | VSS | 1237 | 1302 |
| 14 | OUT | 1237 | 1755 |
| 15 | PON | 1237 | 2035 |
| 16 | VDD | 1031 | 2117 |
| – | TN[1] | 1257 | 1506 |

1. For test mode

## BLOCK DIAGRAM




## PIN DESCRIPTION

| Number | Name | I/O[1] | A/D[2] | Description |
|---|---|---|---|---|
| 1 | VDDA | – | A | AGC amplifier (+) supply input |
| 2 | IN1 | I | A | Antenna input 1 (fixed input) |
| 3 | IN3 | I | A | Antenna input 3 (via analog switch) |
| 4 | IN2 | I | A | Antenna input 2 (analog switch bypass) |
| 5 | FCN | Ipu | D | Analog switch control input (active LOW) |
| 6 | XO | O | A | Output for crystal filter |
| 7 | VSSA | – | A | AGC amplifier (–) supply input |
| 8 | XI | I | A | Input from crystal filter |
| 9 | LF | O | A | Rectifier LPF capacitor connection |
| 10 | CB | O | A | Bottom hold detector capacitor connection |
| 11 | CP | O | A | Peak hold detector capacitor connection |
| 12 | HLDN | Ipu | D | AGC gain hold control (active LOW) |
| 13 | VSS | – | A | Substrate (–) supply input |
| 14 | OUT | O | D | Clock time code output (active LOW) |
| 15 | PON | Ipu | D | Standby state control input (active LOW) |
| 16 | VDD | – | A | (+) supply input |
| – | TN | Ipu | D | AGC amplifier gain control switch (active LOW, for test mode) |

1. I: input, O: output, Ipu: input with pull-up resistor, –: supply pin
2. A: analog signal, D: digital signal

# SPECIFICATIONS

## Absolute Maximum Ratings

$V_{SS}$ = 0V

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage range | $V_{DD}$ | | –0.3 to +7.0 | V |
| Input voltage range | $V_{IN}$ | | –0.3 to $V_{DD}$ +0.3 | V |
| Power dissipation | $P_D$ | 16-pin VSOP | 150 | mW |
| Storage temperature range | $T_{stg}$ | 16-pin VSOP | –55 to +125 | °C |
| | | Chip form | –65 to +150 | °C |

Note. Absolute maximum ratings are the values that must never exceed even for a moment. The device may be damaged or deteriorated the characteristics or reliability if these parameter ratings are exceeded.

## Recommended Operating Conditions

$V_{SS}$ = 0V

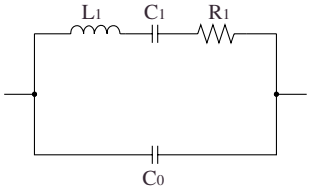
| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage range | $V_{DD}$ | | 2.4 to 3.6 | V |
| Operating temperature range | $T_{opr}$ | | –20 to +70 | °C |

## Electrical Characteristics

$V_{DD}$ = 2.4 to 3.6V, $V_{SS}$ = 0V, Ta = –20 to +70°C unless otherwise noted.

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply voltage | $V_{DD}$ | | 2.4 | 3.0 | 3.6 | V |
| Maximum operating current consumption[1] | $I_{DDM}$ | $V_{DD}$ = 3.0V, Ta = 25°C, no input signal, PON: VSS, OUT: no load | – | 65 | 100 | µA |
| Operating current consumption[1] | $I_{DDT}$ | $V_{DD}$ = 3.0V, Ta = 25°C, 0.1mVrms input amplitude (differential input), 500ms pulsewidth, PON: VSS, OUT: no load | – | 55 | – | µA |
| Standby mode current consumption | $I_{ST}$ | $V_{DD}$ = $V_{DDA}$ = 3.6V, PON, FCN, HLDN: OPEN, OUT: no load | – | – | 0.1 | µA |
| Minimum input voltage range | $V_{fmin}$ | IN1–IN2 differential input, $f_{IN}$ = 40kHz, 60kHz, Ta = 25°C | – | 0.5 | 1.0 | µVrms |
| Maximum input voltage range | $V_{fmax}$ | IN1–IN2 differential input, $f_{IN}$ = 40kHz, 60kHz | 80 | – | – | mVrms |
| Input frequency | $f_{IN}$ | IN1–IN2 differential input | 35 | – | 80 | kHz |
| Analog switch resistance | $R_A$ | $V_{IN2}$ = 0V, $V_{IN3}$ = 50mV | – | – | 15 | Ω |
| Startup time[2] | $t_{ON}$ | When supply is applied | – | – | 8 | sec |
| Startup time[2] (PON) | $t_{PON}$ | From standby mode | – | – | 8 | sec |
| Input voltage | $V_{IL}$ | PON, FCN, HLDN pins | – | – | 0.5 | V |
| | $V_{IH}$ | | $V_{DD}$–0.5 | – | – | V |
| Input current | $I_{IL}$ | $V_{IL}$ = 0V, PON, FCN, HLDN pins | – | –0.5 | –1.5 | µA |
| | $I_{IH}$ | $V_{IH}$ = $V_{DD}$ , PON, FCN, HLDN pins | – | – | 1 | µA |
| LOW-level output current | $I_{OL}$ | OUT pin, $V_{OL}$ = $V_{SS}$ + 0.5V | 10 | – | – | µA |
| HIGH-level output current | $I_{OH}$ | OUT pin, $V_{OH}$ = $V_{DD}$ − 0.5V | –10 | – | – | µA |
| Gain hold time | $t_{HLD}$ | ± 3dB change | 1 | – | – | sec |
| Fall time output propagation delay[3] | $t_{DN}$ | $f_{IN}$ = 40kHz, 60kHz, Ta = 25°C, $V_{IN}$ = 1µVrms to 80mVrms, NPC standard crystal, NPC standard jig | – | – | 160 | ms |
| Rise time output propagation delay[3] | $t_{UP}$ | | – | – | 200 | ms |
| LOW-level output pulsewidth[4] (200ms) | $T_{200}$ | | 100 | 200 | 300 | ms |
| LOW-level output pulsewidth[4] (500ms) | $T_{500}$ | | 400 | 500 | 650 | ms |
| LOW-level output pulsewidth[4] (800ms) | $T_{800}$ | | 700 | 800 | 900 | ms |
| Noise rejection ratio[5] | S/N | | – | – | 9 | dB |

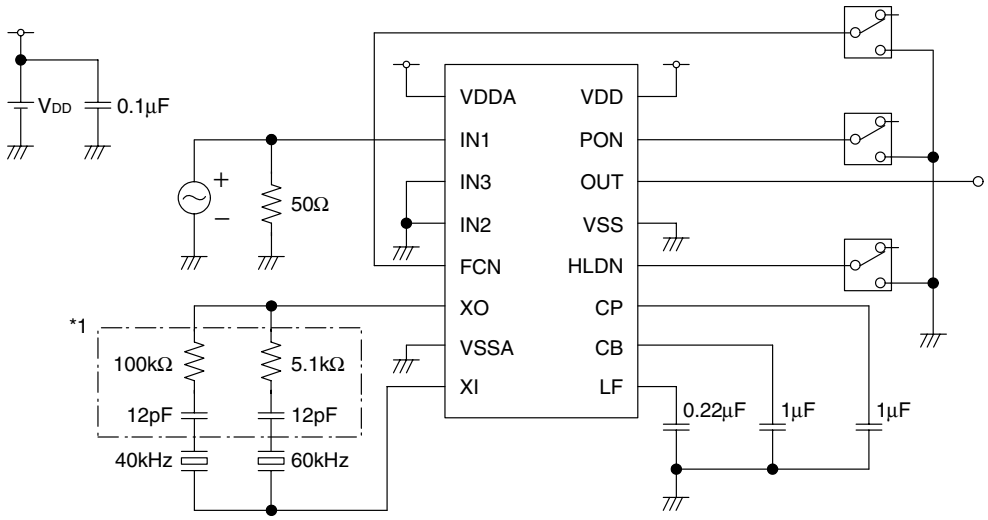
1. Measured using the standard circuit.
2. The time taken under stable wave input conditions from when power is applied or standby is released, using PON, until stable digital output occurs within ratings.
3. The time taken, with 10:1 input signal amplitude ratio and 500ms pulsewidth, from when a change in signal input amplitude occurs until the output OUT changes. Note that this characteristic is very dependent on the antenna and crystal filter characteristics. The standard crystal used for crystal filter by our measurement has the following equivalent circuit coefficients as reference values.




| f [kHz] | L1 [kH] | C1 [fF] | R1 [kΩ] | C0 [pF] |
|---|---|---|---|---|
| 40 | 6.70280 | 2.36228 | 11.4492 | 1.42773 |
| 60 | 5.17396 | 1.36007 | 13.4826 | 1.04927 |

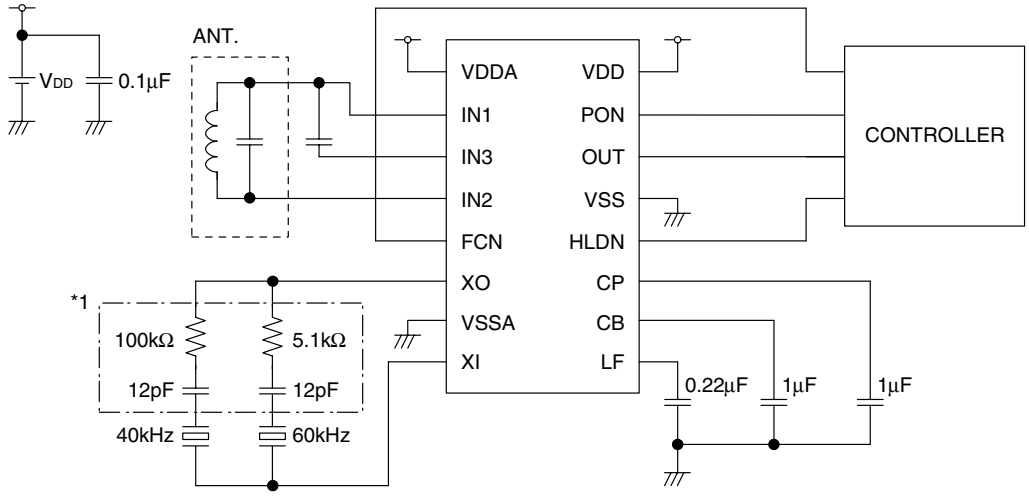
4. Values obtained when using the crystal filter employed here. Note that these values are dependent on the crystal characteristics, and should be considered as reference values.
5. Time averaged rms values, where the noise is white noise and the measurement bandwidth is determined by the crystal filter equivalent used in the standard circuit. Note that this value is very dependent on the crystal filter characteristics used.

## STANDARD CIRCUIT




*1. These values are obtained when using NPC's standard crystal and should be considered as reference values.
In case of using different crystal, the values are different.

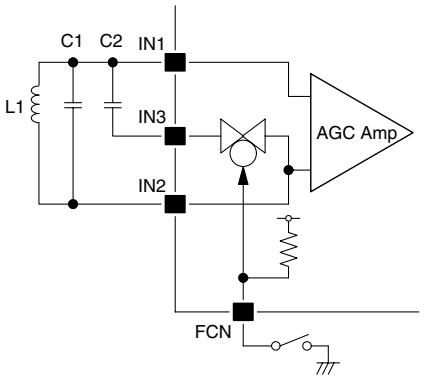
## APPLICATION CIRCUIT




*1. These values are obtained when using NPC's standard crystal and should be considered as reference values.
In case of using different crystal, the values are different.

# FUNCTIONAL DESCRIPTION

## Antenna Input and Tuning Capacitor Switching Function




There are three antenna inputs: IN1, IN2, and IN3. When FCN is open (or HIGH), the internal analog switch is OFF and IN1–IN2 are the antenna inputs (60kHz mode). When FCN is LOW, the analog switch is ON, connecting IN3 and IN2. C2 is then connected in parallel to C1 in the tuning circuit, reducing the resonant frequency (40kHz mode).

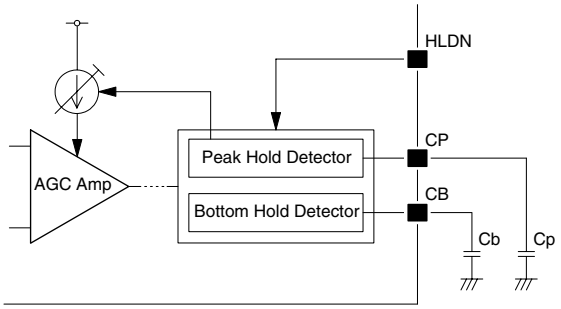
| FCN | Analog switch | Antenna input | Tuning capacitor | Receiver frequency |
|---|---|---|---|---|
| Open or HIGH | OFF | Between IN1 and IN2 | C1 | 60kHz |
| LOW | ON | Between IN1 and IN2, IN3 | C1 + C2 parallel | 40kHz |

FCN should be left open if not using the tuning capacitor switching function, and IN2 should be connected to IN3 externally.

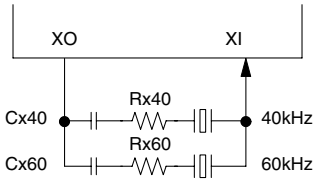
## AGC Amplifier and Gain Hold Function

The input voltage from the antenna is amplified by the AGC amplifier. The gain can be monitored by the voltage on pin CP, and can be changed by varying the CP voltage. An external capacitor Cp can be connected to CP to stabilize the voltage, but the gain tracking time is dependent on the capacitance. When HLDN is open (or HIGH), the gain automatically adjusts to follow the post-amplifier detector signal. When HLDN is LOW, the immediately preceding gain is held for an interval determined by the Cp capacitance.

| HLDN | Gain tracking |
|---|---|
| Open or HIGH | Auto tracking |
| LOW | Gain held fixed |



## Crystal Filter Circuit

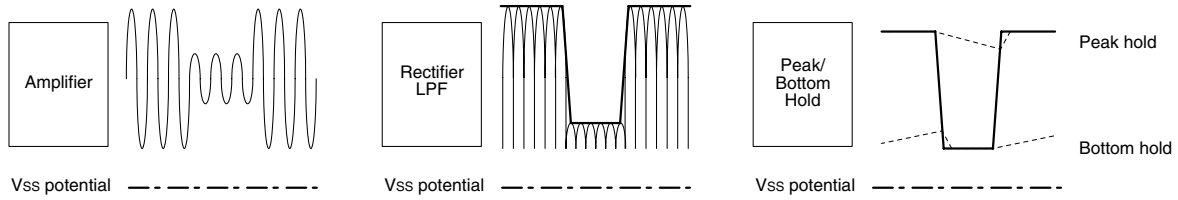



Recommended goods(Crystal filter)
DAISHINKU CORP. : DT-261
Resonance frequency : 40.000kHz/60.000kHz
Load capacitance : 12.5pF±25ppm

External crystals are used as filters. Multiple frequencies (40kHz and 60kHz) are supported by connecting crystals in parallel. The center frequency and bandwidth of the filters is determined by the crystal characteristics. If the center frequency is lower than the target frequency, C×40 and C×60 can be added to change the resonant frequency. And R×40 and R×60 can be added to adjust the filter Q factor. Internally, pin XO is linked to pin XI by a phase-inverted signal passed through a capacitor, which cancels the high-frequency components that pass through the crystal parallel capacitances.

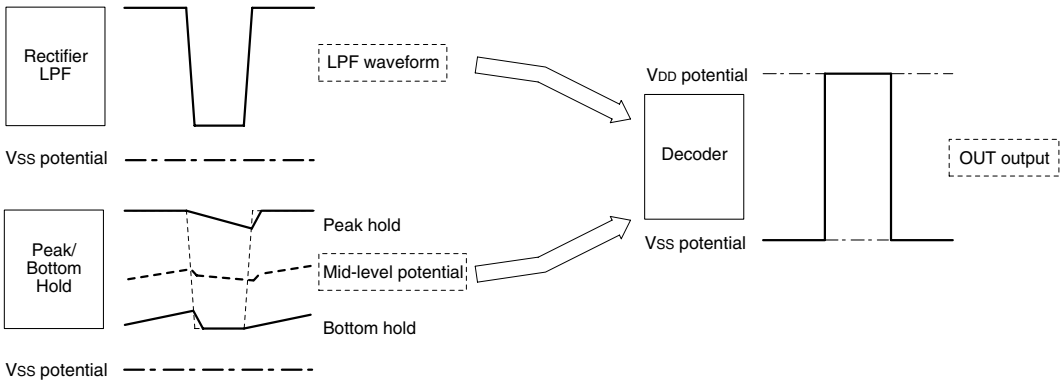
## Detector Circuit

The amplified signal is full-wave rectified and passed through a lowpass filter detector. The detector output is input to peak hold (pin CP) and bottom hold (pin CB) circuits to form the decoder reference potentials and peak hold potential for AGC control.




## Decoder Circuit

The detector output and peak/bottom hold mid-level potential reference are used to decode the time code signal, which is output on pin OUT. The output is active-LOW, so that the output is LOW when the input amplitude is HIGH.




## Standby Function

When PON is open (or HIGH), the device is in standby mode and the current consumption is reduced. Receiver operation starts when PON goes LOW.

| PON | Mode | OUT |
|---|---|---|
| Op (HIGH) | Standby | HIGH |
| LOW | Operating | Time code |

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