SM8580AM
Real-time Clock IC with 4-bit Interface and Built-in Temperature Sensor

OVERVIEW

The SM8580AM is a real-time clock IC based on a 32.768kHz crystal oscillator, which features a 4-bit parallel interface for communication with an external microcontroller. It comprises second-counter to year-counter clock and calendar circuits that feature automatic leap-year adjustment up to year 2099, alarm and timer interrupt functions, clock counter change detect functions, ±30-second correction function, time error correction function, and built-in temperature sensor. The 4-bit parallel interface is compatible with general-purpose SRAM over a high-speed bus.

FEATURES

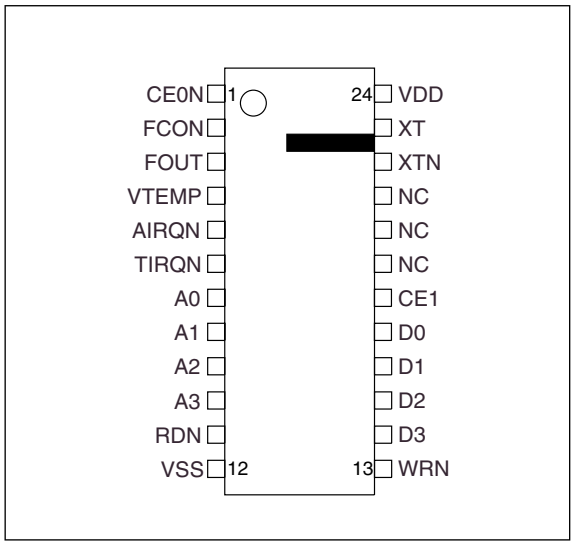
- High-speed bus 4-bit parallel interface
- Date, day, hour, minute, and second-counter presettable alarm interrupt
- 1/4096 seconds to 255 minutes presettable interval timer interrupt function
- 2 software-maskable alarm and timer interrupt outputs
- Clock counter change detect functions
- 4-digit western calendar display
- Automatic leap year correction up to year 2099
- ±30-second adjust function
- −195 to +192ppm time error correction range
- Built-in temperature sensor (analog voltage output)
- 2.4 to 5.5V interface voltage range
- 1.6 to 5.5V clock voltage range
- 0.6μA/3V (typ) current consumption

ORDERING INFORMATION

Device	Package
SM8580AM	24-pin SSOP

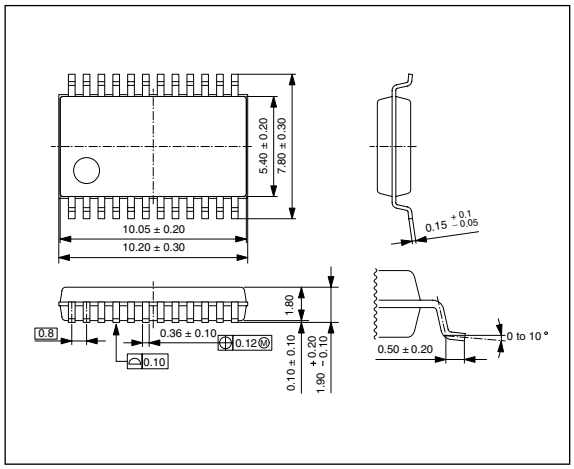
PINOUT

(Top view)

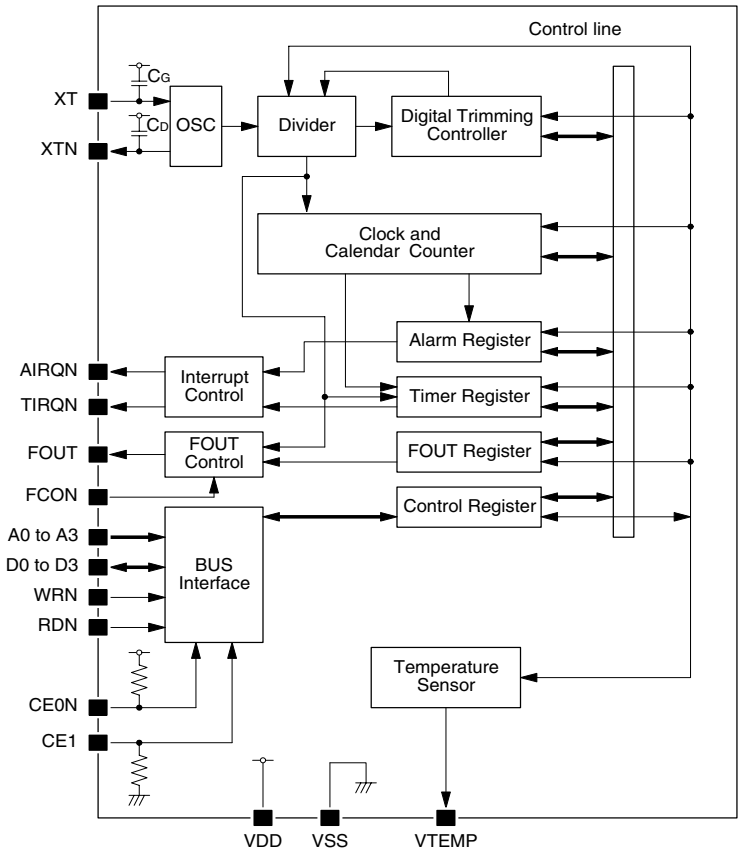


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Function[1]
1	CE0N	I	Chip enable 0 input with built-in pull-up resistor. The SM8580AM can be accessed when CE0N is LOW and CE1 is HIGH.
2	FCON	I	FOUT output frequency select control input (when CE1 is HIGH). 32.768kHz fixed frequency output when FCON is LOW. Output frequency determined by bit FD when FCON is HIGH (when FE bit is 1). Note that a HIGH-level voltage should be applied to FCON to avoid unwanted 32.768kHz output during backup.
3	FOUT	O	Frequency set register, frequency output (CMOS output)
4	VTEMP	O	Temperature voltage output (analog output)
5	AIRQN	O	Alarm interrupt output (N-channel open-drain output)
6	TIRQN	O	Timer interrupt output (N-channel open-drain output)
7	A0	I	Address inputs. Connect to the microcontroller address bus. The selected register address is input on this bus when accessing the SM8580AM (positive logic).
8	A1	I	
9	A2	I	
10	A3	I	
11	RDN	I	Read strobe input. Data can be read from SM8580AM when RDN is LOW and WRN is HIGH. An error will occur if both RDN and WRN are simultaneously LOW.
12	VSS	–	Ground
13	WRN	I	Write strobe input. Data can be written to SM8580AM when RDN is HIGH and WRN is LOW. An error will occur if both RDN and WRN are simultaneously LOW.
14	D3	I/O	Data bus input/outputs. Connect to the microcontroller data bus.
15	D2	I/O	
16	D1	I/O	
17	D0	I/O	
18	CE1	I	Chip enable 1 input with built-in pull-down resistor. The SM8580AM can be accessed when CE0N is LOW and CE1 is HIGH. FOUT is in output mode when CE1 is HIGH, regardless of the state of CE0N. FOUT is high impedance when CE1 is LOW.
19	NC	–	No connection
20	NC	–	No connection
21	NC	–	No connection
22	XTN	O	Oscillator output, with built-in oscillator capacitance C_D
23	XT	I	Oscillator output, with built-in oscillator capacitance C_G
24	VDD	–	Supply

1. Connect a 0.1µF capacitor between VDD and VSS.

FOUT Output and SM8580AM Access Relationship

CE0N	CE1	FCON	FE bit	FOUT output	SM8580AM accessible
HIGH	LOW	×	×	High impedance	No
LOW	LOW	×	×	High impedance	No
HIGH	HIGH	LOW	0	32.768kHz output	No
		LOW	1	32.768kHz output	No
		HIGH	0	High impedance	No
		HIGH	1	FD bit select frequency output	No
LOW	HIGH	LOW	0	32.768kHz output	Yes
		LOW	1	32.768kHz output	Yes
		HIGH	0	High impedance	Yes
		HIGH	1	FD bit select frequency output	Yes

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0V$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.3 to 7.0	V
Input voltage range	V_{IN}	All inputs, D0 to D3	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT1}	TIRQN, AIRQN	V_{SS} – 0.3 to 8.0	V
	V_{OUT2}	FOUT, D0 to D3, VTEMP	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}		–55 to 125	°C

Recommended Operating Conditions

$V_{SS} = 0V$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		2.4 to 5.5	V
Clock supply voltage range	V_{CLK}		1.6 to 5.5	V
Operating temperature range	T_{opr}		–40 to 85	°C

DC Electrical Characteristics

V_{SS} = 0V, V_{DD} = 1.6 to 5.5V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Current consumption 1	I_{DD1}	V_{DD} = 5V	CE0N = RDN = WRN = V_{DD}, A0 to A3 = D0 to D3 = V_{DD} or V_{SS}, CE1 = FCON = V_{SS}, AIRQN = TIRQN = FOUT = V_{DD}, VTEMP output OFF (TEMP bit = 0)	–	1.0	2.0	µA
Current consumption 2	I_{DD2}	V_{DD} = 3V		–	0.6	1.0	µA
Current consumption 3	I_{DD3}	V_{DD} = 5V	Ta = 25°C, CE0N = RDN = WRN = V_{DD}, A0 to A3 = D0 to D3 = V_{DD} or V_{SS}, CE1 = FCON = V_{SS}, AIRQN = TIRQN = FOUT = V_{DD}, VTEMP output ON (TEMP bit = 1)	–	50	75	µA
Current consumption 4	I_{DD4}	V_{DD} = 3V		–	40	60	µA
Current consumption 5	I_{DD5}	V_{DD} = 5V	CE0N = CE1 = RDN = WRN = V_{DD}, A0 to A3 = D0 to D3 = V_{SS}, FCON = V_{SS}, AIRQN = TIRQN = FOUT = VTEMP = Hi-Z, VTEMP output OFF (TEMP bit = 0), FOUT = 32kHz output, C_L = 0pF	–	3.0	7.5	µA
Current consumption 6	I_{DD6}	V_{DD} = 3V		–	1.7	4.5	µA
Current consumption 7	I_{DD7}	V_{DD} = 5V	CE0N = CE1 = RDN = WRN = V_{DD}, A0 to A3 = D0 to D3 = V_{SS}, FCON = V_{SS}, AIRQN = TIRQN = FOUT = VTEMP = Hi-Z, VTEMP output OFF (TEMP bit = 0), FOUT = 32kHz output, C_L = 30pF	–	8.0	20	µA
Current consumption 8	I_{DD8}	V_{DD} = 3V		–	5.0	12	µA
HIGH-level input voltage 1	V_{IH1}	V_{DD} = 4.5 to 5.5V, CE0N, FCON, RDN, WRN, A0 to A3, D0 to D3		2.2	–	V_{DD} + 0.3	V
LOW-level input voltage 1	V_{IL1}			V_{SS} – 0.3	–	0.8	V
HIGH-level input voltage 2	V_{IH2}	V_{DD} = 2.4 to 3.6V, CE0N, FCON, RDN, WRN, A0 to A3, D0 to D3		0.8V_{DD}	–	V_{DD} + 0.3	V
LOW-level input voltage 2	V_{IL2}			V_{SS} – 0.3	–	0.2V_{DD}	V
HIGH-level input voltage 3	V_{IH3}	V_{DD} = 1.6 to 5.5V, CE1		0.8V_{DD}	–	V_{DD} + 0.3	V
LOW-level input voltage 3	V_{IL3}			V_{SS} – 0.3	–	0.2V_{DD}	V
Input leakage current	I_{LEAK}	CE0N = V_{DD}, CE1 = V_{SS}, FCON = RDN = WRN = A0 to A3 = V_{DD} or V_{SS}		–0.5	–	0.5	µA
Pull-up resistance 1	R_{UP1}	V_{DD} = 5V	CE0N = V_{SS}	75	150	300	kΩ
Pull-up resistance 2	R_{UP2}	V_{DD} = 3V		150	300	600	kΩ
Pull-down resistance 1	R_{DWN1}	V_{DD} = 5V	CE1 = V_{DD}	20	40	80	MΩ
Pull-down resistance 2	R_{DWN2}	V_{DD} = 3V		42.5	85	170	MΩ
Pull-down resistance 3	R_{DWN3}	V_{DD} = 5V	CE1 = 0.5V	30	60	120	kΩ
Pull-down resistance 4	R_{DWN4}	V_{DD} = 3V		55	110	220	kΩ
HIGH-level output voltage 1	V_{OH1}	V_{DD} = 5V	I_{OH} = –1mA, D0 to D3, FOUT	4.5	–	5.0	V
HIGH-level output voltage 2	V_{OH2}	V_{DD} = 3V		2.0	–	3.0	V
HIGH-level output voltage 3	V_{OH3}	V_{DD} = 3V	I_{OH} = –100µA, D0 to D3, FOUT	2.9	–	3.0	V
LOW-level output voltage 1	V_{OL1}	V_{DD} = 5V	I_{OL} = 1mA, D0 to D3, FOUT	0	–	0.5	V
LOW-level output voltage 2	V_{OL2}	V_{DD} = 3V		0	–	0.8	V
LOW-level output voltage 3	V_{OL3}	V_{DD} = 3V	I_{OL} = 100µA, D0 to D3, FOUT	0	–	0.1	V
LOW-level output voltage 4	V_{OL4}	V_{DD} = 5V	I_{OL} = 1mA, AIRQN, TIRQN	0	–	0.25	V
LOW-level output voltage 5	V_{OL5}	V_{DD} = 3V		0	–	0.4	V
Output leakage current	I_{OZ}	D0 to D3, AIRQN, TIRQN, FOUT, V_{OUT} = V_{DD} or V_{SS}		–0.5	–	0.5	µA

Terminal Capacitance Characteristics

Ta = 25°C, f = 1MHz

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Address input capacitance	C_{ADD}	A0 to A3	–	–	8	pF
Data output capacitance	C_{DATA}	D0 to D3	–	–	15	pF

Oscillator Characteristics

Ta = 25°C, NPC's standard crystal (C_I = 30kΩ, C_L = 10pF) unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator start time	t_{STA}	V_{DD} = 1.6 V	–	–	3.0	s
Oscillator stop voltage	V_{STO}		–	–	1.5	V
Frequency voltage characteristic	f/V	V_{DD} = 1.6 to 5.5V	–2	–	+2	ppm/V
Frequency accuracy	ε_{IC}	V_{DD} = 3.0V	–20	–	+20	ppm
Input capacitance	C_G	V_{DD} = 3.0V	–	15	–	pF
Output capacitance	C_D	V_{DD} = 3.0V	–	10	–	pF

AC Characteristics (1)

V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	max	min	
FOUT duty	Duty	V_{DD} = 5V ± 10%	40	–	60	%
		V_{DD} = 3V ± 10%	40	–	60	%
Oscillator failure detection time	t_{OSC}	V_{DD} = 5V ± 10%	10	–	–	ms
		V_{DD} = 3V ± 10%	10	–	–	ms

AC Characteristics (2)

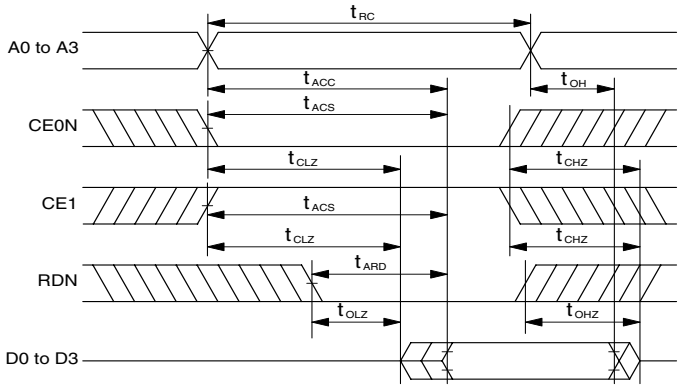
V_{DD} = 2.4 to 3.6V, V_{SS} = 0V, Ta = –40 to 85°C, inputs $V_I = 0.5V_{DD}$, outputs $V_O = 0.5V_{DD}$, output load capacitance C_L = 100pF (t_{ACC}, t_{ACS}, t_{ARD})

Parameter	Symbol	Rating		Unit
		min	max	
Read cycle time	t_{RC}	150	–	ns
Address access time	t_{ACC}	–	150	ns
CE access time	t_{ACS}	–	150	ns
RD access time	t_{ARD}	–	100	ns
CE output set time	t_{CLZ}	5	–	ns
CE output floating	t_{CHZ}	–	60	ns
RD output set time	t_{OLZ}	5	–	ns
RD output floating	t_{OHZ}	–	60	ns
Output hold time	t_{OH}	10	–	ns
Write cycle time	t_{WC}	150	–	ns
Chip select time	t_{CW}	140	–	ns
Address valid to end-of-write	t_{AW}	140	–	ns
Address setup time	t_{AS}	0	–	ns
Address hold time	t_{WR}	0	–	ns
Write pulsewidth	t_{WP}	130	–	ns
Input data set time	t_{DW}	80	–	ns
Input data hold time	t_{DH}	0	–	ns

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C, inputs $V_I = 0.5V_{DD}$, outputs $V_O = 0.5V_{DD}$, output load capacitance C_L = 100pF (t_{ACC}, t_{ACS}, t_{ARD})

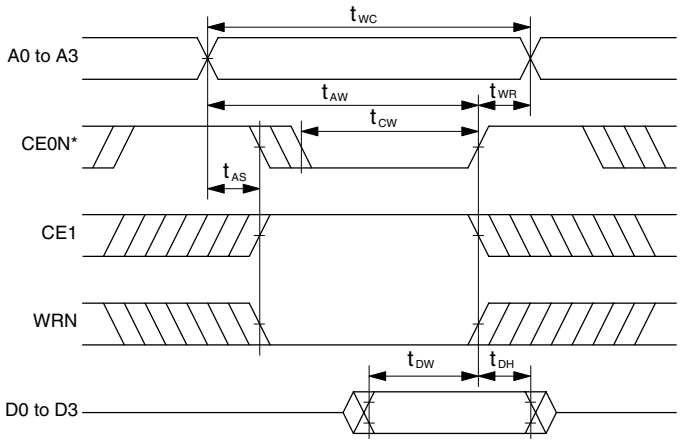
Parameter	Symbol	Rating		Unit
		min	max	
Read cycle time	t_{RC}	85	–	ns
Address access time	t_{ACC}	–	85	ns
CE access time	t_{ACS}	–	85	ns
RD access time	t_{ARD}	–	45	ns
CE output set time	t_{CLZ}	3	–	ns
CE output floating	t_{CHZ}	–	30	ns
RD output set time	t_{OLZ}	3	–	ns
RD output floating	t_{OHZ}	–	30	ns
Output hold time	t_{OH}	5	–	ns
Write cycle time	t_{WC}	85	–	ns
Chip select time	t_{CW}	70	–	ns
Address valid to end-of-write	t_{AW}	70	–	ns
Address setup time	t_{AS}	0	–	ns
Address hold time	t_{WR}	0	–	ns
Write pulsewidth	t_{WP}	65	–	ns
Input data set time	t_{DW}	35	–	ns
Input data hold time	t_{DH}	0	–	ns

Data read

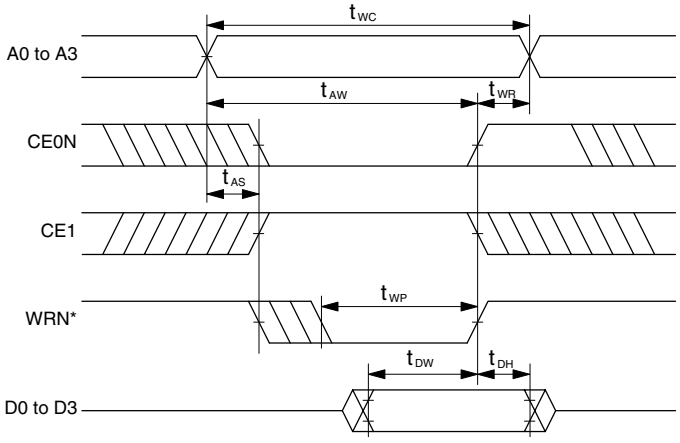


Data write

CE control



WR control



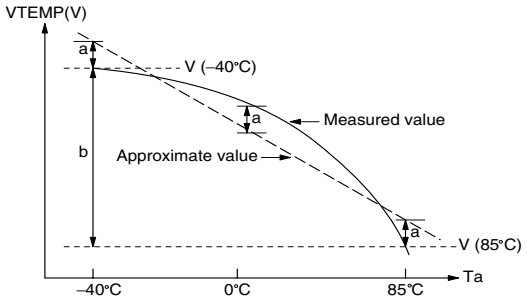
*: When writing data, CE0N or WRN should be held HIGH level while the address changes.

Temperature Sensor

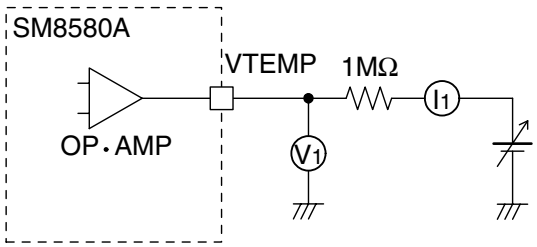
V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	max	min	
Temperature sensor output voltage	V_{OUT}	Ta = 25°C, VSS reference output voltage, V_{DD} = 2.7 to 5.5V, VTEMP	–	1.470	–	V
Output accuracy	T_{ACR}	Ta = 25°C	–	–	±5	°C
Temperature sensitivity[1]	V_{SE}	–40°C ≤ Ta ≤ 85°C, V_{DD} = 2.7 to 5.5V	–7.3	–7.8	–8.3	mV/°C
Linearity[2]	ΔNL	–40°C ≤ Ta ≤ 85°C, V_{DD} = 2.7 to 5.5V	–	–	±2.0	%
Temperature detection range	T_{OPR}	ΔNL ≤ ±2.0%, V_{DD} = 2.7 to 5.5V	–40	–	85	°C
Output resistance[3]	R_O	Ta = 25°C, V_{DD} = 2.7 to 5.5V, VTEMP	–	1.0	3.0	kΩ
Output load capacitance	C_L	V_{DD} = 2.7 to 5.5V	–	–	100	pF
Output load resistance	R_L	V_{DD} = 2.7 to 5.5V	500	–	–	kΩ
Response time	t_{RSP}	V_{DD} = 3.0V, R_L = 500kΩ, C_L = 100pF	–	–	200	µs

1. Temperature sensitivity V_{SE} = (V(85°C) – V(–40°C)) ÷ 125 [mV/°C]
2. Linearity ΔNL = a ÷ b × 100 [%], where
   a = maximum deviation between the measured value and the approximated value of VTEMP, and
   b = difference between the measured values at temperatures of –40 and 85°C



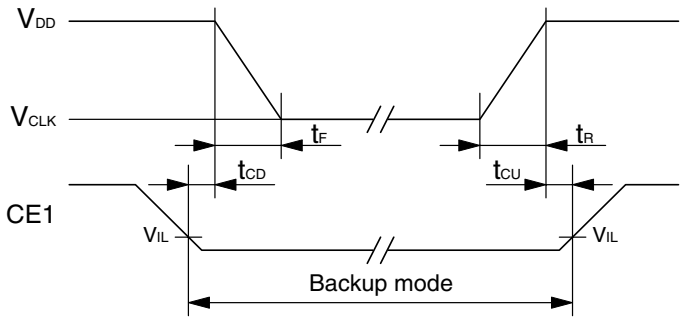
3. Output resistance R_O = $\Delta V_1 \div \Delta I_1$ [Ω]



Backup Transfer and Return

Parameter[1]	Symbol	Condition	Rating			Unit
			min	max	min	
Supply voltage falling edge CE setup time	t_{CD}		0	–	–	µs
Supply voltage fall time	t_F	$(V_{DD} - V_{CLK}) \leq 2.0V$	2	–	–	µs/V
		$(V_{DD} - V_{CLK}) > 2.0V$	50	–	–	µs/V
Supply voltage rise time	t_R		1	–	–	µs/V
Supply voltage rising edge CE hold time	t_{CU}		0	–	–	µs

1. Before switching the supply, confirm that the chip enable CE1 is LOW and that SM8580AM is deselected.



FUNCTIONAL DESCRIPTION

Register Tables

Bank 0 (clock, calendar registers)

Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
0	Second registers	8	4	2	1
1		FOS	40	20	10
2	Minute registers	8	4	2	1
3		#	40	20	10
4	Hour registers	8	4	2	1
5		#	#	20	10
6	Day of week register	#	4	2	1
7	Date registers	8	4	2	1
8		#	#	20	10
9	Month registers	8	4	2	1
A		#	#	#	10
B	Year registers	8	4	2	1
C		80	40	20	10
D		800	400	200	100
E		TEST	TEMP	2000	1000
F	Control register	Bank SEL1	Bank SEL0	STOP	BUSY/ ADJ

Bank 1 (alarm, FOUT registers)

Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
0	Second registers	8	4	2	1
1		AE	40	20	10
2	Minute registers	8	4	2	1
3		AE	40	20	10
4	Hour registers	8	4	2	1
5		AE	*	20	10
6	Day of week register	AE	4	2	1
7	Date registers	8	4	2	1
8		AE	*	20	10
9	–	*	*	*	*
A	–	*	*	*	*
B	CE1 control	CTEMP	CDT_ON	*	*
C	FOUT divider set register	#	FD2	FD1	FD0
D	FOUT frequency set register	FE	#	FD4	FD3
E	Alarm control	TEST	TEMP	AF	AIE
F	Control register	Bank SEL1	Bank SEL0	STOP	BUSY/ ADJ

Bank 2 (digital correction, timer registers)

Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
0	Digital correction registers	DT3	DT2	DT1	DT0
1		DT_ON	DT6	DT5	DT4
2	–	#	#	#	#
3	–	#	#	#	#
4	Timer counter set registers	8	4	2	1
5		128	64	32	16
6	Timer counter output registers	8	4	2	1
7		128	64	32	16
8	Timer setting	TE	TI/TP	TD1	TD0
9	–	#	#	#	#
A	–	#	#	#	#
B	–	*	*	*	*
C	–	*	*	*	*
D	–	*	*	*	*
E	Timer control	TEST	TEMP	TF	TIE
F	Control register	Bank SEL1	Bank SEL0	STOP	BUSY/ ADJ

- All bits in register F and bits 2 to 3 in register E are common to all register banks.
- When alarm interrupts are not used, registers 0 to 8 in bank 1 can be used as RAM (total 36 bits).
- When timer interrupts are not used, registers 4 to 5 in bank 2 can be used as RAM (total 8 bits).
- When digital correction is not used, registers 0 to 1 in bank 2 can be used as RAM, excluding bit 3 (DT_ON) in register 1 (total 7 bits).
- The BUSY/ADJ bit function is BUSY when reading, and ADJ when writing.
- The BUSY flag is set to 1 an interval of 244µs before clock counter update timing.
- Registers 6 and 7 in bank 2 are read-only registers, and cannot be written to.
- When power is applied, all register bits are undefined, with the exception of bits FOS, TEST and TEMP. Accordingly, these bits need to be initialized. TEST and TEMP are automatically reset to 0 and FOS is automatically reset to 1 when power is applied.
- Bits marked # are all read-only bits fixed to 0. These bits cannot be written to.
- Bits marked * can be used as RAM bits.

Control Registers (All Banks, Register E (bits 2, 3) and F)

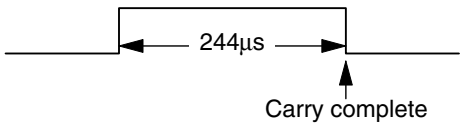
Bank	Address	Bit 3	Bit 2	Bit 1	Bit 0
0, 1, 2	E	TEST	TEMP		
	F	Bank SEL1	Bank SEL0	STOP	BUSY/ADJ

- TEST bit
  Factory test bit.
  This bit should be set to 0. Take care when writing to other E register bits not to accidentally write 1 to the TEST bit. Automatically resets to 0 when power (VDD) is applied.
- TEMP bit
  When set to 1, it enables the temperature sensor voltage output on pin VTEMP. When set to 0, VTEMP is high impedance. Automatically resets to 0 when power is applied.
- Bank SEL bits
  Bank select bits for read/write operations.

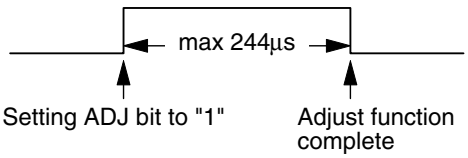
Bank SEL1	Bank SEL0	Accessed bank
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 1

- STOP bit
  When set to 1, the clock 32Hz frequency divider counter stops and is reset. When set to 0, the clock restarts.
- BUSY/ADJ bit
  This bit functions as a BUSY function in read mode, and as an ADJ function in write mode.
  - ADJ function (±30 seconds adjust bit)
    The following processes are operated when a logic 1 is written to ADJ, however a logic 0 cannot be written to.
    Second registers are reset to 00 and minute registers not incremented when the clock counter is reset and the second registers are currently 00 to 29.
    Second registers are reset to 00 and minute registers are incremented when the clock counter is reset and the second registers are currently 30 to 59.
    The ADJ bit is automatically reset to 0 a maximum of 244µs after it is set to 1.
  - BUSY function (second registers increment or ±30 seconds adjust busy indicator bit)
    When BUSY is 1, the counters are being updated (incremented or reset). To read or write to clock and calendar registers, the BUSY flag has to be 0. If reading data when BUSY is set to 1, there is a possibility that incorrect (intermediate) data will be output.
    BUSY is set to 1 under the following two circumstances.

Normal seconds digit carry



±30 seconds digit adjust (when ADJ is set to 1)



■ Function operation table

Bit		Function			
STOP	**ADJ**	**Clock**	**Timer**	**Alarm**	**FOUT**
0	0	Operating	Operating[3]	Operating	Operating[7]
0	1	Adjust[1]	Operating[4]	Operating[6]	Operating[8]
1	0	Stopped	Operating/stopped[5]	Stopped	Operating/stopped[9]
1	1	Stopped/adjust[2]	Operating/stopped[5]	Stopped	Operating/stopped[9]

1. ±30 seconds adjust function
2. The clock stops, and the ±30 seconds adjust function operates.
3. If the timer source clock frequency is ≤ 1Hz, the timer cycle changes when the digital correction function is used.
   If the timer source clock frequency is ≥ 64Hz, the timer cycle is not affected when the digital correction function is used.
4. If the timer source clock frequency is ≤ 1Hz, the timer cycle changes.
   If the timer source clock frequency is ≥ 64Hz, the timer cycle does not change.
5. If the timer source clock frequency is ≤ 1Hz, the timer is stopped.
   If the timer source clock frequency is ≥ 64Hz, the timer operates.
6. An alarm interrupt is not generated by the 30-second adjust function (ADJ) even if all other alarm conditions are met.
   However, an alarm interrupt is generated 1 second later if the alarm conditions are still met.
7. If the FOUT source clock frequency is ≤ 1Hz, the cycle changes when the digital correction function is used.
   If the FOUT source clock frequency is ≥ 32Hz, the cycle is not affected when the digital correction function is used.
8. If the FOUT source clock frequency is ≤ 1Hz, the cycle changes.
   If the FOUT source clock frequency is ≥ 32Hz, the cycle does not change.
9. If the FOUT source clock frequency is ≤ 1Hz, the timer is stopped.
   If the FOUT source clock frequency is ≥ 32Hz, the timer operates.

Clock and Calendar Registers (Bank 0, Registers 0 to E)

Clock counters (registers 0 to 5)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
0	0	Second registers	8	4	2	1
	1		FOS	40	20	10
	2	Minute registers	8	4	2	1
	3			40	20	10
	4	Hour registers	8	4	2	1
	5				20	10

- Data in these registers is interpreted in BCD format. For example, if the seconds registers 1 and 0 contain 0101 1001, then the contents are interpreted as the value 59 seconds.
- Hour register contents are values expressed in 24-hour mode.

FOS (oscillator failed detect bit (register 1, bit 3))

- The FOS bit is the oscillator failure flag. It indicates that the oscillator has stopped due to supply voltage reduction during operation. It is set to 1 when the oscillator stops, and remains 1 until reset by writing 0 to FOS. It is not affected by the function of other bits. A 1 is written to FOS when power is applied.

Day-of-week counter (register 6)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
0	6	Day of week register		4	2	1

- The day-of-week register contains values representing the day of the week as shown in the following table.

Bit 2	Bit 1	Bit 0	Weekday
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

Calendar registers (registers 7 to E)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
0	7	Date registers	8	4	2	1
	8				20	10
	9	Month registers	8	4	2	1
	A					10
	B	Year registers	8	4	2	1
	C		80	40	20	10
	D		800	400	200	100
	E		TEST	TEMP	2000	1000

- Registers B to E are 4 digits forming the western calendar year.
- Leap-year adjustment is automatic for years 1901 to 2099.

Alarm Registers (Bank 1, Registers 0 to 8, E)

Alarm control register (register E)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
1	E	Alarm control			AF	AIE

- AF bit (alarm flag)
  The AF bit is set to 1 when an alarm event is occurred, when the settings in the alarm set registers (bank 1, registers 0 to 8) match the settings in the day, clock and calendar registers (bank 0, registers 0 to 8). A logic 0 cannot be written to AF for 1µs maximum after AF is set to 1. The AF bit remains 1 until reset by writing 0 to AF. A logic 1 cannot be written to AF.
- AIE bit (alarm interrupt enable)
  This bit enables the output on AIRQN when an alarm interrupt is occurred. If the AIE is not set to 1, then no output occurs even if the AF bit is set to 1. The AIRQN output is high impedance when AIE is set to 0.

Alarm set registers (registers 0 to 8)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
1	0	Second registers	8	4	2	1
	1		AE	40	20	10
	2	Minute registers	8	4	2	1
	3		AE	40	20	10
	4	Hour registers	8	4	2	1
	5		AE	*	20	10
	6	Day of week register	AE	4	2	1
	7	Date registers	8	4	2	1
	8		AE	*	20	10

- These registers set the alarm time and date.
- When the corresponding bank 0 registers match these bank 1 registers, an alarm event occurs and AIRQN goes LOW if AIE is set to 1.
- An alarm can be set for date, day-of-week, hour, minute, and second. Each of these have a corresponding AE (alarm enable) bit which allows easy combination to create alarm events every second, every minute, hourly, daily, and weekly alarms.
- Note that alarms cannot be set for multiple days within the same week (such as an alarm on Mondays and Fridays only).
- When an AE bit is set to 0, the relevant register and corresponding bank 0 register are compared. When an AE bit is set to 1, the data is disregarded and all bits considered as “don’t care” bits.

Day-of-week alarm bits (register 6)

- The day-of-week register contains values representing the day of the week as shown in the following table.

Bit 2	Bit 1	Bit 0	Weekday
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

Timer Registers (Bank 2, Registers 4 to 8, E)

Timer control registers (registers 8, E)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
2	8	Timer setting	TE	TI/TP		
	E	Timer control			TF	TIE

- TE bit (timer enable)
  Timer countdown stop/start control bit.
  When set to 1, the timer starts counting down. When set to 0 during countdown, the timer stops.
- TF bit (timer flag)
  The timer flag is set to 1 when the timer counter counts down to zero, occurring a timer event. A logic 0 cannot be written to TF for 1µs maximum after TF is set to 1. It is held at 1 until 0 is written to this bit. A 1 cannot be written to TF.
- TIE bit (timer interrupt enable)
  This bit enables the timer interrupt output on TIRQN when a timer event is occurred. If the TIE is not set to 1, then no output occurs even if the TF bit is set to 1. The TIRQN output is high impedance when TIE is set to 0.
- TI/TP bit (level/periodic interrupt mode select bit)
  Sets the timer interrupt signal output mode.
  The SM8580AM supports two timer function modes.
  - TI/TP = 0 (level interrupt mode)
    When a timer interrupt is occurred, TIRQN goes LOW (if TIE = 1) and TF is set to 1. TIRQN remains LOW and TF is held at 1 until a 0 is written to the TF bit.
    The timer operates by counting down until the data is zero, then the TE bit is cleared and the count stops automatically. However, if the timer is started when the TF bit is 1, then the TE bit is not cleared. The timer count register contents remain zero after the count down stops.
  - TI/TP = 1 (periodic interrupt mode)
    When a timer interrupt is occurred, TIRQN goes LOW (if TIE = 1) and TF is set to 1. TIRQN subsequently goes high impedance after a fixed interval, but TF is held at 1 until a 0 is written to the TF bit.
    The timer operates by counting down until the data is zero, then the timer register data is reloaded automatically after a fixed interval, and the countdown restarts. This mode can be used as a repetitive interval timer.

Timer source clock set register (register 8)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
2	8	Timer setting			TD1	TD0

- The register 8 bits 0 and 1 set the timer source clock to one of four frequencies listed in the following table.

TD1	TD0	Timer source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz (1 minute)

Timer counter set registers (registers 4 to 7)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
2	4	Timer counter set registers	8	4	2	1
	5		128	64	32	16
	6	Timer counter output registers	8	4	2	1
	7		128	64	32	16

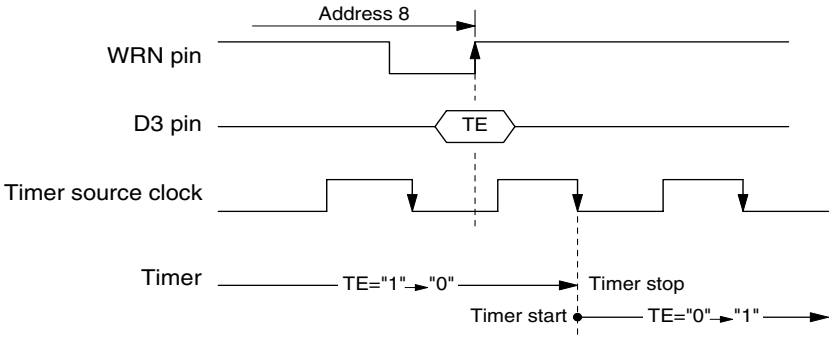
- Registers 4 and 5 set an 8-bit presettable binary down-counter value for the timer interrupt function.
- The value of the count can be determined by reading the values of registers 6 and 7 during the count.
- The presettable binary down-counter is updated when the data is written to registers 4 and 5.
- The data written to registers 4 and 5 are stored and are not changed until replacement data is written. This allows these bits to function as RAM bits if the timer interrupt mode is not used (when TIE = 0).
- When TE is set to 1, periodic interrupts are not output on TIRQN, even if registers 4 and 5 are set to zero.

Timer interrupt function example

Example of an hourly periodic timer interrupt

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
2	4	Timer counter set registers	1	1	0	0
	5		0	0	1	1
	8	Timer set register	TE	1	1	1
	E	Timer control	TEST	TEMP	TF	1

- The timer error, when the timer starts, is an interval of 0 to 1 cycles of the source clock selected during the first timer operation. Specifically, if the source clock is 1/60Hz (1 minute cycle) and with TE bit = 1 write timing, the maximum error that can occur is +60 seconds. Also, timer operations that last less than 1 source clock cycle are not normally counted.
- The timer count start timing in data write mode occurs on the first falling edge of the source clock after the WRN rising edge that sets the TE bit, shown in the timing diagram below. Also, when the timer is stopped by changing the setting of TE bit from 1 to 0, the count stops after the countdown operation a maximum of 1 clock cycle of the selected source clock later. Specifically, if the source clock is 1/60Hz (1 minute cycle) and with TE bit = 0 write timing, the timer count is decremented and the timing stops a maximum of 60 seconds later. At this point, there is a possibility that the timer count has decremented to zero and generated an interrupt. Therefore, if interrupts are not required, the TIE interrupt enable bit should be set to avoid unwanted interrupts from occurring.



CE1 Control Register (Bank 1, Register B)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
1	B	CE1 control	CTEMP	CDT_ON		

- This register determines whether the temperature sensor function and digital correction function in combination with the CE1 input pin. CTEMP determines the temperature sensor operation, and CDT_ON determines the digital correction function operation.
- CTEMP bit
  When CTEMP is set to 0, the temperature sensor operates only when the CE1 pin is HIGH.
  When CTEMP is set to 1, the temperature sensor operates without any relationship to the CE1 input state.
  Note that the temperature sensor operation also depends on the bank 2 TEMP bit to be active.
- CDT_ON bit
  When CDT_ON is set to 0, the digital correction function operates only when the CE1 pin is HIGH.
  When CDT_ON is set to 1, the digital correction function operates without any relationship to the CE1 input state.
  Note that the digital correction function also depends on the bank 2 DT_ON bit to be active.
- Function operation tables

CE1 pin	CTEMP bit	TEMP bit	Temperature sensor
×	×	0	Not operating
LOW	0	1	Not operating
HIGH	0	1	Operating
LOW	1	1	Operating
HIGH	1	1	Operating

CE1 pin	CDT_ON bit	DT_ON bit	Digital correction
×	×	0	Not operating
LOW	0	1	Not operating
HIGH	0	1	Operating
LOW	1	1	Operating
HIGH	1	1	Operating

Frequency Set Registers (Bank 1, Registers C, D)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
1	C	FOUT divider set register		FD2	FD1	FD0
	D	FOUT frequency set register	FE		FD4	FD3

■ FD3, FD4 bit
FOUT source clock frequency set bits.

FD4	FD3	Source clock
0	0	32768Hz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

■ FD0 to FD2 bits
Frequency divider set bits for the FOUT source clock set by FD3 and FD4.

FD2	FD1	FD0	Frequency divider ratio	FOUT output duty
0	0	0	1/1	1/2
0	0	1	1/2	1/2
0	1	0	1/3	1/3
0	1	1	1/6	1/2
1	0	0	1/5	1/5
1	0	1	1/10	1/2
1	1	0	1/15	1/3
1	1	1	1/30	1/2

■ FE bit
FOUT frequency signal set by FD0 to FD4 output enable bit.
When FCON is HIGH and FE is set to 1, then the frequency signal set by FD0 to FD4 is output on FOUT.
When FE is set to 0, the FOUT output is high impedance.
When FCON is LOW, a standard 32.768kHz signal is output on FOUT without reference to the settings in the C and D registers.

Digital Correction Registers (Bank 2, Registers 0, 1)

Bank	Address	Register	Bit 3	Bit 2	Bit 1	Bit 0
2	0	Digital correction registers	DT3	DT2	DT1	DT0
	1		DT_ON	DT6	DT5	DT4

- These registers enable and set the level of digital correction applied to oscillator clock. DT_ON enables the correction function, and bits DT0 to DT6 set the level of correction to be applied. This function adjusts the number of 1 second cycles which occur every 10 seconds.
- When digital correction is not used, a 0 should be written to DT_ON to disable correction.
- Correction range and resolution (correction range depends on the frequency)

Correction range	Correction resolution	Correction cycle
–195.20 to +192.15ppm	3.05ppm	10 seconds

- DT bits and digital correction (correction value depends on the frequency)

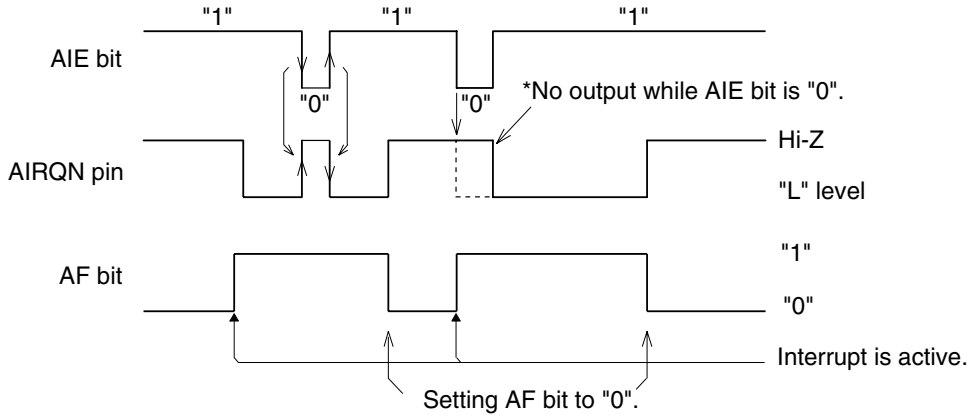
Digital correction bits							Correction (ppm)
DT6	DT5	DT4	DT3	DT2	DT1	DT0	
0	1	1	1	1	1	1	+192.15
0	1	1	1	1	1	0	+189.10
↓							↓
0	0	0	0	0	1	0	+6.10
0	0	0	0	0	0	1	+3.05
0	0	0	0	0	0	0	±0.00
1	1	1	1	1	1	1	–3.05
1	1	1	1	1	1	0	–6.10
↓							↓
1	0	0	0	0	0	1	–192.15
1	0	0	0	0	0	0	–195.20

- Correction value calculation
  - Positive correction (leading time)
    [DT6:0] = correction ÷ 3.05 (with decimal round-off)
    Example: for correction of 192.15ppm
    [DT6:0] = 192.15 ÷ 3.05 = $63_{10} = 0111111_2$
  - Negative correction (lagging time)
    [DT6:0] = 128 + correction ÷ 3.05 (with decimal round-off)
    Example: for correction of –158.6ppm
    [DT6:0] = 128 + (–158.6 ÷ 3.05) = $76_{10} = 1001100_2$

INTERRUPT OPERATION

Alarm Interrupt

When AIE is 1 and an alarm event occurs (AF bit is set to 1), AIRQN output goes LOW. If AIE is 0, however, AIRQN is in a high-impedance state. The alarm interrupt is output when a carry from the seconds register to the minute register occurs.

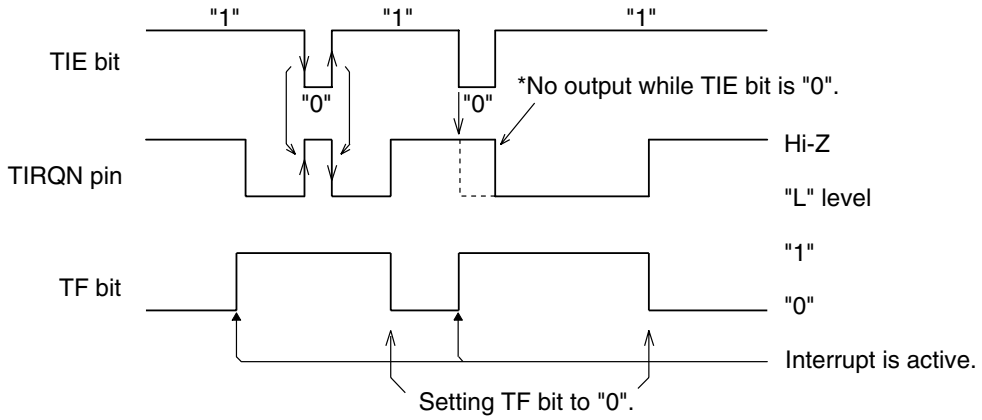


Timer Interrupt

The timer interrupt mode (level interrupt or periodic interrupt) is selected by the setting of TI/TP.

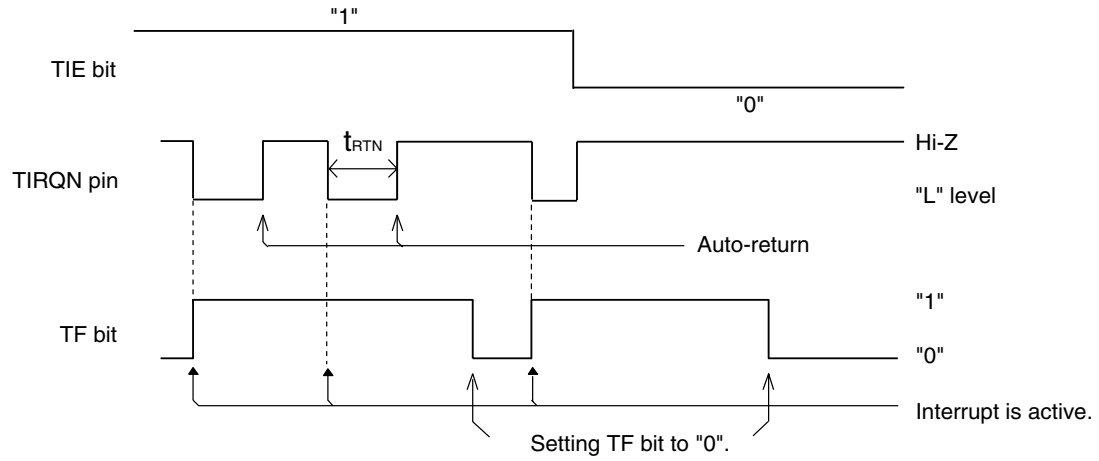
Level interrupt mode (TI/TP = 0)

When TIE is 1 and a timer interrupt event occurs (TF bit is set to 1), TIRQN goes LOW. When TIE is 0, however, TIRQN is in a high-impedance state.

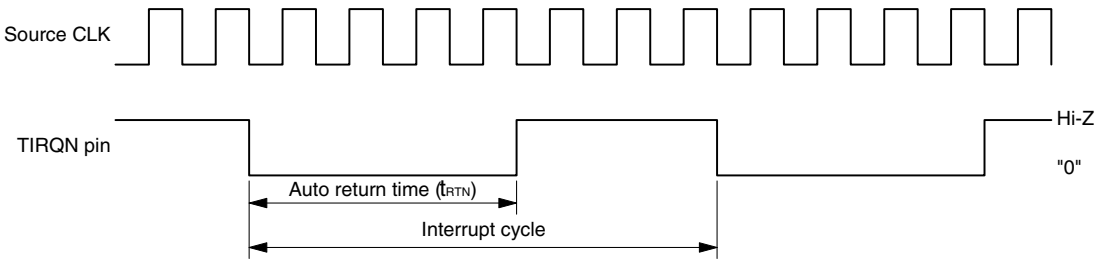


Periodic interrupt mode (TI/TP = 1)

When TIE is 1 and a timer interrupt event occurs (TF bit is set to 1), TIRQN goes LOW. If TIE is 0, however, TIRQN is in a high-impedance state, and the TF bit remains set to 1.



The auto-return time (t_{RTN}), shown in the following figure and table, is determined by the source clock frequency set by register 8 in bank 2 bits TD0 and TD1.



TD1	TD0	Source clock	Auto-return time (t_{RTN})
0	0	4096Hz	0.122ms
0	1	64Hz	7.81ms
1	0	1Hz	7.81ms
1	1	1/60Hz	7.81ms

APPLICATION NOTES

Setting the Alarm

Alarms can be set for day, weekday, hour, minute, and second. However, it is not possible to set an alarm for more than one weekday.

Note that it is recommended that AF and AIE be set to 0 at the same time to avoid accidental hardware interrupts while setting the alarm. After the alarm data is entered, initialization occurs when AF is again set to 0.

If the interrupt output is not used by setting AIE set to 0, an alarm can still be controlled by software monitoring of the AF bit.

Example 1

To set an alarm for 6pm of the following day:

- Set bits AIE and AF to 0.
- Set the day register AE bit to 1.
- Acquire the current weekday setting from bank 0 register 6, add 1 to the current value (except in the case of Saturday), and write the updated data. Note that the day following 6_H (Saturday) is 0_H (Sunday).
- Write 18_H to the hour alarm register.
- Write 00_H to the minute alarm register.
- Write 00_H to the seconds alarm register.
- Set bit AF to 0.
- Set bit AIE to 1.

Example 2

To set an alarm for 6am on every for Sunday:

- Set bits AIE and AF to 0.
- Set the day alarm register AE bit to 1.
- Write 0_H to the weekday alarm register.
- Write 06_H to the hour alarm register.
- Write 00_H to the minute alarm register.
- Write 00_H to the seconds alarm register.
- Set bit AF to 0.
- Set bit AIE to 1.

Using the Temperature Sensor

The SM8580AM temperature sensor can be used to monitor the surrounding temperature. The temperature sensor information can then be used to adjust the clock for any temperature variations in the oscillator frequency which affect the accuracy of the clock. One method of utilizing the temperature sensor to adjust timing errors is by using the clock error correction function (digital correction), as described below.

1. Based on the known temperature characteristics of the oscillator crystal, store temperature correction values for various temperatures in an external non-volatile EEPROM.
2. Use an A/D converter, such as in a general-purpose CPU, to convert the VTEMP temperature sensor output voltage into a digital value.
3. Use the digital value of the current temperature to access the temperature correction data stored in the EEPROM, and then write the corresponding data into the digital correction registers.

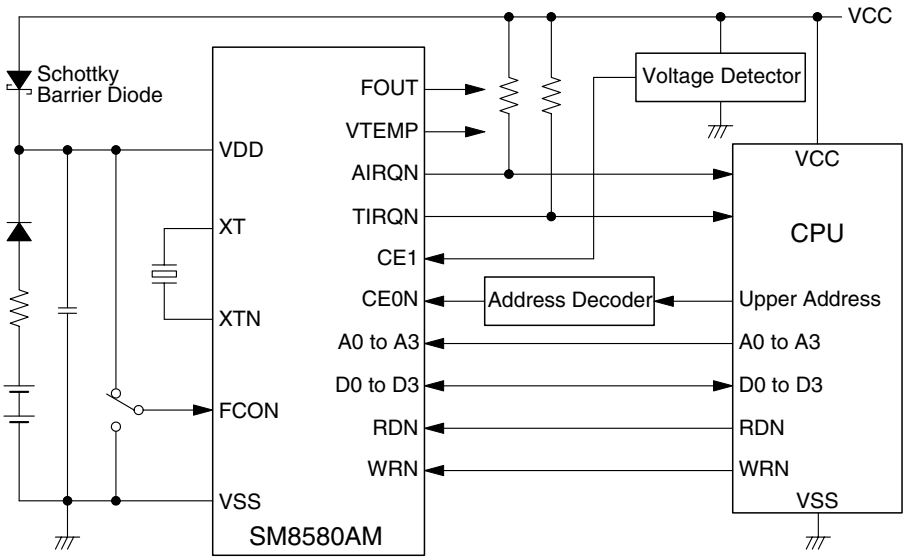
This procedure is useful in implementing a high-accuracy clock function.

Monitoring Digital Correction

Using the test mode allows the 64Hz digital correction clock to be output on pin FOUT. The test mode works as follows.

1. Apply a HIGH-level on FCON.
2. Set the FOUT frequency set register FE bit to 1.
3. Set the CE1 control register CDT_ON bit to 1.
4. Set correction data in the digital correction register DT0 to DT6 bits, and then set DT_ON to 1.
5. Set the bank 2 register C, bit 1 to 1.
6. When CE0N is LOW and CE1 is HIGH and the test mode set register TEST bit is set to 1, the digital correction cycle changes from 10 seconds to 1/64 seconds, and the clock output on FOUT is the 64Hz clock after timing correction. The output is the corrected timing for the set digital correction value corresponding to a 64Hz clock × 64[ppm]. Measuring this output provides a quick method for monitoring the digital correction function.
7. When CE0N goes HIGH, the TEST bit is reset to 1 and test mode is released.

TYPICAL APPLICATION CIRCUIT



Note. Because all the circuit components, except the crystal unit, are built in the SM8580AM chip, the oscillation circuit is realized just by the connection of the 32.768kHz crystal unit between XT and XTN terminals. The digital correction function is used to adjust the accuracy of clock time.

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