SM5320A

5-channel Video Buffer with Built-in wideband LPF

OVERVIEW

The SM5320A is a 5-channel video buffer with built-in 5th-order lowpass filters. The HD block lowpass filter cutoff frequency range can adjust from 4.10MHz to 42.7MHz*1 by 256 steps. The lowpass filter supports 480i to 1080i format, video signal equipment analog input/outputs. For video input systems, the device functions as a next-stage ADC system anti-aliasing filter. For video output systems, the filter reduces video DAC aliasing and external noise and can drive up to 300Ω terminating resistance. The cutoff frequency and signal input type can be controlled using an I²C-BUS*2, and the I²C slave address can be set by ADS (3-state input) to allow up to three SM5320A on the same bus. The output gain can be varied in the range of 0dB ± 2.1dB (max step: 0.15dB) for each Y/C block and HD block individually using the I²C-BUS.

*1. When the resistor connected to ISET (R_{ISET}) is 1.8kΩ.
*2. I²C-BUS is a registered trademark of NXP B.V.

FEATURES

- Supply voltages
  - Analog: 4.75 to 5.25V
  - Digital: 3.0 to 5.5V
- Lowpass filter with adjustable cutoff frequency (256 steps) (CH-1 to CH-3)
  - Cutoff frequency range: 4.10MHz to 42.7MHz (R_{ISET} = 1.8kΩ)
- Filter bypass mode function for display specifications up to SXGA resolution (CH-1 to CH-3)
  - Passband: 80MHz (typ)
- Half fc mode switch function suitable for component signals (CH-2, CH-3)
- Video input pins can be independently set to sync-tip clamp/bias inputs (CH-1 to CH-3)
- Filter passband (± 1.5dB): 6MHz (CH-Y/C)
- Up to 300Ω terminating resistance drive capability
- Output gain: 0dB ± 2.1dB (max step: 0.15dB)
- Power-down function
  - ≤ 500µA current consumption when power-down
- I²C-BUS interface control
  - Slave address: 48h, 49h, or 4Ah (up to three devices can be used simultaneously, selected by ADS input)
  - Data transfer rate: Fast mode (up to 400kbit/s)
- Operating ambient temperature range: 0 to 70°C
- Package: 28-pin VSOP

APPLICATIONS

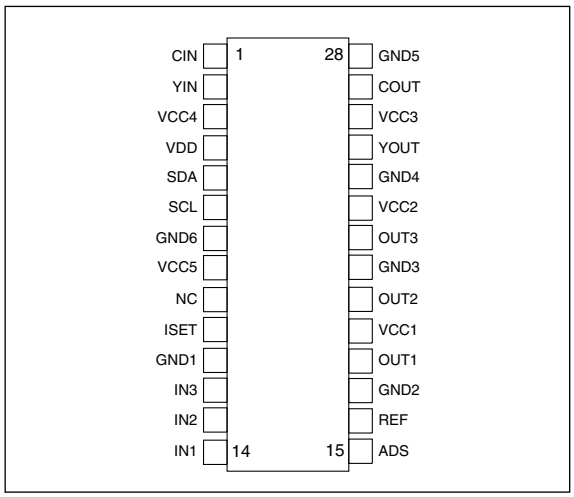
- HDTVs
- LCD TVs
- PDPs
- Projectors

ORDERING INFORMATION

Device	Package
SM5320AV	28-pin VSOP

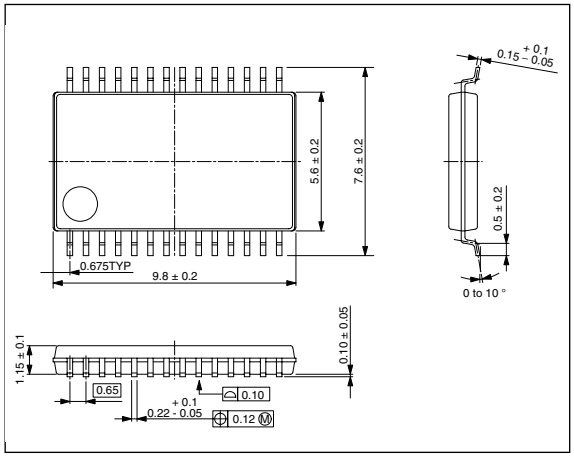
PINOUT

(Top view)

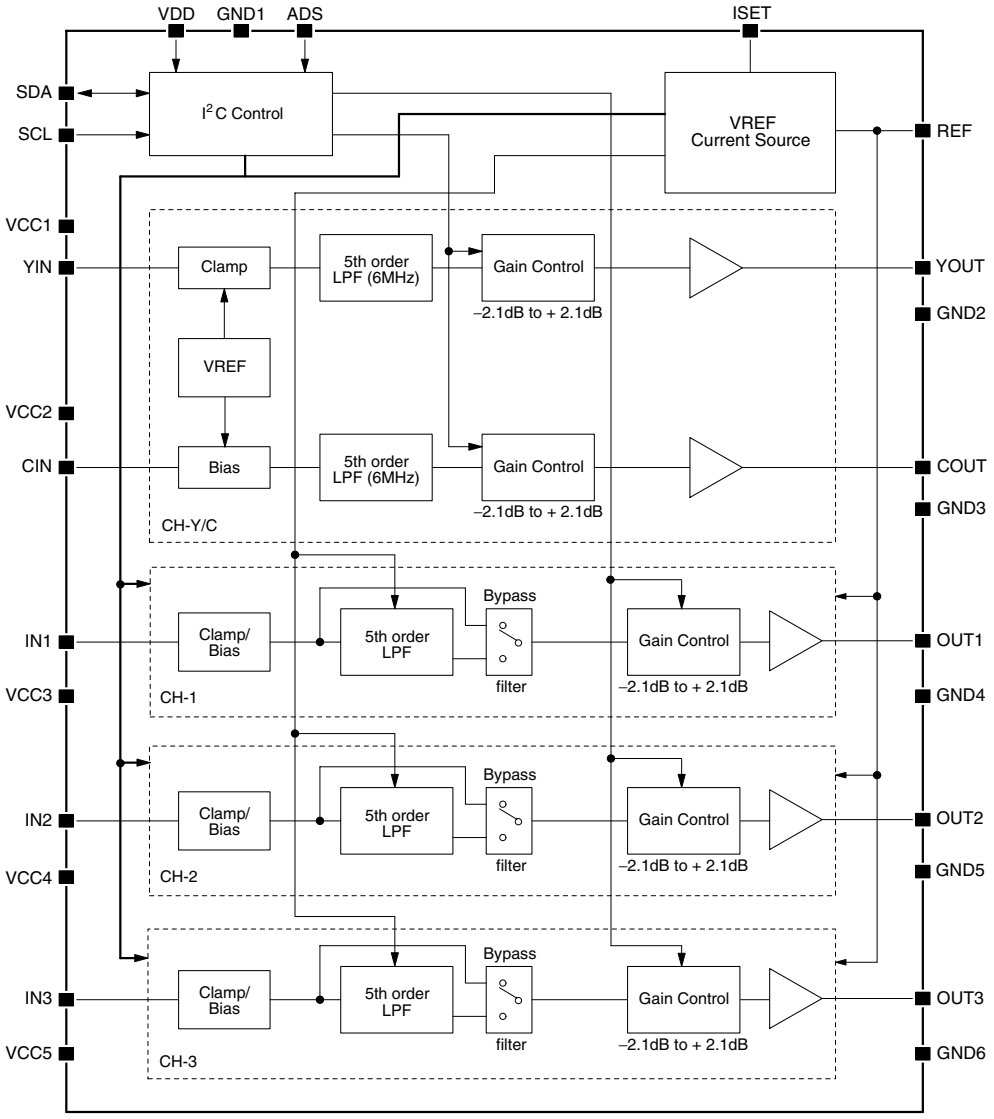


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



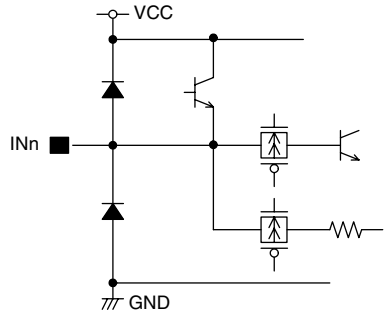
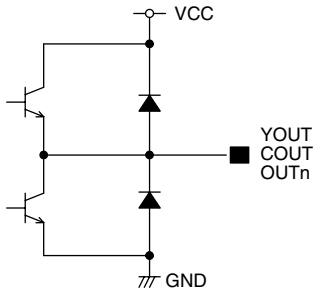
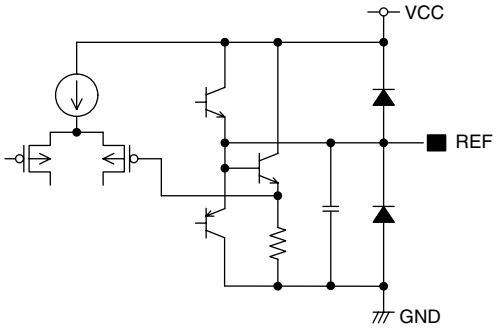
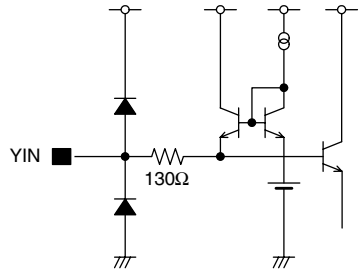
Note. The recommended value of the external resistor (R_{ISET}) connected to ISET is 1.8kΩ.

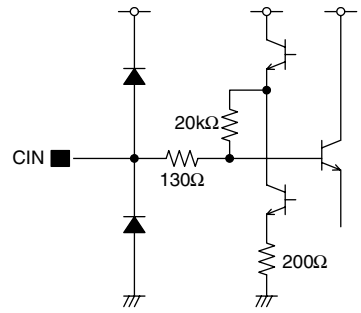
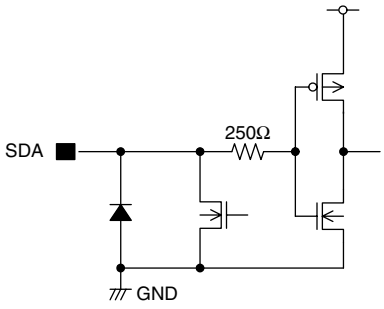
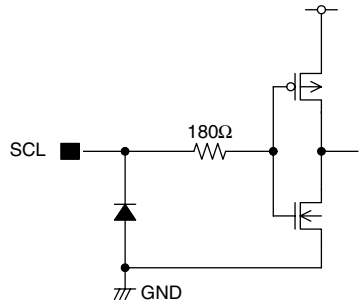
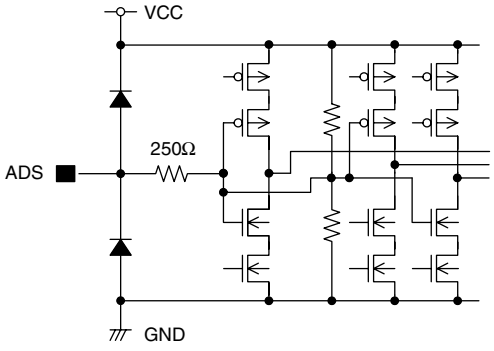
PIN DESCRIPTION

Number	Name	I/O*1	A/D*2	Description
1	CIN	I	A	Video signal input (C)
2	YIN	I	A	Video signal input (Y)
3	VCC4	–	A	Analog supply 4
4	VDD	–	D	Digital supply
5	SDA	I/O	D	I^2C data signal input/output
6	SCL	I	D	I^2C clock signal input
7	GND6	–	A	Ground 6
8	VCC5	–	A	Analog supply 5
9	NC	–	–	No connection
10	ISET	–	A	Internal current-setting resistor (R_{ISET}) connection (standard 1.8kΩ)
11	GND1	–	A	Ground 1
12	IN3	I	A	Video signal input (CH-3)
13	IN2	I	A	Video signal input (CH-2)
14	IN1	I	A	Video signal input (CH-1)
15	ADS	I	D	I^2C slave address select (3-state input)
16	REF	O	A	Internal reference voltage
17	GND2	–	A	Ground (Y/C block)
18	OUT1	O	A	Video signal output (CH-1)
19	VCC1	–	A	Analog supply 1
20	OUT2	O	A	Video signal output (CH-2)
21	GND3	–	A	Ground 3
22	OUT3	O	A	Video signal output (CH-3)
23	VCC2	–	A	Analog supply 2
24	GND4	–	A	Ground 4
25	YOUT	O	A	Video signal output (Y)
26	VCC3	–	A	Analog supply 3
27	COUT	O	A	Video signal output (C)
28	GND5	–	A	Ground 5

*1. I: input, O: output
*2. A: analog, D: digital

PIN EQUIVALENT CIRCUITS

Number	Name	I/O*1	Equivalent circuit
14 13 12	IN1 IN2 IN3	I	
25 27 18 20 22	YOUT COUT OUT1 OUT2 OUT3	O	
16	REF	O	
2	YIN	I	

Number	Name	I/O*1	Equivalent circuit
1	CIN	I	
5	SDA	I/O	
6	SCL	I	
15	ADS	I	

*1. I: input, O: output

Note. Resistance values in the equivalent circuits indicate design values.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = GND1 = GND2 = GND3 = GND4 = GND5 = GND = 0V, VCC1 = VCC2 = VCC3 = VCC4 = VCC5 = VDD = V_{CC}

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	VCC1, VCC2, VCC3, VCC4, VCC5, VDD	– 0.3 to 7.0	V
Input voltage	V_{IN}	ADS, SDA, SCL, INn (n = 1, 2, 3)	GND – 0.3 to V_{CC} + 0.3	V
Storage temperature range	T_{STG}		– 55 to + 125	°C
Power dissipation*1	P_D		1.2	W
Junction temperature*1	T_J		125	°C

*1. Ta = 80°C, when mounted on NPC's regulation substrate (112 × 80 × 1.6mm double layer glass-epoxy substrate with 180% wiring factor)

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1	V_{CC}	VCC1, VCC2, VCC3, VCC4, VCC5	4.75 to 5.25	V
Supply voltage difference	ΔV_{CC}	Difference between VCC1 to VCC5 pin each	± 0.1	V
Supply voltage 2	V_{DD}	VDD	3.0 to 5.5	V
Operating ambient temperature	Ta		0 to 70	°C

Note. VCC1 to VCC5 should be applied simultaneously.

Electrical Characteristics

DC Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, GS1 = 04h, GS2 = 04h, R_L = 300Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

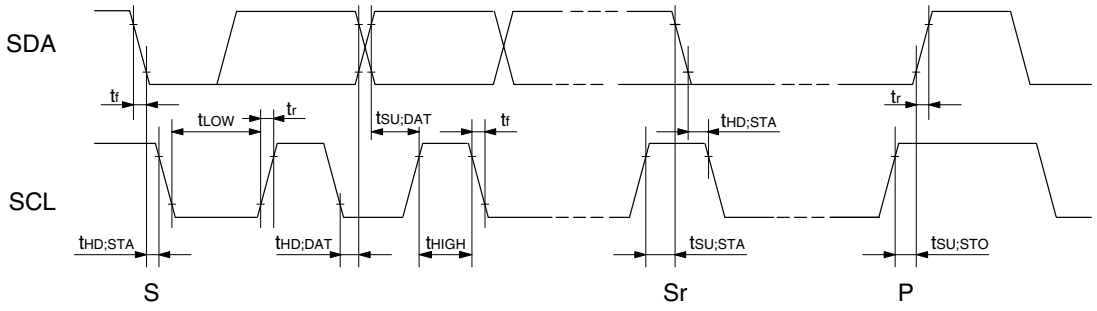
Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Current consumption 1*1	I_{CC1}	Filter mode, FCDATA = 255	–	110	150	mA	I
Current consumption 2*1	I_{CC2}	Filter bypass mode	–	75	100	mA	I
Current consumption 3*1	I_{CC3}	Power-down mode	–	–	500	µA	I
HIGH-level input voltage	V_{IH1}	SDA, SCL	0.7 V_{DD}	–	–	V	I
LOW-level Input voltage	V_{IL1}	SDA, SCL	–	–	0.3 V_{DD}	V	I
ADS HIGH-level input voltage	V_{IH2}	ADS	0.8 V_{CC}	–	–	V	I
ADS LOW-level input voltage	V_{IL2}	ADS	–	–	0.2 V_{CC}	V	I
ADS open-circuit input voltage	V_{OPEN}	ADS	$V_{CC}/2$ – 0.2	–	$V_{CC}/2$ + 0.2	V	I
LOW-level input leakage current	I_{LL}	SDA, SCL, V_{IN} = 0V	–	–	1.0	µA	I
HIGH-level input leakage current	I_{LH}	SDA, SCL, V_{IN} = V_{DD}	–	–	1.0	µA	I
SDA output voltage	V_{OL}	SDA = LOW output, Sink current = 3mA	0	–	0.4	V	I

*1. Total of current consumption of VCC1, VCC2, VCC3, VCC4, VCC5 and VDD, when no input signals.

AC Characteristics (I^2C-BUS)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
SCL clock frequency	f_{SCL}		0	–	400	kHz	II
SCL hold time (start condition)	$t_{HD;STA}$		0.6	–	–	µs	II
SCL clock LOW-level pulsewidth	t_{LOW}		1.3	–	–	µs	II
SCL clock HIGH-level pulsewidth	t_{HIGH}		0.6	–	–	µs	II
SCL setup time (start condition)	$t_{SU;STA}$		0.6	–	–	µs	II
SDA data hold time	$t_{HD;DAT}$		0	–	0.9	µs	II
SDA data setup time	$t_{SU;DAT}$		100	–	–	ns	II
SDA, SCL rise time	t_r		–	–	300	ns	II
SDA, SCL fall time	t_f		–	–	300	ns	II
SCL setup time (stop condition)	$t_{SU;STO}$		0.6	–	–	µs	II
SDA, SCL input capacitance	C_i		–	–	10	pF	II



Note. S, Sr: start condition, P: stop condition

Analog Characteristics

Analog input characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, GS1 = 04h, GS2 = 04h, R_L = 300Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Clamp voltage 1	V_{CLMP1}	Clamp input, no signal input, IN1, IN2, IN3	1.80	2.00	2.20	V	I
Clamp voltage 2	V_{CLMP2}	No signal input, YIN	1.45	1.65	1.85	V	I
Bias voltage 1	V_{BIAS1}	Bias input, no signal input, IN1, IN2, IN3	2.25	2.45	2.65	V	I
Bias voltage 2	V_{BIAS2}	No signal input, CIN	2.10	2.30	2.50	V	I
Input resistance	R_{BIAS}	Bias input, IN1, IN2, IN3, CIN	–	20	–	kΩ	II
Input voltage (CH-1, CH-2, CH-3)*1	V_{AI1}	THD < 1.0%, IN1, IN2, IN3	–	–	1.4	Vp-p	I
Input voltage (Y)*1	V_{AI2}	THD < 1.5%, YIN	–	–	1.4	Vp-p	I
Input voltage (C)*1	V_{AI3}	THD < 1.5%, CIN	–	–	1.0	Vp-p	I
Crosstalk between channels	X_{TLK}	fin = 1MHz, between each channel	–	70	–	dB	II

*1. This item represents values of maximum input signal amplitude in which the output distortion rate shown in the condition column is filled. When the signal amplitude that exceeds this specification value is input, the output distortion rate is deteriorated. When using this device, the input signal level should be set not to exceed the standard value of the signal amplitude.

Filter and filter bypass mode frequency characteristics (CH-1, CH-2, CH-3)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, GS1 = 04h, R_L = 300Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Cutoff frequency	F_{C1}	FCDATA = 0	–	4.10	–	MHz	II
	F_{C2}	FCDATA = 10	4.99	5.68	6.37	MHz	I
	F_{C3}	FCDATA = 227	31.0	35.3	39.6	MHz	I
	F_{C4}	FCDATA = 255	–	42.7	–	MHz	II
Half fc mode cutoff frequency ratio	R_{half1}	Half fc mode, FCDATA = 10	44	49	54	%	I
	R_{half2}	Half fc mode, FCDATA = 227	46	51	56	%	I
4fc attenuation	G_{SB}	fin ≥ 4fc, attenuation from fin = 100kHz	–	50	–	dB	II
Filter bypass mode passband*1	F_{BP}	Filter bypass mode, V_{IN} = 0.7Vp-p	74.25	80	–	MHz	II

*1. The passband that the attenuation from fin = 100kHz is ≤ 1dB. A_{VB} (F_{BP}) – A_{VB} (100kHz) ≥ –1dB

Frequency characteristics (CH-Y/C)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, GS2 = 04h, R_L = 300Ω, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			Min	Typ	Max		
Passband attenuation	F_{PB}	fin = 6MHz/100kHz	– 1.5	0	1.5	dB	I
Stopband attenuation	F_{SB}	fin= 27MHz/100kHz	30	40	–	dB	II
Group delay deviation	ΔT_{GD}	100kHz to 5MHz	–	10	–	ns	II

Output characteristics (CH-1, CH-2, CH-3)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, GS1 = 04h, R_L = 300Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Filter mode output gain 1	A_{VF1}	GS1 = 04h	– 0.5	0	0.5	dB	I
Filter mode output gain 2	A_{VF2}	GS1 = 20h	– 2.6	– 2.1	– 1.6	dB	I
Filter mode output gain 3	A_{VF3}	GS1 = 1Fh	1.6	2.1	2.6	dB	I
Filter mode gain step width	A_{VFstep}		–	–	0.15	dB	I
Filter bypass mode output gain 1	A_{VB1}	GS1 = 04h	– 0.5	0	0.5	dB	I
Filter bypass mode output gain 2	A_{VB2}	GS1 = 20h	– 2.6	– 2.1	– 1.6	dB	I
Filter bypass mode output gain 3	A_{VB3}	GS1 = 1Fh	1.6	2.1	2.6	dB	I
Filter bypass mode gain step width	A_{VBstep}		–	–	0.15	dB	I
Filter bypass mode gain error	dA_{VBP}	Gain error between filter mode and bypass mode	–	± 0.2	–	dB	I
Channel to channel gain error	dA_{VCH}		–	–	± 0.2	dB	I
Maximum output voltage	V_{out1}	THD < 1.0%	–	1.4	–	Vp-p	I
Output distortion	T_{HD1}	V_{IN} = 1.4Vp-p	–	0.2	1.0	%	I
Drive load resistance	R_L	1 load = 300Ω	–	–	1	load	I
I^2C response time	T_{IC}	Response time from ACK bit output when changing settings using I^2C-BUS	–	–	1	µs	II

Output characteristics (CH-Y/C)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, GS2 = 04h, R_L = 300Ω, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Output gain 1	A_{V1}	GS2 = 04h	– 0.5	0	0.5	dB	I
Output gain 2	A_{V2}	GS2 = 20h	– 2.6	– 2.1	– 1.6	dB	I
Output gain 3	A_{V3}	GS2 = 1Fh	1.6	2.1	2.6	dB	I
Output gain step width	A_{Vstep}		–	–	0.15	dB	I
Y to C gain error	dA_{VYC}		–	–	± 0.2	dB	I
Maximum output voltage (Y)	V_{out2}	YOUT, THD < 1.5%	–	1.4	–	Vp-p	I
Maximum output voltage (C)	V_{out3}	COUT, THD < 1.5%	–	1.0	–	Vp-p	I
Output distortion (Y)	T_{HD2}	YOUT, V_{IN} = 1.4Vp-p	–	0.2	1.5	%	I
Output distortion (C)	T_{HD3}	COUT, V_{IN} = 1.0Vp-p	–	0.2	1.5	%	I
Drive load resistance	R_L	1 load = 300Ω	–	–	1	load	I

Reference voltage characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
REF output voltage	V_R	REF	–	2.65	–	V	II

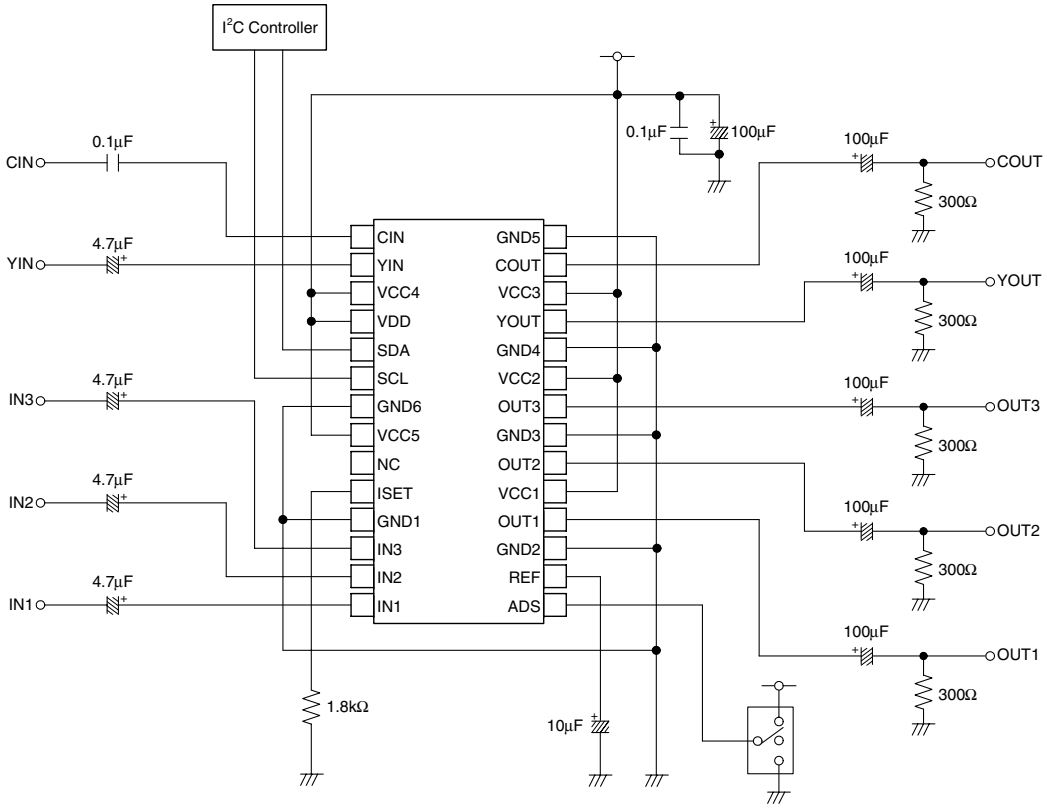
Test level

The definition of “Test Level” shown in the electrical characteristic table is as follows.

I : 100% of products tested at Ta = + 25°C.

II : Guaranteed as result of design and characteristics evaluation.

Evaluation Circuit Diagram



Note. This is a circuit only for the evaluation board of an electric characteristics. (It is not a recommended application circuit.)

FUNCTIONAL DESCRIPTION

I²C-BUS Control

The SM5320A uses an I²C-BUS interface to set the following functions.

1) Cutoff frequency (HD block)
2) fc mode switching (1/2 cutoff frequency switching, HD block)
3) Filter mode/filter bypass mode switching (HD block)
4) Input type switching (sync-tip clamp, bias, HD block)
5) Power-down function
6) Gain setting

The transfer rate of I²C-BUS corresponds to the fast-mode (up to 400kbit/s). Note that the SM5320A does not support a read function (IC is write only).

Basic Cycle

The write sequence is: SM5320A slave address → specific control register sub-address → write data. Data can be written to the SM5320A in successive bytes, as the sub-address for the register is incremented automatically after each byte. However, if the sub-address exceeds the address of the last register (03h), data write operation to the SM5320A register stops and the acknowledge signal is not returned.

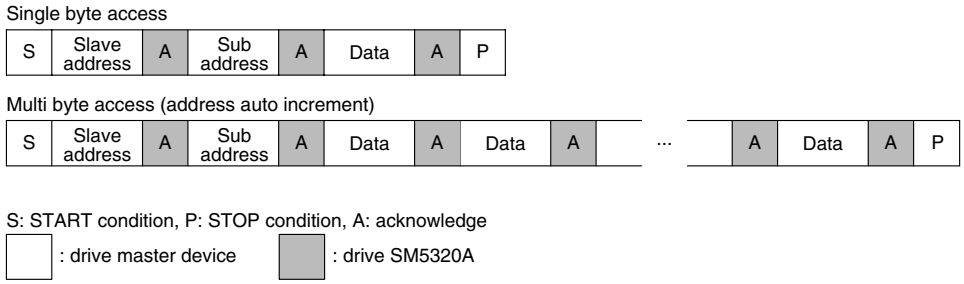


Figure 1. Write sequence

Slave Address

The 7-bit slave address is selected using the ADS pin. When ADS = “L” the address is 48h (1001000b), when ADS = “H” the address is 49h (1001001b), and when ADS = “Z” (open) the address is 4Ah (1001010b). A maximum of three SM5320A devices can be connected to the same I^2C-BUS simultaneously, and controlled independently by setting the slave address of each using the ADS pin. When writing to control register, send sub address of control register following slave address.

SLAVE ADDRESS for control register write (1st byte)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	SLAVE ADDRESS							R/W		
Value	1	0	0	1	0	0	0	0	90h	Indicate to write when device's slave address is 48h (ADS = "L")
	1	0	0	1	0	0	1	0	92h	Indicate to write when device's slave address is 49h (ADS = "H")
	1	0	0	1	0	1	0	0	94h	Indicate to write when device's slave address is 4Ah (ADS = "Z")

SUB ADDRESS for control register write (2nd byte)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	SUB ADDRESS									
Value	0	0	0	0	0	0	0	0	00h	Indicate to write control register 00h
	0	0	0	0	0	0	0	1	01h	Indicate to write control register 01h
	0	0	0	0	0	0	1	0	02h	Indicate to write control register 02h
	0	0	0	0	0	0	1	1	03h	Indicate to write control register 03h

Control Register

The SM5320A has a 4-byte control register.

Sub Addr.	Register assign								default	Description
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	
00h	FCM	FC6	FC5	FC4	FC3	FC2	FC1	FC0	00h	OUT1 to OUT3 fc control
01h	CB5	CB4	CB3	CB2	CB1	CB0	BYP	–	00h	OUT1 to OUT3 input method and filter bypass setting
02h	PD	HALF	GS15	GS14	GS13	GS12	GS11	GS10	00h	OUT1 to OUT3 gain control
03h	–	–	GS25	GS24	GS23	GS22	GS21	GS20	00h	YOUT, COUT gain control

Flag settings

(1) Cutoff frequency

Register name: FCM, FC

Address: Sub address = 00h, bit7 to bit0

FCDATA	FCSET	Flag name								Cutoff frequency [MHz]	Default
		FCM	FC6	FC5	FC4	FC3	FC2	FC1	FC0		
0	00h	0	0	0	0	0	0	0	0	4.10	○
1	01h	0	0	0	0	0	0	0	1	4.26	
2	02h	0	0	0	0	0	0	1	0	4.42	
:											
125	7Dh	0	1	1	1	1	1	0	1	22.5	
126	7Eh	0	1	1	1	1	1	1	0	22.7	
127	7Fh	0	1	1	1	1	1	1	1	22.8	
128	80h	1	0	0	0	0	0	0	0	7.53	
129	81h	1	0	0	0	0	0	0	1	7.83	
130	82h	1	0	0	0	0	0	1	0	8.12	
:											
253	FDh	1	1	1	1	1	1	0	1	42.2	
254	FEh	1	1	1	1	1	1	1	0	42.5	
255	FFh	1	1	1	1	1	1	1	1	42.7	

(2) Input type switching (sync-tip clamp, bias)

Register name: CB

Address: Sub address = 01h, bit7 to bit2

Control register Sub address 01h						INPUT			Description
bit7	bit6	bit5	bit4	bit3	bit2	IN1	IN2	IN3	
*	0					Clamp			IN1: sync-tip clamp input (default)
*	1					Bias			IN1: bias input
		*	0				Clamp		IN2: sync-tip clamp input (default)
		*	1				Bias		IN2: bias input
				*	0			Clamp	IN3: sync-tip clamp input (default)
				*	1			Bias	IN3: bias input

Sets the input method of IN1, IN2, IN3.

(3) Power-down mode select

Register name: PD

Address: Sub address = 02h, bit7

Control register Sub address 02h	Description
bit7	
0	Normal operation (default)
1	Power-down mode. Current consumption: ≤ 500μA

Sets the normal operation or power-down mode.

(4) fc mode switching (1/2 cutoff frequency switching)

Register name: HALF

Address: Sub address = 02h, bit6

Control register Sub address 02h	Description
bit6	
0	Standard fc mode. OUT1, OUT2, OUT3 cutoff frequency is identical. (default)
1	Half fc mode. OUT2, OUT3 cutoff frequency is 1/2 that of OUT1.

Sets the standard fc mode or half fc mode.

(5) Filter bypass mode

Register name: BYP

Address: Sub address = 01h, bit1

Control register Sub address 01h	Description
bit1	
0	Filter mode. The signals is output to OUT1, OUT2, OUT3 passing through filter. (default)
1	Filter bypass mode. The signals is output to OUT1, OUT2, OUT3 without passing through filter.

Sets the use or nonuse of filter.

(6) Output gain setting

Register name: GS1

Address: Sub address = 02h, bit5 to bit0

Control register Sub address 02h								OUT1, OUT2, OUT3 gain control
bit5	bit4	bit3	bit2	bit1	bit0	(HEX)	(DEC)	
1	0	0	0	0	0	20h	– 32	– 2.10dB
1	0	0	0	0	1	21h	– 31	– 2.05dB
1	0	0	0	1	0	22h	– 30	– 2.00dB
:								
1	1	1	1	1	0	3Eh	– 2	– 0.35dB
1	1	1	1	1	1	3Fh	– 1	– 0.28dB
0	0	0	0	0	0	00h	0	– 0.21dB (default)
0	0	0	0	0	1	01h	1	– 0.15dB
0	0	0	0	1	0	02h	2	– 0.10dB
0	0	0	0	1	1	03h	3	– 0.05dB
0	0	0	1	0	0	04h	4	± 0.00dB
:								
0	1	1	1	0	1	1Dh	29	+ 1.94dB
0	1	1	1	1	0	1Eh	30	+ 2.02dB
0	1	1	1	1	1	1Fh	31	+ 2.10dB

Sets the output gain of OUT1, OUT2, OUT3.

Register name: GS2

Address: Sub address = 03h, bit5 to bit0

Control register Sub address 03h								YOUT, COUT gain control
bit5	bit4	bit3	bit2	bit1	bit0	(HEX)	(DEC)	
1	0	0	0	0	0	20h	– 32	– 2.10dB
1	0	0	0	0	1	21h	– 31	– 2.05dB
1	0	0	0	1	0	22h	– 30	– 2.00dB
:								
1	1	1	1	1	0	3Eh	– 2	– 0.35dB
1	1	1	1	1	1	3Fh	– 1	– 0.28dB
0	0	0	0	0	0	00h	0	– 0.21dB (default)
0	0	0	0	0	1	01h	1	– 0.15dB
0	0	0	0	1	0	02h	2	– 0.10dB
0	0	0	0	1	1	03h	3	– 0.05dB
0	0	0	1	0	0	04h	4	± 0.00dB
:								
0	1	1	1	0	1	1Dh	29	+ 1.94dB
0	1	1	1	1	0	1Eh	30	+ 2.02dB
0	1	1	1	1	1	1Fh	31	+ 2.10dB

Sets the output gain of YOUT, COUT.

Lowpass Filter

The SM5320A has built-in 5th-order lowpass filters with variable cutoff frequency. The cutoff frequency range is set by the resistor (R_{ISET}) connected between ISET and GND, and the cutoff frequency setting is determined by FCDATA data. The cutoff frequency vs. FCDATA values are listed in table 1, and shown graphically in figure 2.

Table 1. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]
0	00	4.10	64	40	13.8	128	80	7.53	192	C0	26.0
1	01	4.26	65	41	13.9	129	81	7.83	193	C1	26.2
2	02	4.42	66	42	14.0	130	82	8.12	194	C2	26.5
3	03	4.58	67	43	14.2	131	83	8.42	195	C3	26.8
4	04	4.74	68	44	14.3	132	84	8.71	196	C4	27.0
5	05	4.90	69	45	14.5	133	85	9.01	197	C5	27.3
6	06	5.06	70	46	14.6	134	86	9.31	198	C6	27.6
7	07	5.21	71	47	14.8	135	87	9.60	199	C7	27.8
8	08	5.36	72	48	14.9	136	88	9.88	200	C8	28.1
9	09	5.52	73	49	15.1	137	89	10.2	201	C9	28.4
10	0A	5.68	74	4A	15.2	138	8A	10.5	202	CA	28.7
11	0B	5.83	75	4B	15.4	139	8B	10.8	203	CB	28.9
12	0C	5.99	76	4C	15.5	140	8C	11.1	204	CC	29.2
13	0D	6.14	77	4D	15.7	141	8D	11.4	205	CD	29.4
14	0E	6.30	78	4E	15.8	142	8E	11.7	206	CE	29.7
15	0F	6.45	79	4F	15.9	143	8F	12.0	207	CF	30.0
16	10	6.59	80	50	16.1	144	90	12.2	208	D0	30.2
17	11	6.79	81	51	16.2	145	91	12.5	209	D1	30.5
18	12	6.94	82	52	16.4	146	92	12.8	210	D2	30.8
19	13	7.09	83	53	16.5	147	93	13.1	211	D3	31.0
20	14	7.23	84	54	16.7	148	94	13.4	212	D4	31.3
21	15	7.38	85	55	16.8	149	95	13.7	213	D5	31.6
22	16	7.53	86	56	17.0	150	96	14.0	214	D6	31.8
23	17	7.67	87	57	17.1	151	97	14.3	215	D7	32.1
24	18	7.80	88	58	17.2	152	98	14.6	216	D8	32.4
25	19	7.95	89	59	17.4	153	99	14.9	217	D9	32.6
26	1A	8.10	90	5A	17.5	154	9A	15.1	218	DA	32.9
27	1B	8.25	91	5B	17.7	155	9B	15.4	219	DB	33.2
28	1C	8.40	92	5C	17.8	156	9C	15.7	220	DC	33.5
29	1D	8.55	93	5D	18.0	157	9D	16.0	221	DD	33.7
30	1E	8.70	94	5E	18.1	158	9E	16.3	222	DE	34.0
31	1F	8.85	95	5F	18.3	159	9F	16.6	223	DF	34.3
32	20	8.97	96	60	18.4	160	A0	16.8	224	E0	34.5
33	21	9.13	97	61	18.5	161	A1	17.1	225	E1	34.7
34	22	9.28	98	62	18.7	162	A2	17.4	226	E2	35.0
35	23	9.43	99	63	18.8	163	A3	17.7	227	E3	35.3
36	24	9.58	100	64	19.0	164	A4	18.0	228	E4	35.5
37	25	9.74	101	65	19.1	165	A5	18.3	229	E5	35.8
38	26	9.89	102	66	19.3	166	A6	18.6	230	E6	36.1
39	27	10.0	103	67	19.4	167	A7	18.9	231	E7	36.4
40	28	10.2	104	68	19.5	168	A8	19.2	232	E8	36.6
41	29	10.3	105	69	19.7	169	A9	19.5	233	E9	36.9
42	2A	10.5	106	6A	19.8	170	AA	19.8	234	EA	37.2
43	2B	10.6	107	6B	20.0	171	AB	20.0	235	EB	37.4
44	2C	10.8	108	6C	20.1	172	AC	20.3	236	EC	37.7
45	2D	10.9	109	6D	20.3	173	AD	20.6	237	ED	37.9
46	2E	11.1	110	6E	20.4	174	AE	20.9	238	EE	38.2
47	2F	11.2	111	6F	20.5	175	AF	21.2	239	EF	38.5
48	30	11.4	112	70	20.7	176	B0	21.5	240	F0	38.8
49	31	11.5	113	71	20.8	177	B1	21.8	241	F1	39.0
50	32	11.7	114	72	21.0	178	B2	22.1	242	F2	39.3
51	33	11.8	115	73	21.1	179	B3	22.4	243	F3	39.6
52	34	12.0	116	74	21.2	180	B4	22.7	244	F4	39.8
53	35	12.1	117	75	21.4	181	B5	22.9	245	F5	40.1
54	36	12.3	118	76	21.5	182	B6	23.2	246	F6	40.3
55	37	12.4	119	77	21.7	183	B7	23.5	247	F7	40.6
56	38	12.6	120	78	21.8	184	B8	23.8	248	F8	40.9
57	39	12.7	121	79	22.0	185	B9	24.1	249	F9	41.1
58	3A	12.9	122	7A	22.1	186	BA	24.4	250	FA	41.4
59	3B	13.0	123	7B	22.2	187	BB	24.6	251	FB	41.7
60	3C	13.2	124	7C	22.4	188	BC	24.9	252	FC	42.0
61	3D	13.3	125	7D	22.5	189	BD	25.2	253	FD	42.2
62	3E	13.5	126	7E	22.7	190	BE	25.5	254	FE	42.5
63	3F	13.6	127	7F	22.8	191	BF	25.7	255	FF	42.7

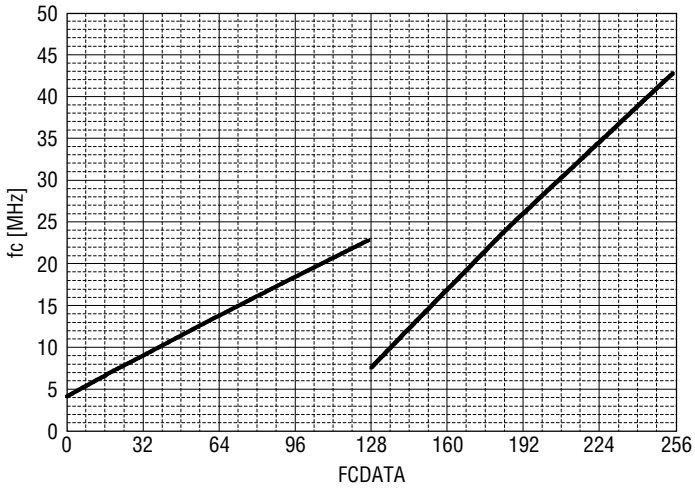


Figure 2. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

R_{ISET}

R_{ISET} controls the internal current source, and its connection is essential. The recommended value (R_{ISET}) is 1.8kΩ. In power-down mode and filter bypass mode, no current flows into R_{ISET}.

Note. A value other than 1.8kΩ will change the current consumption of SM5320A. In the determination of resistance value, caution should be taken to ensure the power dissipation does not exceed the absolute maximum rating for the package.

Half fc Mode

In half fc mode, the CH-2 and CH-3 cutoff frequency is 1/2 that of the CH-1 cutoff frequency setting. Half fc mode is useful for systems where the sampling frequency varies due to luminance (Y) and color difference signal (Cr, Cb) requirements as in component signals.

Group Delay Characteristics

The group delay varies with the cutoff frequency setting. Note also that in half fc mode, the group delay between CH-1 and CH-2/CH-3 varies.

Filter Bypass Mode

In filter bypass mode, the internal lowpass filter in SM5320A is bypassed and the signal is input to the output buffer stage directly. In filter bypass mode, the input type and output gain are set just as for filter mode. But the cutoff frequency setting and fc mode setting have no effect on the outputs. In this mode, the passband frequency is 80MHz (typ), which can support SXGA-class signals.

Power-ON Reset

When power is applied, an internal power-ON reset circuit operates initializing the internal register flags to their default settings. At power-ON, all supplies should be applied simultaneously.

Reference Voltage (REF)

The REF pin is internal reference voltage output. A 10 µF capacitor connected between pin and ground is recommended for stability of movement.

USAGE PRECAUTIONS

Slave Address (4Ah) Setting

When slave address 4Ah is used, the ADS input must be left open circuit. In this case, an external resistor should be connected as shown in figure 3 to reduce the risk of malfunction in the I^2C-BUS interface due to large external spikes or other noise invaded from outside. The recommended value is 10kΩ.

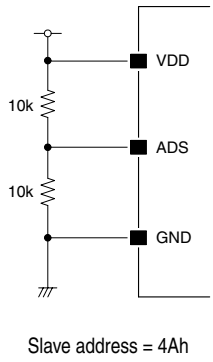


Figure 3. Slave address 4Ah setting

Power Supply Invest Timing

The SM5320A uses 2-type power supply, analog one (VCC1, VCC2, VCC3, VCC4, VCC5) and digital one (VDD). Therefore all power supply pins should be forced voltage at the same time power supply invested. In the case analog power supply and digital one are set up separately, composing system the time-lag to makes short time as standard under 1ms is need. And if voltage of digital power supply comes higher than one of analog power supply, it is necessary to set voltage of digital power supply to make potential difference bellow 250mV as compared with voltage of analog one.