SM5308AS

3-channel Video Buffer with Built-in wideband LPF

OVERVIEW

The SM5308AS is a 3-channel video buffer with built-in 5th-order lowpass filters. The lowpass filter cutoff frequency range can adjust from 5.0MHz to 44MHz[*1] by 256 steps. The lowpass filter supports 480i to 1080i format, video signal equipment analog input/outputs. For video input systems, the device functions as a next-stage ADC system anti-aliasing filter. For video output systems, the filter reduces video DAC aliasing and external noise and can drive up to two 75Ω terminating resistance. The cutoff frequency, signal input type, and output gain switching can be controlled using an I^2C-BUS[*2], and the I^2C slave address can be set by ADS (3-state input) to allow up to three SM5308AS on the same bus.

*1. When the resistor connected to ISET (R_{ISET}) is 1.8kΩ.
*2. I^2C-BUS is a registered trademark of Philips Electronics N.V.

FEATURES

- Supply voltages
  - Analog: 4.75 to 5.25V
  - Digital: 3.0 to 5.5V
- Lowpass filter with adjustable cutoff frequency (256 steps)
  - Cutoff frequency range: 5.0MHz to 44MHz (R_{ISET} = 1.8kΩ)
- Filter bypass mode function for display specifications up to SXGA resolution
  - Passband: 80MHz (typ)
- Half fc mode switch function (CH-2, CH-3) suitable for component signals
- Video input pins can be independently set to sync-tip clamp/bias/direct inputs
- Up to two 75Ω terminating resistance drive capability
- Output gain switching: 0dB/6dB
- Disable function
  - ≤ 300µA current consumption when disabled
- I^2C-BUS interface control
  - Slave address: 90h, 92h, or 94h (up to three devices can be used simultaneously, selected by ADS input)
  - Data transfer rate: Fast mode (up to 400kbit/s)
- Operating ambient temperature range: 0 to 70°C
- Package: 28-pin HSOP

APPLICATIONS

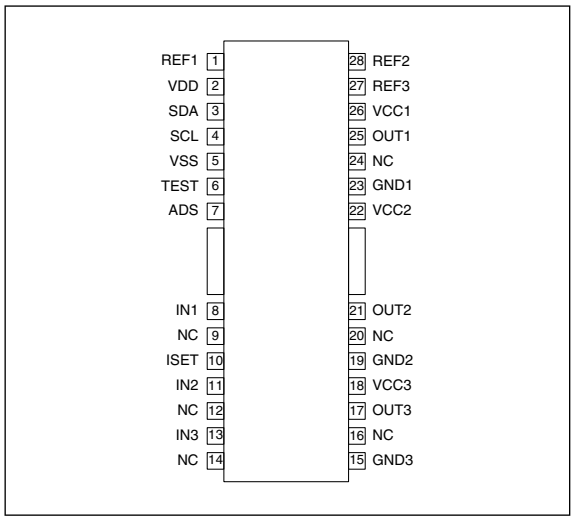
- HDTVs
- LCD TVs
- PDPs
- Projectors

ORDERING INFORMATION

Device	Package
SM5308AS	28-pin HSOP

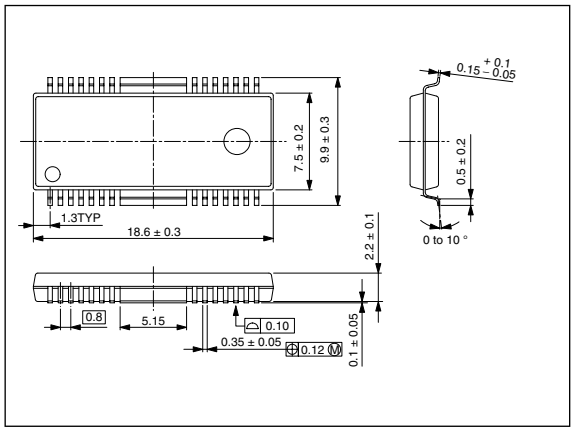
PINOUT

(Top view)

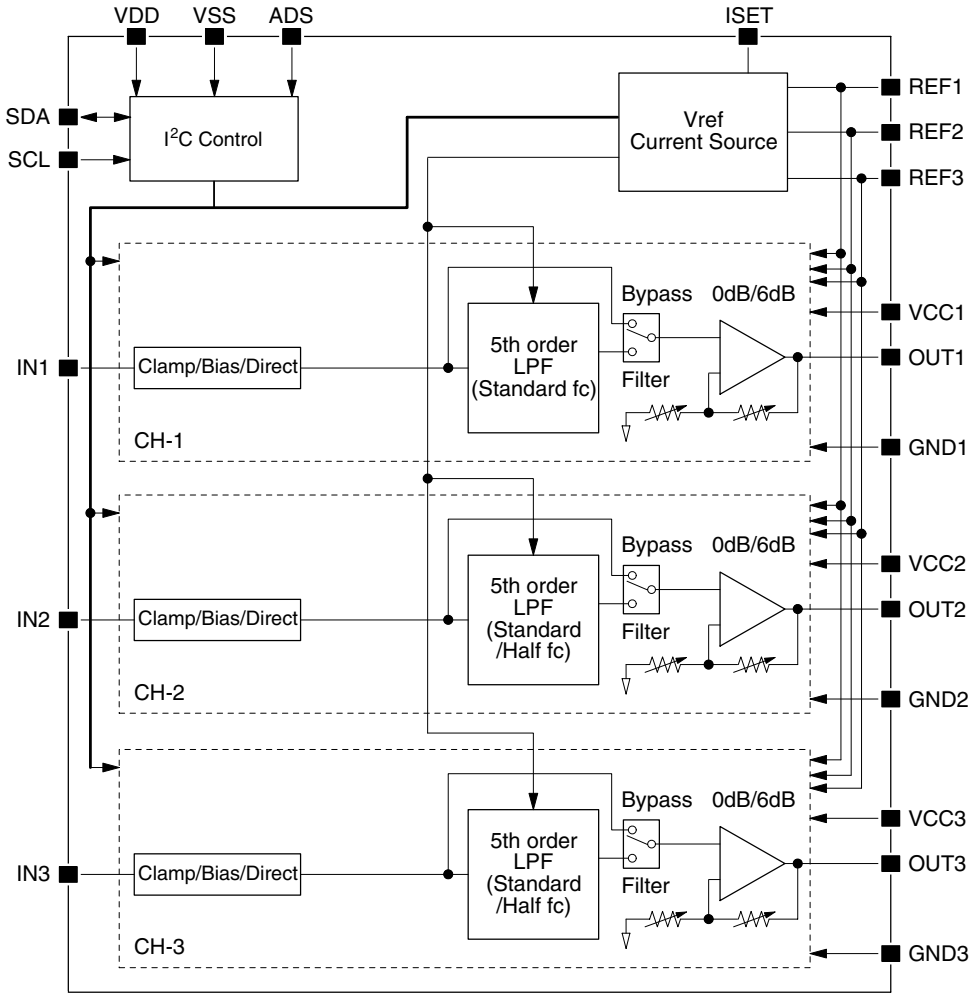


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



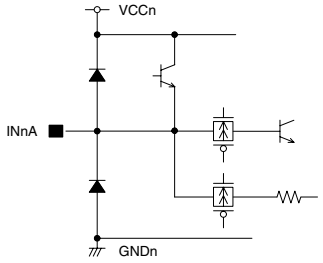
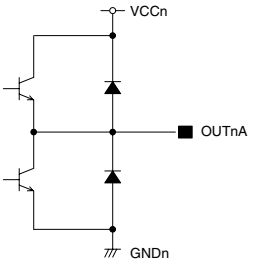
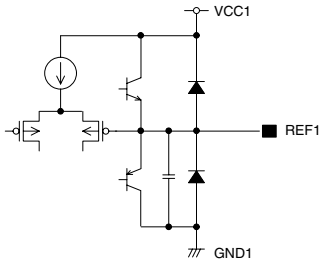
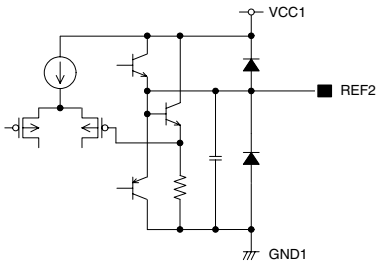
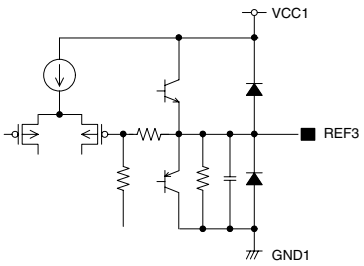
Note. The recommended value of the external resistor (R_{ISET}) connected to ISET is 1.8kΩ.

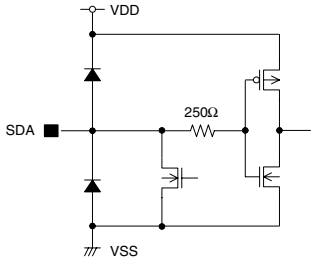
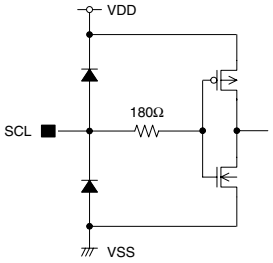
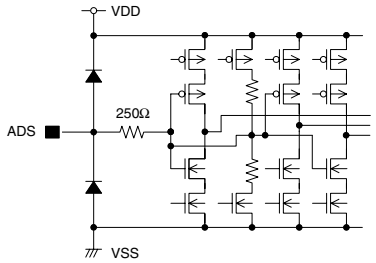
PIN DESCRIPTION

Number	Name	I/O*1	A/D*2	Description
1	REF1	O	A	Internal reference voltage 1
2	VDD	–	D	Digital supply
3	SDA	I/O	D	I^2C data signal input/output
4	SCL	I	D	I^2C clock signal input
5	VSS	–	D	Digital ground
6	TEST	–	–	Test pin (connect to ground)
7	ADS	I	D	I^2C slave address select (3-state input)
8	IN1	I	A	Video signal input (CH-1 input)
9	NC	–	–	No connection
10	ISET	–	A	Internal current-setting resistor (R_{ISET}) connection (standard 1.8kΩ)
11	IN2	I	A	Video signal input (CH-2 input)
12	NC	–	–	No connection
13	IN3	I	A	Video signal input (CH-3 input)
14	NC	–	–	No connection
15	GND3	–	A	Analog ground (CH-3)
16	NC	–	–	No connection
17	OUT3	O	A	Video signal output (CH-3)
18	VCC3	–	A	Analog supply (CH-3)
19	GND2	–	A	Analog ground (CH-2)
20	NC	–	–	No connection
21	OUT2	O	A	Video signal output (CH-2)
22	VCC2	–	A	Analog supply (CH-2)
23	GND1	–	A	Analog ground (CH-1, Vref)
24	NC	–	–	No connection
25	OUT1	O	A	Video signal output (CH-1)
26	VCC1	–	A	Analog supply (CH-1, Vref)
27	REF3	O	A	Internal reference voltage 3
28	REF2	O	A	Internal reference voltage 2

*1. I: input, O: output
*2. A: analog, D: digital

PIN EQUIVALENT CIRCUITS

Number	Name	I/O*1	Equivalent circuit
8 11 13	IN1 IN2 IN3	I	
25 21 17	OUT1 OUT2 OUT3	O	
1	REF1	O	
28	REF2	O	
27	REF3	O	

Number	Name	I/O*1	Equivalent circuit
3	SDA	I/O	
4	SCL	I	
7	ADS	I	

*1. I: input, O: output

Note. Resistance values in the equivalent circuits indicate design values.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = GND1 = GND2 = GND3 = GND = 0V, VCC1 = VCC2 = VCC3 = VDD = V_{CC}

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	VCC1, VCC2, VCC3, VDD	– 0.3 to 7.0	V
Input voltage	V_{IN}	ADS, SDA, SCL, INn (n = 1, 2, 3)	GND – 0.3 to V_{CC} + 0.3	V
Storage temperature range	T_{STG}		– 55 to + 125	°C
Power dissipation	P_D	θja = 60°C/W Note. θja is the measured quantity under the mounted condition which NPC specified.	1.0	W
Junction temperature	T_J		125	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1	V_{CC}	VCC1, VCC2, VCC3	4.75 to 5.25	V
Supply voltage difference	ΔV_{CC}	VCC1 – VCC2, VCC1 – VCC3, VCC2 – VCC3	± 0.1	V
Supply voltage 2	V_{DD}	VDD	3.0 to 5.5	V
Operating ambient temperature	Ta		0 to 70	°C

Note. VCC1 to VCC3 should be applied simultaneously.

Electrical Characteristics

DC Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

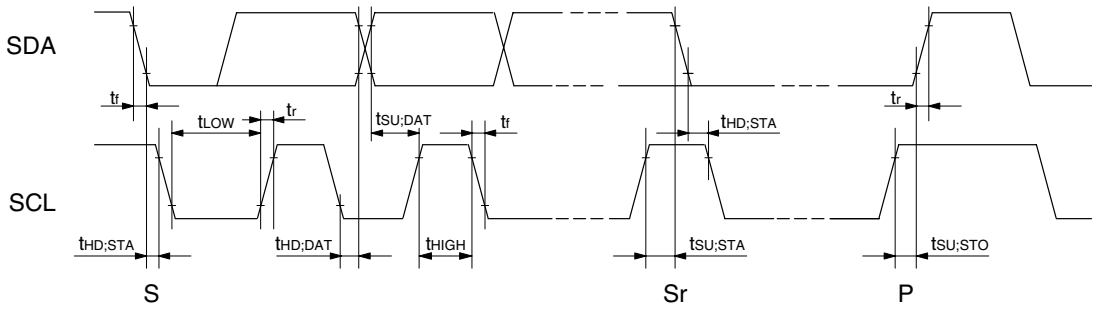
Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Current consumption 1*1	I_{CC1}	Filter mode, FCDATA = 255	–	130	155	mA	I
Current consumption 2*1	I_{CC2}	Filter bypass mode	–	85	125	mA	I
Current consumption 3*1	I_{CC3}	Power-down mode, 3-address mode	–	–	300	μA	I
Current consumption 4*1	I_{CC4}	Power-down mode, 2-address mode	–	–	250	μA	I
HIGH-level input voltage	V_{IH1}	SDA, SCL	0.7 V_{DD}	–	–	V	I
LOW-level Input voltage	V_{IL1}	SDA, SCL	–	–	0.3 V_{DD}	V	I
ADS HIGH-level input voltage	V_{IH2}	ADS	0.8 V_{DD}	–	–	V	I
ADS LOW-level input voltage	V_{IL2}	ADS	–	–	0.2 V_{DD}	V	I
ADS open-circuit input voltage	V_{OPEN}	ADS	$V_{DD}/2$ – 0.2	–	$V_{DD}/2$ + 0.2	V	I
LOW-level input leakage current	I_{LL}	SDA, SCL, V_{IN} = 0V	–	–	1.0	μA	I
HIGH-level input leakage current	I_{LH}	SDA, SCL, V_{IN} = V_{DD}	–	–	1.0	μA	I
SDA output voltage	V_{OL}	SDA = LOW output, Sink current = 3mA	0	–	0.4	V	I

*1. Total of current consumption of VCC1, VCC2, VCC3, and VDD, when no input signals.

AC Characteristics (I^2C-BUS)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
SCL clock frequency	f_{SCL}		0	–	400	kHz	II
SCL hold time (start condition)	$t_{HD;STA}$		0.6	–	–	µs	II
SCL clock LOW-level pulsewidth	t_{LOW}		1.3	–	–	µs	II
SCL clock HIGH-level pulsewidth	t_{HIGH}		0.6	–	–	µs	II
SCL setup time (start condition)	$t_{SU;STA}$		0.6	–	–	µs	II
SDA data hold time	$t_{HD;DAT}$		0	–	0.9	µs	II
SDA data setup time	$t_{SU;DAT}$		100	–	–	ns	II
SDA, SCL rise time	t_r		–	–	300	ns	II
SDA, SCL fall time	t_f		–	–	300	ns	II
SCL setup time (stop condition)	$t_{SU;STO}$		0.6	–	–	µs	II
SDA, SCL input capacitance	C_i		–	–	10	pF	II



Note. S, Sr: start condition, P: stop condition

Analog Characteristics

Analog input characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted. Internal mode settings are shown in table 1 in "Mode Condition Settings".

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Clamp voltage	V_{CLMP}	Clamp input	1.65	1.85	2.05	V	I
Bias voltage	V_{BIAS}	Bias input	2.15	2.35	2.55	V	I
Input resistance	R_{BIAS}	Bias input	–	20	–	kΩ	II
Filter mode maximum input voltage	V_{AI1}	Mode: b0 (bias, 0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI2}	Mode: b6 (bias, 6dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI3}	Mode: c0 (clamp, 0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI4}	Mode: c6 (clamp, 6dB), THD < 1.5%	1.0	–	–	Vp-p	I
Bypass mode maximum input voltage	V_{AI5}	Mode: f0 (bias, 0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI6}	Mode: f6 (bias, 6dB), THD < 1.5%	1.2	–	–	Vp-p	I
	V_{AI7}	Mode: g0 (clamp, 0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{AI8}	Mode: g6 (clamp, 6dB), THD < 1.5%	1.0	–	–	Vp-p	I
Direct mode input DC voltage range	V_{IDC1}	Mode: h0, THD < 1.5%, V_{IN} < 1.4Vp-p	1.3	–	2.9	V	I
	V_{IDC2}	Mode: h6, THD < 1.5%, V_{IN} < 1.2Vp-p	1.7	–	3.0	V	I
	V_{IDC3}	Mode: j0, THD < 1.5%, V_{IN} < 1.4Vp-p	1.1	–	3.3	V	I
	V_{IDC4}	Mode: j6, THD < 1.5%, V_{IN} < 1.2Vp-p	1.6	–	3.0	V	I

Note. This item represents values of maximum input signal amplitude in which the output distortion rate shown in the condition column is filled. When the signal amplitude that exceeds this specification value is input, the output distortion rate is deteriorated. When using this device, the input signal level should be set not to exceed the standard value (min) of the signal amplitude.

Filter mode and bypass mode frequency characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Cutoff frequency	F_{C1}	FCDATA = 0	–	5.00	–	MHz	II
	F_{C2}	FCDATA = 10	5.93	6.74	7.55	MHz	I
	F_{C3}	FCDATA = 227	32.4	36.78	41.2	MHz	I
	F_{C4}	FCDATA = 255	–	44.27	–	MHz	II
Half fc mode cutoff frequency ratio	R_{half1}	Half fc mode, FCDATA = 10	46	51	56	%	I
	R_{half2}	Half fc mode, FCDATA = 227	49	54	59	%	I
4fc attenuation	G_{SB}	fin ≥ 4fc, attenuation from fin = 100kHz	–	50	–	dB	II
Filter bypass mode passband	F_{BP}	V_{IN} = 0.7Vp-p, Gain = – 1dB	68	80	–	MHz	I

Analog output characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted. Internal mode settings are shown in table 1 in "Mode Condition Settings".

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Filter mode output gain	A_{VF1}	Gain = 0dB	– 0.5	0	0.5	dB	I
	A_{VF2}	Gain = 6dB	5.5	6.0	6.5	dB	I
Filter bypass mode output gain	A_{VB1}	Gain = 0dB	– 0.5	0	0.5	dB	I
	A_{VB2}	Gain = 6dB	5.5	6.0	6.5	dB	I
Filter bypass mode gain error	dA_{VBP}	Gain error between filter mode and bypass mode	–	± 0.2	–	dB	I
Channel to channel gain error	dA_{VCH}		–	–	± 0.2	dB	I
Maximum output voltage	V_{out1}	Mode: b0, c0 (0dB), THD < 1.0%	1.4	–	–	Vp-p	I
	V_{out2}	Mode: b6, c6 (6dB), THD < 1.5%	2.4	–	–	Vp-p	I
Output distortion	T_{HDB1}	Mode: b0, fin = 1kHz, V_{IN} = 1.4Vp-p	–	0.2	1.0	%	I
	T_{HDB2}	Mode: b6, fin = 1kHz, V_{IN} = 1.2Vp-p	–	0.2	1.0	%	I
	T_{HDC1}	Mode: c0, fin = 1kHz, V_{IN} = 1.4Vp-p	–	0.2	1.0	%	I
	T_{HDC2}	Mode: c6, fin = 1kHz, V_{IN} = 1.0Vp-p	–	0.5	1.5	%	I
Channel to channel crosstalk	X_{TLK1}	0.5Vp-p input, fin = 1MHz, between 2 channels	–	– 71	–	dB	II
Drive load resistance	R_L	1 load = 150Ω	–	–	2	load	I
I^2C response time	T_{IC}	Response time from ACK bit output when changing settings using I^2C-BUS	–	–	1	µs	II

Reference voltage characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
REF output voltage	V_{R1}	REF1	–	2.40	–	V	II
	V_{R2}	REF2	–	2.50	–	V	II
	V_{R3}	REF3	–	3.40	–	V	II

Test level

The definition of “Test Level” shown in the electrical characteristic table is as follows.

I : 100% of products tested at Ta = + 25°C.

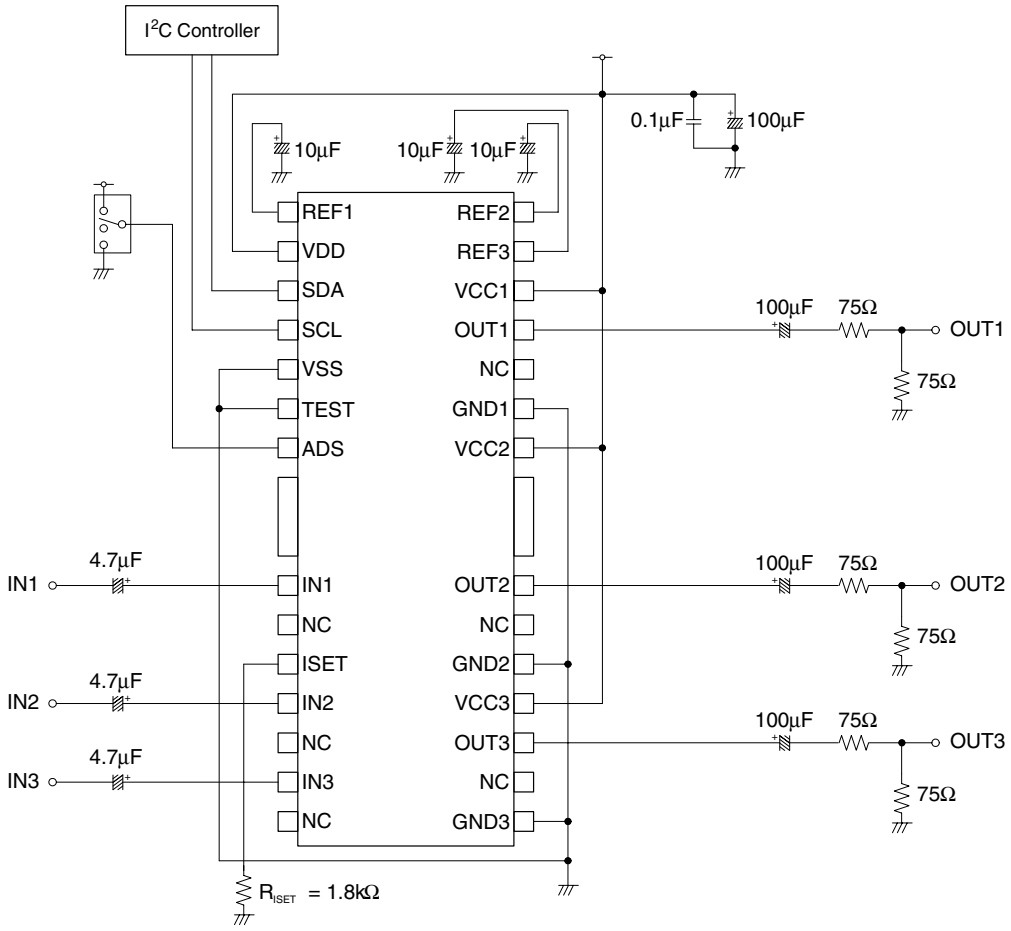
II : Guaranteed as result of design and characteristics evaluation.

Mode Condition Settings

Table 1. Mode settings

Mode setting	Input type			Output gain	fc mode	Filter/Bypass mode
	CH-1	CH-2	CH-3			
a0	Clamp	Bias	Bias	0dB	Standard	Filter
a6				6dB		
b0	Bias			0dB		
b6				6dB		
c0	Clamp			0dB		
c6				6dB		
d0	Bias			0dB	Half	
d6				6dB		
e0	Clamp			0dB		
e6				6dB		
f0	Bias			0dB	–	Bypass
f6				6dB		
g0	Clamp			0dB		
g6				6dB		
h0	Direct			0dB	Standard	Filter
h6				6dB		
i0				0dB	Half	
i6				6dB		
j0				0dB	–	Bypass
j6				6dB		

Evaluation Circuit Diagram



Note. This is the electrical characteristics evaluation circuit only, then it is not a recommended application circuit.
TEST pin should be connected to GND.

FUNCTIONAL DESCRIPTION

I²C-BUS Control

The SM5308AS uses an I²C BUS interface to set the following functions.

1) Cutoff frequency
2) Output gain
3) fc mode switching (1/2 cutoff frequency switching)
4) Filter mode/filter bypass mode switching
5) Input type switching (sync-tip clamp, bias, direct)
6) Disable function
7) Maximum number of slave addresses

The transfer rate of I²C-BUS corresponds to the fast-mode (up to 400kbit/s). Note that the SM5308AS does not support a read function (IC is write only).

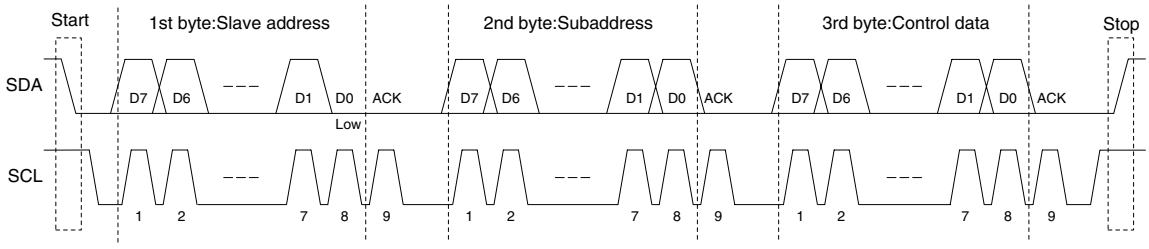
Basic cycle

I²C-BUS start/stop condition

The basic access cycle comprises the following elements.

1) Start condition
2) 1st byte: Slave address
3) 2nd byte: Subaddress
4) 3rd byte: Control data
5) Stop condition

If the input data does not match the slave address or the subaddress is incorrect, the corresponding ACK (acknowledge) bit is not output LOW. However, the ACK bit is output after 3rd byte irrespective of the byte data. Also note that the IC does not support a subaddress auto-increment function, hence each subaddress access requires all the basic cycle steps 1 to 5.



1st byte: slave address

The ADS pin can set one of three slave addresses. Note that D0 must be “0 (Write)”.

ADS	1st byte: slave address								
	HEX	D7	D6	D5	D4	D3	D2	D1	D0
L	90h	1	0	0	1	0	0	0	0 (W)
H	92h	1	0	0	1	0	0	1	0 (W)
Open*1	94h	1	0	0	1	0	1	0	0 (W)

*1. When ADS is open (94h), I^2C-BUS control may not be able to set the address. See “P16. (7) Maximum number of slave addresses”.

2nd byte: subaddress

The 2nd byte sets the subaddress, selecting one of three registers.

Register name	2nd byte: subaddress								
	HEX	D7	D6	D5	D4	D3	D2	D1	D0
FCSET	01h	0	0	0	0	0	0	0	1
CONDITION1	02h	0	0	0	0	0	0	1	0
CONDITION2	03h	0	0	0	0	0	0	1	1

3rd byte: control data

The 3rd byte control data sets the register flags corresponding to the subaddress selected by 2nd byte. The flags assigned are shown in the following table.

Register name	3rd byte: control data							
	D7	D6	D5	D4	D3	D2	D1	D0
FCSET	FCM	FC6	FC5	FC4	FC3	FC2	FC1	FC0
CONDITION1	CB5	CB4	CB3	CB2	CB1	CB0	–	GS
CONDITION2	PD	–	HALF	BYPASS	–	NCA	–	–

Flag settings

(1) Cutoff frequency

Register name: FCSET

Flag names: FCM, FC [6:0]

The FCSET register setting sets the cutoff frequency using one of two tuning adjustment functions, thus a total of 256 steps are possible.

FCDATA	FCSET	Flag name								Cutoff frequency [MHz]	Default
		FCM	FC6	FC5	FC4	FC3	FC2	FC1	FC0		
0	00h	0	0	0	0	0	0	0	0	5.00	○
1	01h	0	0	0	0	0	0	0	1	5.17	
2	02h	0	0	0	0	0	0	1	0	5.35	
:											
125	7Dh	0	1	1	1	1	1	0	1	23.58	
126	7Eh	0	1	1	1	1	1	1	0	23.72	
127	7Fh	0	1	1	1	1	1	1	1	23.85	
128	80h	1	0	0	0	0	0	0	0	9.31	
129	81h	1	0	0	0	0	0	0	1	9.62	
130	82h	1	0	0	0	0	0	1	0	9.93	
:											
253	FDh	1	1	1	1	1	1	0	1	43.73	
254	FEh	1	1	1	1	1	1	1	0	44.00	
255	FFh	1	1	1	1	1	1	1	1	44.27	

(2) Input type switching (sync-tip clamp, bias, direct)

Register name: CONDITION1

Flag names: CB [5:4], CB [3:2], CB [1:0]

These flags set the input type of CH-1, CH-2, and CH-3 to one of three types: sync-tip clamp input, bias input, or direct input.

Channel	Flag name		Input type	Default
CH-1 CH-2 CH-3	CB5 CB3 CB1	CB4 CB2 CB0		
	L	L	Sync-tip clamp input	○
	L	H	Bias input	
	H	Don't care	Direct input*1	

*1. An input coupling capacitor should not be connected when direct input is selected.

(3) Output gain

Register name: CONDITION1

Flag name: GS

Flag name	Output gain	Default
GS		
L	0dB	○
H	6dB	

(4) Disable mode select

Register name: CONDITION2

Flag name: PD

This flag enables/disables the analog block. When the analog block is disabled, the output pins are high impedance.

Flag name	Mode	Default
PD		
L	Enable (normal operation)	○
H	Disable (no operation)	

(5) fc mode switching (1/2 cutoff frequency switching)

Register name: CONDITION2

Flag name: HALF

This flag switches the cutoff frequency of CH-2 and CH-3 to divide the value set by the FCSET register into halves. Note that the CH-1 cutoff frequency cannot be switched to 1/2. This mode is suitable for systems where the sampling frequency varies due to Y, Cr, and Cb requirements, such as component signals.

Flag name	fc mode	Default
HALF		
L	Standard fc mode (CH-1, CH-2, CH-3 cutoff frequency is identical)	○
H	Half fc mode (CH-2, CH-3 cutoff frequency is 1/2 that of CH-1)	

(6) Filter bypass mode

Register name: CONDITION2

Flag name: BYPASS

This flag allows the internal lowpass filter in SM5308AS to be bypassed. The output gain can be switched, even in filter bypass mode. The input type and output gain can all be set just as in filter mode. However, the cutoff frequency and fc mode settings have no effect on the outputs.

Flag name	Filter	Default
BYPASS		
L	Filter mode (signals pass through lowpass filter)	○
H	Filter bypass mode (signals bypass lowpass filter)	

(7) Maximum number of slave addresses

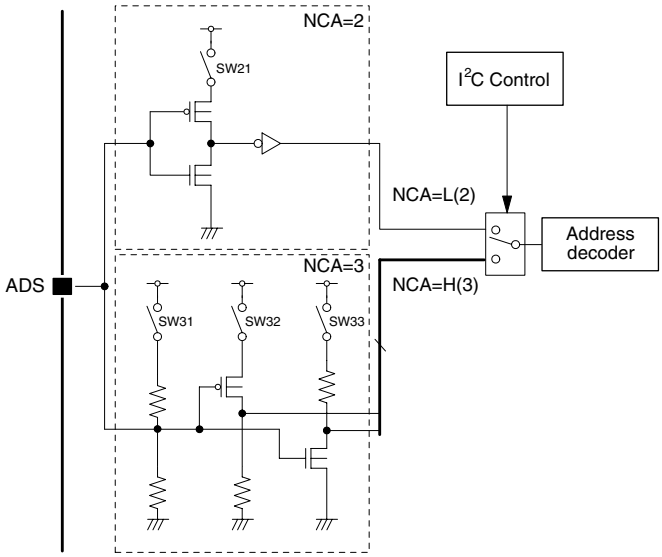
Register name: CONDITION2

Flag name: NCA

The NCA flag sets the maximum number of slave address selected by the ADS input pins to either 2 or 3 by setting of the NAC resistor. The ADS input pin equivalent circuit is shown below.
When NCA = LOW, switches SW31 to SW33 are OFF and 2 ADS input levels (LOW or HIGH) are valid.
When NCA = HIGH, switches SW31 to SW33 are ON and 3 ADS input levels (LOW, HIGH, and Open) are valid. In this time, the current consumption increases by several hundreds μA compared to the NCA = "L" setting.

Note. The default value for NCA plug is HIGH (3 address). If NCA is once set to LOW (2 address) for a device addressed by the setting when ADS is Open, that device is subsequently no longer accessible until power supply turns OFF.

Flag name NCA	Maximum number of slave address	Default	ADS pin setting	Slave address	ADS pin current flow
L	2 (2-address mode)		LOW HIGH Open	1001000 1001001 Invalid	No
H	3 (3-address mode)	○	LOW HIGH Open	1001000 1001001 1001010	Yes



Lowpass Filter

The SM5308AS has built-in 5th-order lowpass filters with variable cutoff frequency. The cutoff frequency range is set by the resistor (R_{ISET}) connected between ISET and GND, and the cutoff frequency setting is determined by FCDATA data. The cutoff frequency vs. FCDATA values are listed in table 2, and shown graphically in figure 1.

Table 2. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]
0	00	5.00	64	40	15.18	128	80	9.31	192	C0	27.56
1	01	5.17	65	41	15.33	129	81	9.62	193	C1	27.83
2	02	5.35	66	42	15.47	130	82	9.93	194	C2	28.10
3	03	5.52	67	43	15.62	131	83	10.24	195	C3	28.36
4	04	5.70	68	44	15.76	132	84	10.55	196	C4	28.63
5	05	5.87	69	45	15.90	133	85	10.86	197	C5	28.90
6	06	6.04	70	46	16.05	134	86	11.16	198	C6	29.16
7	07	6.22	71	47	16.19	135	87	11.47	199	C7	29.43
8	08	6.39	72	48	16.33	136	88	11.78	200	C8	29.69
9	09	6.57	73	49	16.48	137	89	12.09	201	C9	29.96
10	0A	6.74	74	4A	16.62	138	8A	12.40	202	CA	30.21
11	0B	6.92	75	4B	16.77	139	8B	12.71	203	CB	30.48
12	0C	7.09	76	4C	16.91	140	8C	13.00	204	CC	30.74
13	0D	7.26	77	4D	17.05	141	8D	13.30	205	CD	31.00
14	0E	7.42	78	4E	17.20	142	8E	13.60	206	CE	31.26
15	0F	7.59	79	4F	17.34	143	8F	13.90	207	CF	31.53
16	10	7.75	80	50	17.49	144	90	14.20	208	D0	31.79
17	11	7.92	81	51	17.62	145	91	14.48	209	D1	32.05
18	12	8.08	82	52	17.76	146	92	14.77	210	D2	32.31
19	13	8.24	83	53	17.90	147	93	15.06	211	D3	32.58
20	14	8.41	84	54	18.04	148	94	15.35	212	D4	32.83
21	15	8.57	85	55	18.18	149	95	15.64	213	D5	33.10
22	16	8.74	86	56	18.32	150	96	15.92	214	D6	33.36
23	17	8.89	87	57	18.45	151	97	16.21	215	D7	33.63
24	18	9.06	88	58	18.60	152	98	16.50	216	D8	33.88
25	19	9.21	89	59	18.73	153	99	16.79	217	D9	34.15
26	1A	9.38	90	5A	18.87	154	9A	17.08	218	DA	34.41
27	1B	9.53	91	5B	19.01	155	9B	17.36	219	DB	34.67
28	1C	9.69	92	5C	19.15	156	9C	17.65	220	DC	34.93
29	1D	9.85	93	5D	19.29	157	9D	17.94	221	DD	35.20
30	1E	10.01	94	5E	19.43	158	9E	18.23	222	DE	35.46
31	1F	10.17	95	5F	19.56	159	9F	18.51	223	DF	35.72
32	20	10.33	96	60	19.71	160	A0	18.80	224	E0	35.98
33	21	10.49	97	61	19.84	161	A1	19.09	225	E1	36.25
34	22	10.65	98	62	19.97	162	A2	19.38	226	E2	36.51
35	23	10.80	99	63	20.11	163	A3	19.66	227	E3	36.78
36	24	10.97	100	64	20.24	164	A4	19.93	228	E4	37.05
37	25	11.12	101	65	20.37	165	A5	20.21	229	E5	37.32
38	26	11.28	102	66	20.51	166	A6	20.49	230	E6	37.58
39	27	11.43	103	67	20.64	167	A7	20.77	231	E7	37.85
40	28	11.59	104	68	20.78	168	A8	21.04	232	E8	38.12
41	29	11.74	105	69	20.91	169	A9	21.32	233	E9	38.39
42	2A	11.89	106	6A	21.04	170	AA	21.60	234	EA	38.65
43	2B	12.05	107	6B	21.18	171	AB	21.88	235	EB	38.92
44	2C	12.20	108	6C	21.31	172	AC	22.15	236	EC	39.19
45	2D	12.36	109	6D	21.44	173	AD	22.43	237	ED	39.45
46	2E	12.50	110	6E	21.58	174	AE	22.71	238	EE	39.72
47	2F	12.65	111	6F	21.71	175	AF	22.99	239	EF	39.99
48	30	12.80	112	70	21.85	176	B0	23.26	240	F0	40.26
49	31	12.95	113	71	21.98	177	B1	23.54	241	F1	40.52
50	32	13.10	114	72	22.11	178	B2	23.82	242	F2	40.79
51	33	13.25	115	73	22.25	179	B3	24.09	243	F3	41.06
52	34	13.39	116	74	22.38	180	B4	24.35	244	F4	41.33
53	35	13.55	117	75	22.51	181	B5	24.62	245	F5	41.59
54	36	13.69	118	76	22.65	182	B6	24.89	246	F6	41.86
55	37	13.85	119	77	22.78	183	B7	25.16	247	F7	42.13
56	38	13.99	120	78	22.91	184	B8	25.42	248	F8	42.39
57	39	14.15	121	79	23.05	185	B9	25.69	249	F9	42.66
58	3A	14.29	122	7A	23.18	186	BA	25.96	250	FA	42.93
59	3B	14.44	123	7B	23.32	187	BB	26.22	251	FB	43.20
60	3C	14.59	124	7C	23.45	188	BC	26.49	252	FC	43.46
61	3D	14.74	125	7D	23.58	189	BD	26.76	253	FD	43.73
62	3E	14.89	126	7E	23.72	190	BE	27.03	254	FE	44.00
63	3F	15.04	127	7F	23.85	191	BF	27.29	255	FF	44.27

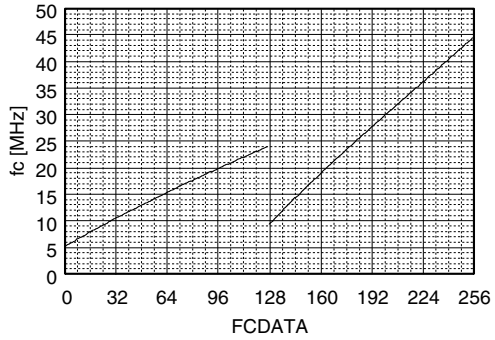


Figure 1. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

R_{ISET}

R_{ISET} controls the internal current source, and its connection is essential. The recommended value (R_{ISET}) is 1.8kΩ. In disable mode and filter bypass mode, the ISET pin is high impedance, and no current flows into R_{ISET}.

Note. A value other than 1.8kΩ will change the current consumption of SM5308AS. In the determination of resistance value, caution should be taken to ensure the power dissipation does not exceed the absolute maximum rating for the package.

Half fc Mode

In half fc mode, the CH-2 and CH-3 cutoff frequency is 1/2 that of the CH-1 cutoff frequency setting. Half fc mode is useful for systems where the sampling frequency varies due to luminance (Y) and color difference signal (Cr, Cb) requirements as in component signals.

Group Delay Characteristics

The group delay varies with the cutoff frequency setting, as shown in figure 3. Note also that in half fc mode, the group delay between CH-1 and CH-2/CH-3 varies.

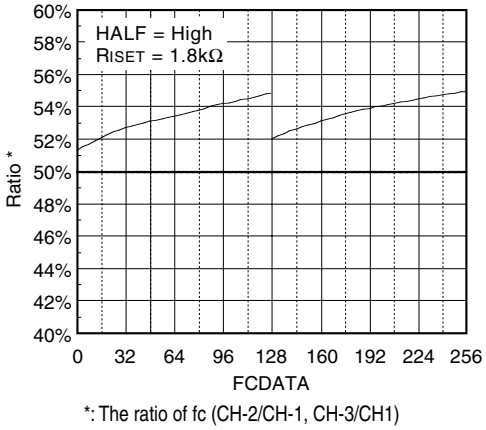


Figure 2. Cutoff frequency ratio (half fc mode)

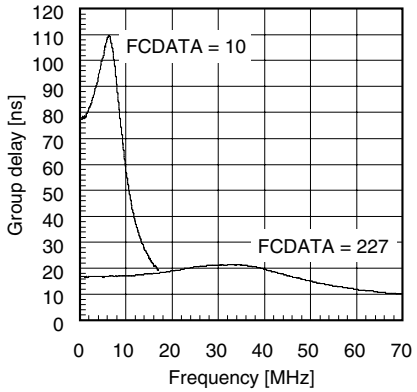


Figure 3. Group delay characteristics

Filter Bypass Mode

In filter bypass mode, the internal lowpass filter in SM5308AS is bypassed and the signal is input to the output buffer stage directly. In filter bypass mode, the input type and output gain are set just as for filter mode. But the cutoff frequency setting and fc mode setting have no effect on the outputs. In this mode, the passband frequency is 80MHz (typ), which can support SXGA-class signals.

Power-ON Reset

When power is applied, an internal power-ON reset circuit operates initializing the internal register flags to their default settings. At power-ON, all supplies should be applied simultaneously.

Reference Voltage (REF)

The REFn pins (n = 1, 2, 3) are internal reference voltage outputs. A 10 μF capacitor connected between pin and ground is recommended for stability of movement. REF1, REF2, and REF3 are independent reference voltage outputs, and have no correspondence with settings of CH-1, CH-2, and CH-3. In disable mode, they are high impedance outputs.

USAGE PRECAUTIONS

Slave Address (94h) Setting

When slave address 94h is used, the ADS input must be left open circuit. In this case, an external resistor should be connected as shown in figure 4 to reduce the risk of malfunction in the I^2C-BUS interface due to large external spikes or other noise invaded from outside. The recommended value is 10kΩ.

Direct Input Mode

In direct input mode, the signal is connected to the input without a capacitor. However, the input DC voltage range varies with the mode setting, hence the signal must be appropriately biased for the corresponding mode. The recommended LOW-level voltage (V_L) and HIGH-level voltage (V_H) for each mode is shown in table 3 (see figure 5, V_{CC} = 5V). If the input voltage exceeds these limits, be careful because harmonic distortion may occur in the output signal. (For preventing the device breakdown, input bottom voltage and top voltage should be set within the absolute maximum ratings.)

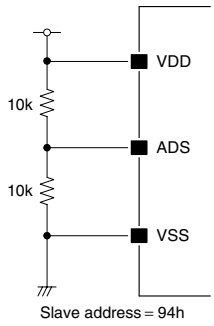


Figure 4. Slave address 94h setting

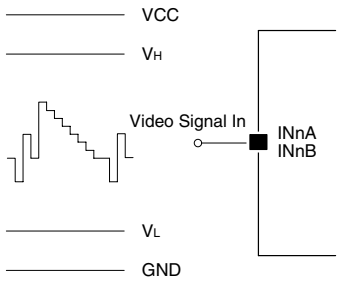


Figure 5. Direct input mode

Table 3. Direct mode recommended input DC voltage range (V_{CC} = 5V)

Mode setting	Gain	fc mode	Filter/Bypass mode	Channel	V_L [V]	V_H [V]
h0	0dB	Standard	Filter	CH-1	1.3	2.9
				CH-2, CH-3		
i0		Half		CH-1	1.3	2.9
				CH-2, CH-3	1.4	2.9
j0		–	Bypass	CH-1	1.1	3.3
				CH-2, CH-3		
h6	6dB	Standard	Filter	CH-1	1.7	3.0
				CH-2, CH-3		
i6		Half		CH-1	1.7	3.0
				CH-2, CH-3	1.7	3.0
j6		–	Bypass	CH-1	1.6	3.0
				CH-2, CH-3		

Power Supply Invest Timing

The SM5308AS uses 2-type power supply, analog one (VCC1, VCC2, VCC3) and digital one (VDD). Therefore all power supply pins should be forced voltage at the same time power supply invested. In the case analog power supply and digital one are set up simultaneously, composing system the time-lag to makes short time as standard under 1ms is need. And if voltage of digital power supply comes higher than one of analog power supply, it is necessary to set voltage of digital power supply to make potential difference bellow 100mV as compared with voltage of analog one.

TYPICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{DD} = 5.0V, Ta = 25°C, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, unless otherwise noted.

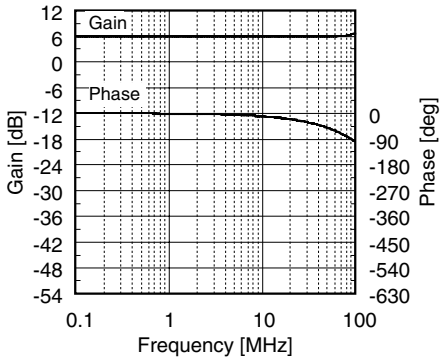


Figure 6. Gain and Phase characteristics (6dB, filter bypass mode)

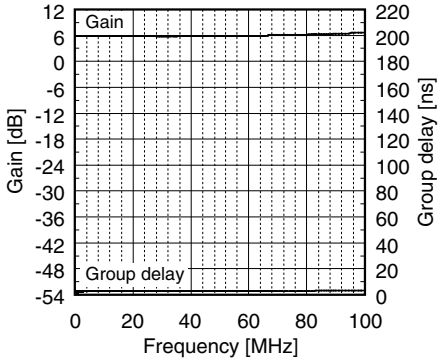


Figure 7. Gain and Group delay characteristics (6dB, filter bypass mode)

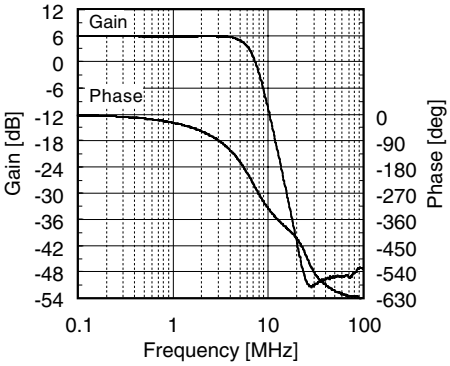


Figure 8. Gain and Phase characteristics (6dB, standard fc mode, FCDATA = 10)

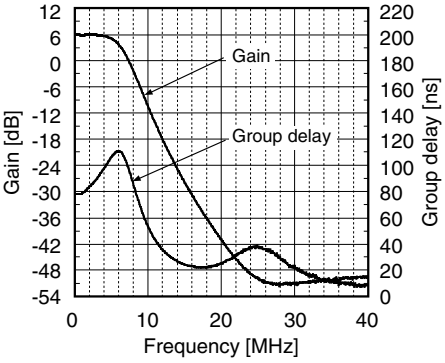


Figure 9. Gain and Group delay characteristics (6dB, standard fc mode, FCDATA = 10)

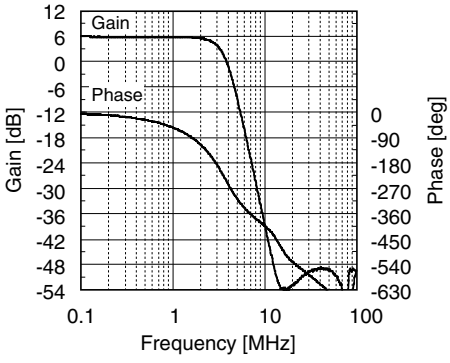


Figure 10. Gain and Phase characteristics (6dB, half fc mode, FCDATA = 10)

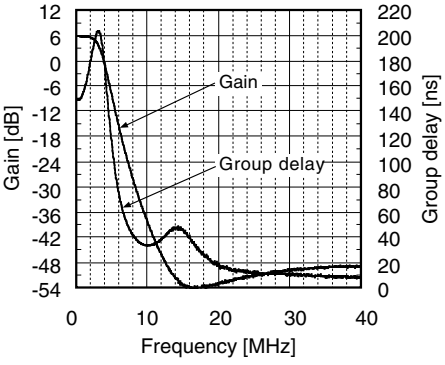


Figure 11. Gain and Group delay characteristics (6dB, half fc mode, FCDATA = 10)

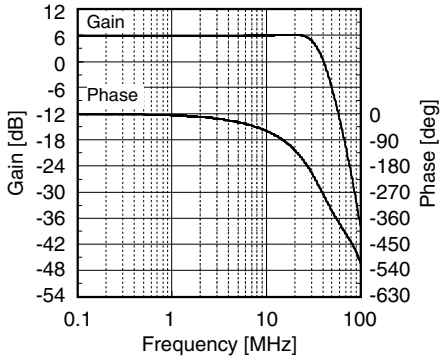


Figure 12. Gain and Phase characteristics (6dB, standard fc mode, FCDATA = 227)

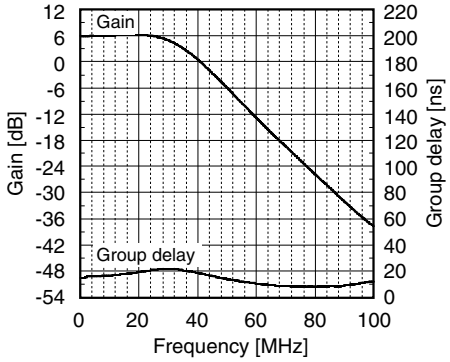


Figure 13. Gain and Group delay characteristics (6dB, standard fc mode, FCDATA = 227)

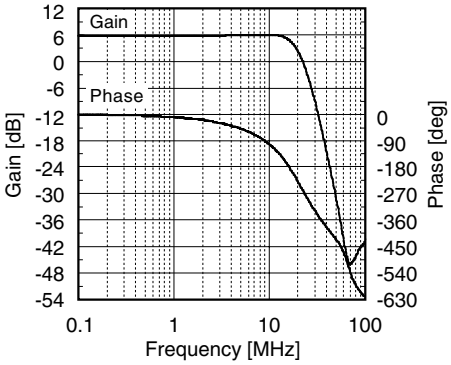


Figure 14. Gain and Phase characteristics (6dB, half fc mode, FCDATA = 227)

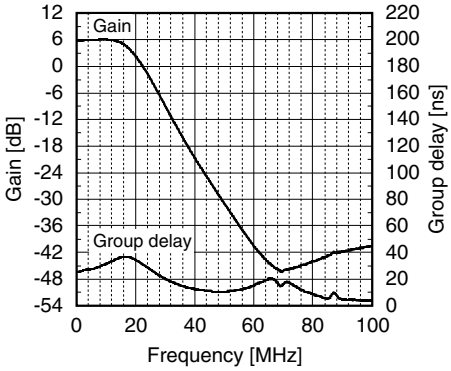


Figure 15. Gain and Group delay characteristics (6dB, half fc mode, FCDATA = 227)

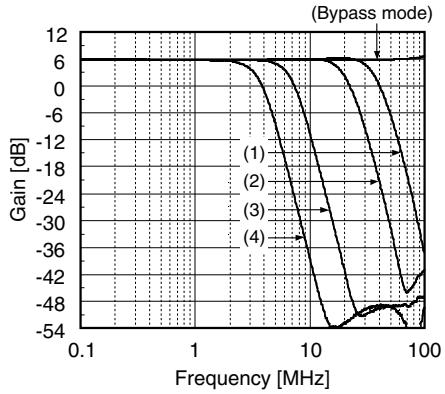


Figure 16. Gain vs. FCDATA, fc mode (6dB)

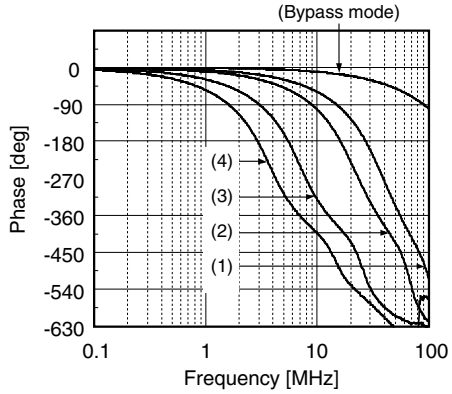


Figure 17. Phase vs. FCDATA, fc mode (6dB)

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half

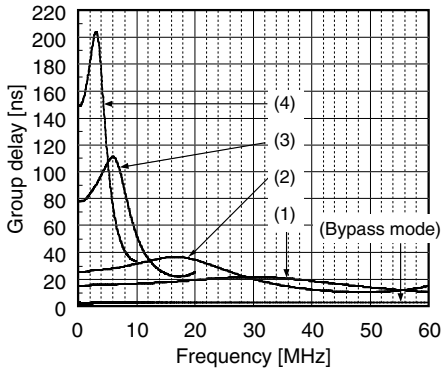


Figure 18. Group delay vs. FCDATA, fc mode (6dB)

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half