

OVERVIEW

The SM5301CS is a video filter LSI with buffered outputs for VESA-standard ATSC digital TV. The filter employs a 5-order Butterworth lowpass filter configuration. The filter characteristics have been optimized for minimal overshoot and flat group delay, it has a variable cutoff frequency and guaranteed driver-stage channel gain difference and phase difference values.

FEATURES

- Supply voltage: $5V \pm 10\%$
- VESA-standard ATSC digital TV RGB/YUV video filters
- RGB/YUV switching multiplexer function
- 0dB, 6dB gain switching function (input-to-output AC signal gain)
- Channel-to-channel gain difference: 0.5dB ($\pm 5\%$ supply voltage variation)
- Channel-to-channel phase difference: 3.5 degree
- Output signal harmonic distortion (all channels): 1.5%
- Cutoff frequency: 5 to 37MHz variable
- Package: 28-pin HSOP (Pb free)

APPLICATIONS

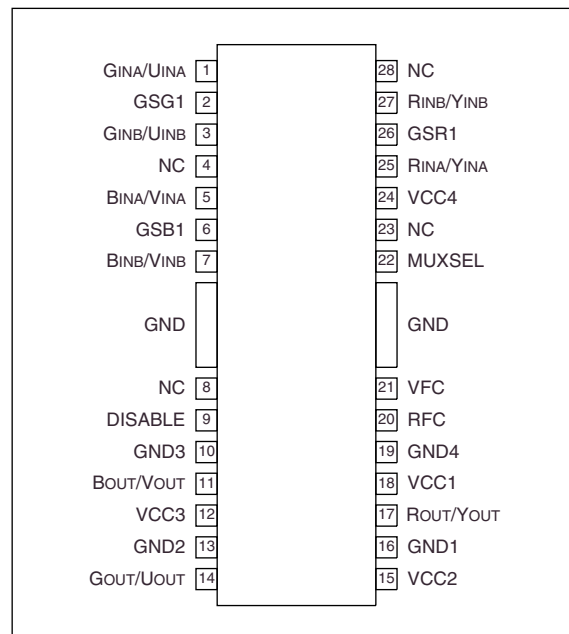
- Set-top boxes
- Digital television
- DVD players

ORDERING INFORMATION

Device	Package
SM5301CS	28-pin HSOP

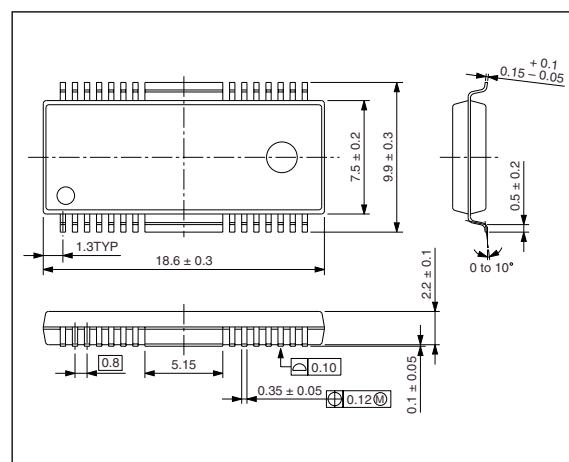
PINOUT

(Top view)

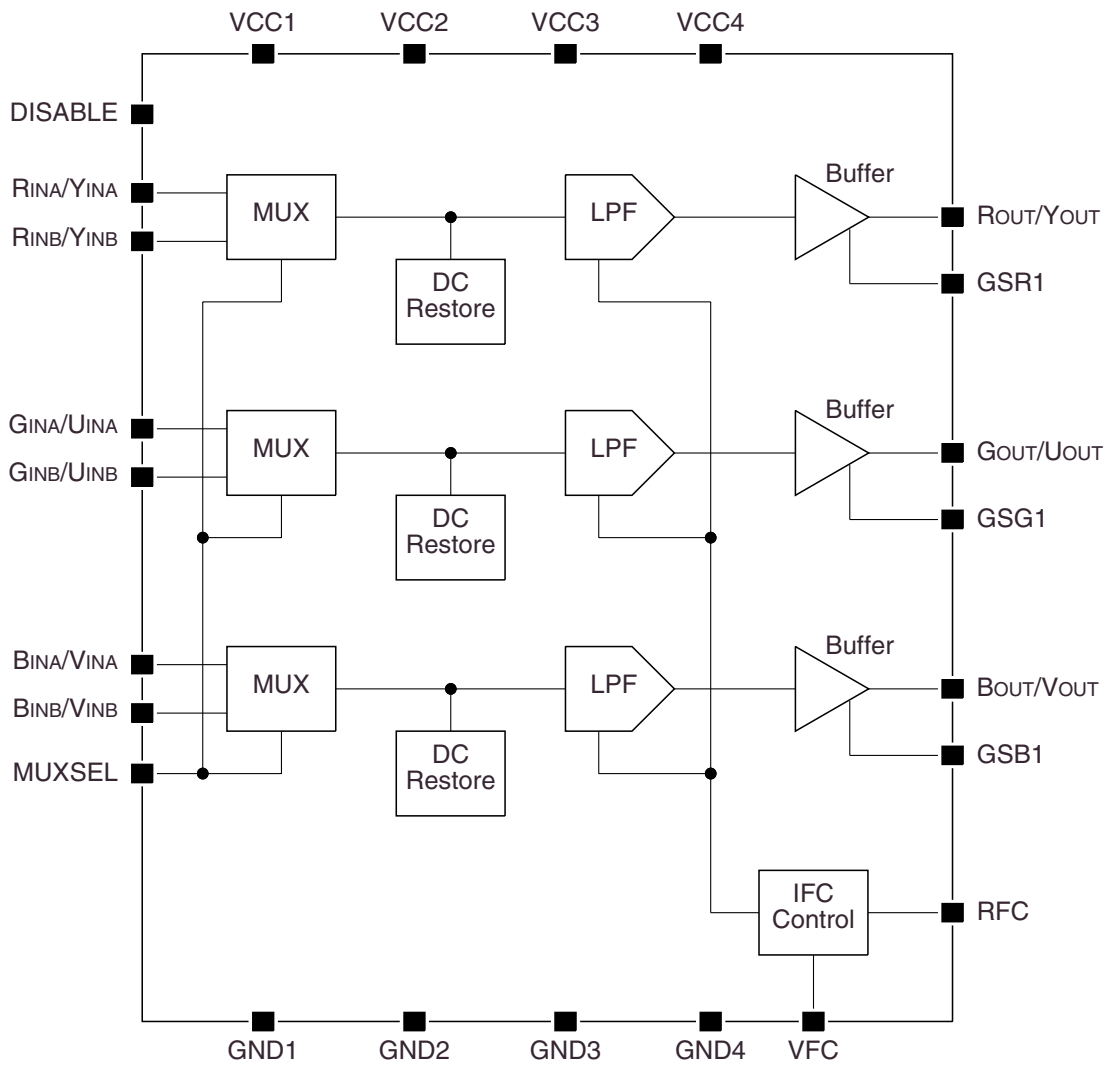


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	G_{INA}/U_{INA}	I	Analog G_{INA} or U_{INA} signal input
2	GSG1	I	G_{OUT}/U_{OUT} output buffer gain set input
3	G_{INB}/U_{INB}	I	Analog G_{INB} or U_{INB} signal input
4	NC	–	No connection (leave open or connect to ground)
5	B_{INA}/V_{INA}	I	Analog B_{INA} or V_{INA} signal input
6	GSB1	I	B_{OUT}/V_{OUT} output buffer gain set input
7	B_{INB}/V_{INB}	I	Analog B_{INB} or V_{INB} signal input
8	NC	–	No connection (leave open or connect to ground)
9	DISABLE	I	Power save function. Built-in pull-down resistor. L: Enable H: Disable (Output pins: R_{OUT}/Y_{OUT} , G_{OUT}/U_{OUT} , and B_{OUT}/V_{OUT} are high impedance.)
10	GND3	–	Analog ground
11	B_{OUT}/V_{OUT}	O	B/V signal output
12	VCC3	–	Analog 5V supply
13	GND2	–	Analog ground
14	G_{OUT}/U_{OUT}	O	G/U signal output
15	VCC2	–	Analog 5V supply
16	GND1	–	Analog ground
17	R_{OUT}/Y_{OUT}	O	R/Y signal output
18	VCC1	–	Analog 5V supply
19	GND4	–	Analog ground
20	RFC	O	LPF (lowpass filter) cutoff frequency setting resistor connection
21	VFC	I	LPF (lowpass filter) cutoff frequency setting voltage input
22	MUXSEL	I	Input select signal L: \times_{INA} pin select H: \times_{INB} pin select
23	NC	–	No connection (leave open or connect to ground)
24	VCC4	–	Analog 5V supply
25	R_{INA}/Y_{INA}	I	Analog R_{INA} or Y_{INA} signal input
26	GSR1	I	R_{OUT}/Y_{OUT} output buffer gain set input
27	R_{INB}/Y_{INB}	I	Analog R_{INB} or Y_{INB} signal input
28	NC	–	No connection (leave open or connect to ground)

PIN EQUIVALENT CIRCUITS

Number	Name	I/O	Equivalent circuit
25 27 1 3 5 7	R _{INA} /Y _{INA} R _{INB} /Y _{INB} G _{INA} /U _{INA} G _{INB} /U _{INB} B _{INA} /V _{INA} B _{INB} /V _{INB}	I	
17 14 11	R _{OUT} /Y _{OUT} G _{OUT} /U _{OUT} B _{OUT} /V _{OUT}	O	
20	RFC	O	
21	VFC	I	
26 2 6	GSR1 GSG1 GAB1	I	
9 22	DISABLE MUXSEL	I	

Note. Resistance values indicate design values.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{CC}		- 0.3 to 7.0	V
Storage temperature range	T_{stg}		- 55 to + 125	°C
Power dissipation 1 ¹	P_{D1}		1.0	W
Power dissipation 2 ²	P_{D2}		0.9	W
Input pin voltage	V_{IN}	GND1 = GND2 = GND3 = GND4 = GND = 0V	GND - 0.3 to $V_{CC} + 0.3$	V

1. When mounted on a substrate: mounted on a 111 × 80 × 1.6mm glass-epoxy substrate with 90% copper (Cu) wiring factor, 0m/s air flow, and $T_a = -25$ to 70°C.
2. When mounted on a substrate: mounted on a 111 × 80 × 1.6mm glass-epoxy substrate with 90% copper (Cu) wiring factor, 0m/s air flow, and $T_a = 70$ to 80°C.

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{CC}		4.5 to 5.5	V
Operating ambient temperature	T_a		- 25 to 85	°C

Electrical Characteristics

$V_{CC} = 4.5$ to $5.5V$, $T_a = -25$ to $85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Supply current 1	I_{CC1}	$V_{CC} = 5.5V$, $R_{FC} = 820\Omega$ to GND, $V_{FC} = 0.2V$, DISABLE = "L"	70	100	130	mA	I
Supply current 2	I_{CC2}	$V_{CC} = 5.5V$, $R_{FC} = 820\Omega$ to GND, $V_{FC} = 1.6V$, DISABLE = "L"	90	120	160	mA	I
Supply current 3	I_{CC3}	$V_{CC} = 5.5V$, $R_{FC} = 820\Omega$ to GND, $V_{FC} = 0.2V$, DISABLE = "H"	0	2.5	5	mA	I
Output gain error 1	ΔA_{V1}	Gain = 0dB/6dB, $V_{CC} = 4.75$ to $5.25V$, $T_a = 0$ to $70^\circ C$	-0.5	-	+0.5	dB	I
Output gain error 2	ΔA_{V2}	Gain = 0dB/6dB, $T_a = -25$ to $85^\circ C$	-1	-	+1	dB	I
Maximum output voltage	V_{out2}	$R_L = 75\Omega$ to GND, Gain = 6dB	2.4	-	-	Vp-p	I
DISABLE-mode input impedance (pull-down)	R_{IN1}	R_{INA}/Y_{INA} , R_{INB}/Y_{INB} , G_{INA}/U_{INA} , G_{INB}/U_{INB} , B_{INA}/V_{INA} , B_{INB}/V_{INB}	-	50	-	k Ω	I
Clamp response time	T_{clamp}	Time for 90% output signal change for 10mV input signal, $C_{IN} = 0.1\mu F$	-	8	-	ms	II
Maximum input amplitude	V_I	AC coupling, Gain = 6dB	-	-	1.4	Vp-p	I
Maximum overshoot 1	V_{OS1}	1.0Vp-p pulse input, bias input shown in Figure 1, Gain = 6dB	-	10	-	%	II
Maximum overshoot 2	V_{OS2}	1.0Vp-p pulse input, bias input shown in Figure 1, Gain = 0dB	-	10	-	%	II
Maximum load capacitance	C_L	B_{OUT}/V_{OUT} , G_{OUT}/U_{OUT} , R_{OUT}/Y_{OUT}	-	-	15	pF	II
Output drive load	R_L	one load unit = 150Ω	-	-	2	load	I
Channel-to-channel gain difference	dG	Between R/G/B, fc/2 [Hz]	-	-	0.5	dB	I
Channel-to-channel phase difference	d ϕ	Between R/G/B, fc/2 [Hz]	-	3.5	-	degree	II
Output harmonic distortion 1	T_{HD1}	Gain = 6dB, $V_{IN} = 1.0Vp-p$, $f = 1MHz$, bias input shown in Figure 1	-	1.5	-	%	II
Output harmonic distortion 2	T_{HD2}	Gain = 0dB, $V_{IN} = 1.4Vp-p$, $f = 1MHz$, bias input shown in Figure 1	-	1.5	-	%	II
Power supply rejection ratio	PSRR	$V_{CC} = 0.5Vp-p$, $f = 100kHz$	-	35	-	dB	II
Logic HIGH-level input voltage 1	V_{IH1}	DISABLE, MUXSEL	2.5	-	-	V	I
Logic LOW-level input voltage 1	V_{IL1}	DISABLE, MUXSEL	-	-	1.0	V	I
Logic HIGH-level input voltage 2	V_{IH2}	GSB1, GSG1, GSR1	$V_{CC} - 0.5$	-	-	V	I
Logic LOW-level input voltage 2	V_{IL2}	GSB1, GSG1, GSR1	-	-	0.5	V	I
Logic pull-up resistance	R_{IN2}	GSB1, GSG1, GSR1	-	40	-	k Ω	I
Logic pull-down resistance	R_{IN3}	DISABLE, MUXSEL	-	50	-	k Ω	I
Input current	I_{IN}	Input voltage 3.0V, $T_a = 25^\circ C$, R_{INA}/Y_{INA} , R_{INB}/Y_{INB} , G_{INA}/U_{INA} , G_{INB}/U_{INB} , B_{INA}/V_{INA} , B_{INB}/V_{INB}	0.33	-	-	μA	I

Filter Mode Characteristics

$V_{CC} = 4.5$ to $5.5V$, $T_a = -25$ to $85^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level	
			min	typ	max			
Cutoff frequency adjustment range	F_C	$T_a=25^{\circ}C$ (see Figure 2)	5.8	–	37	MHz	I	
Cutoff frequency error	ΔF_C	$T_a = 25^{\circ}C$, $V_{CC} = 5.0V$	–	–	± 20	%	I	
4fc attenuation	f_{SB}	$f_{IN} \geq 4f_c$	–	50	–	dB	II	
Output noise characteristic	V_{NOISE}	10kHz to 40MHz, output gain = 6dB	–	1.0	–	mV _{RMS}	II	
Crosstalk	X_{TALK}	Between 2 channels with input 0.5V _{p-p} 1MHz	–	–47	–	dB	II	
Multiplexer crosstalk	X_{TALK}	Between MUX A–B	–	–49	–	dB	II	
Channel-to-channel group delay	T_{PD}	Each input = 500kHz	–	10	–	ns	II	
Group delay variation ¹	ΔT_{PD1}	Gain = 0dB/6dB, Fc = 6.7MHz (500kHz)	to 3.58MHz	–	9	–	ns	II
			to 4.43MHz	–	15	–	ns	II
	ΔT_{PD2}	Gain = 0dB/6dB, Fc = 24MHz (500kHz)	to 3.58MHz	–	1	–	ns	II
			to 4.43MHz	–	1	–	ns	II
			to 10MHz	–	2	–	ns	II
	ΔT_{PD3}	Gain = 0dB/6dB, Fc = 36MHz (1MHz)	to 10MHz	–	0.5	–	ns	II
to 30MHz			–	5	–	ns	II	
VFC input voltage range	VFC		0.2	–	1.6	V	I	

1. Bias input shown in Figure 1

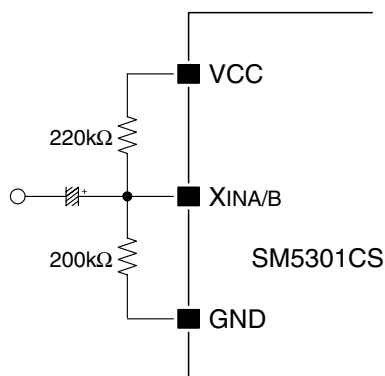


Figure 1. Input pin bias circuit diagram when measuring maximum overshoot, output harmonic distortion, and group delay variation

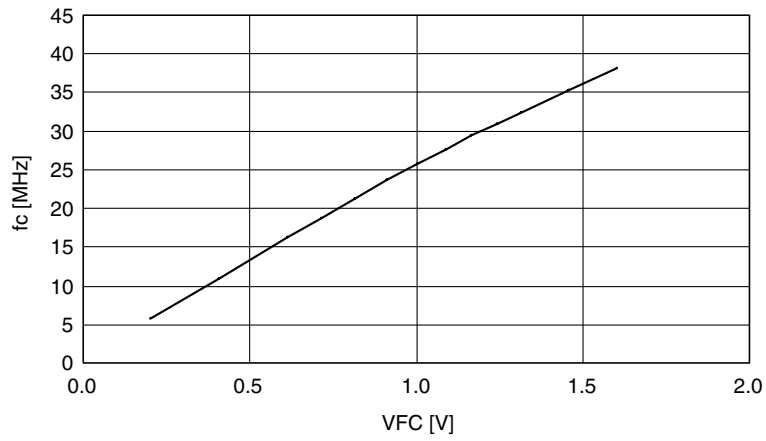
Test level

I : 100% of products tested at $T_a = +25^{\circ}C$.

II : Guaranteed as result of design and characteristics evaluation.

Table 1. Output buffer gain control

GS×1	Gain [dB]
GND	0
VCC or Open	6



RFC: 820Ω to GND

Figure 2. VFC vs. cutoff frequency

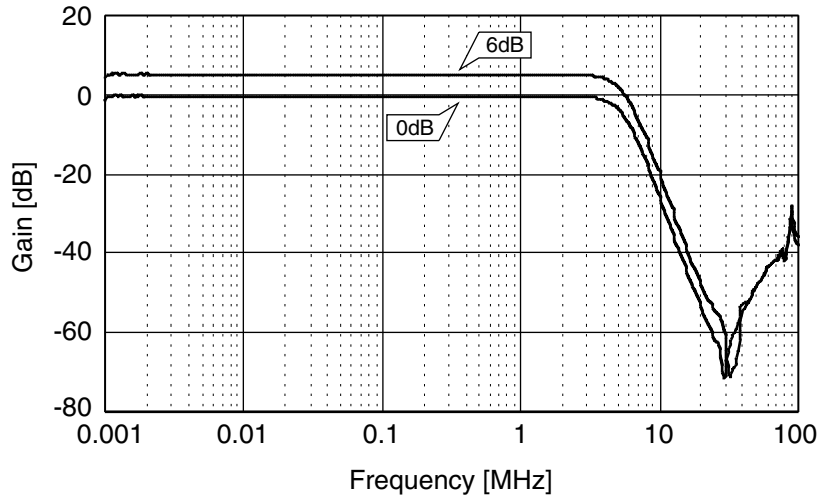


Figure 3. Frequency response (VFC = 0.2V)

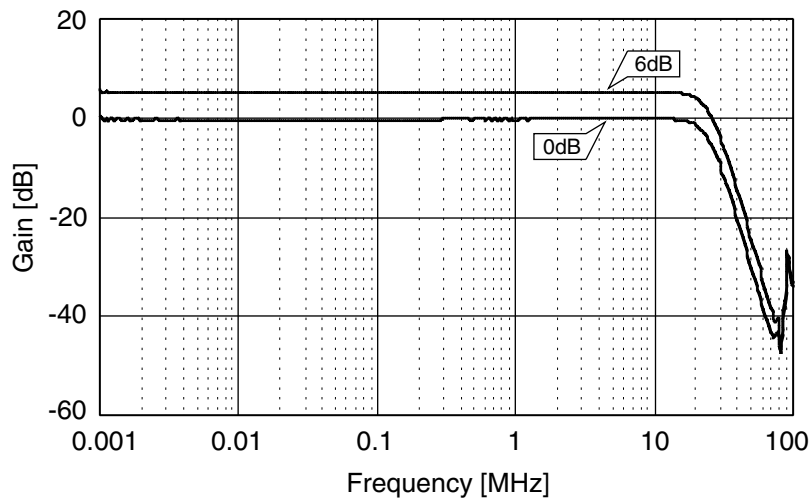


Figure 4. Frequency response (VFC = 1.0V)

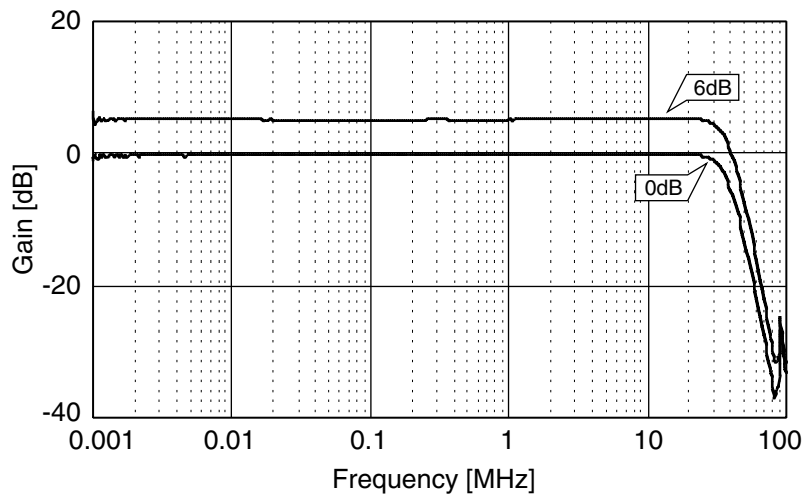
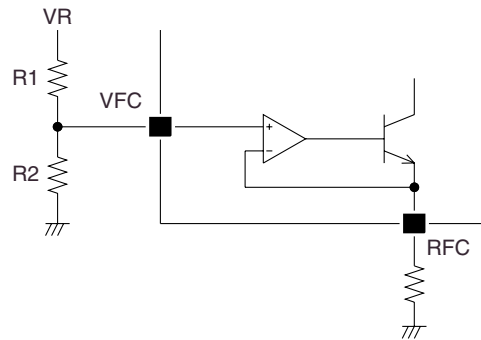


Figure 5. Frequency response (VFC = 1.6V)

Adjusting the Cutoff Frequency

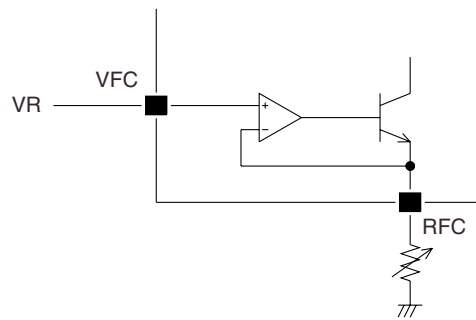
Constant-voltage control 1

Cutoff frequency control using a reference voltage V_R generated by voltage divider formed by R_1 and R_2 .



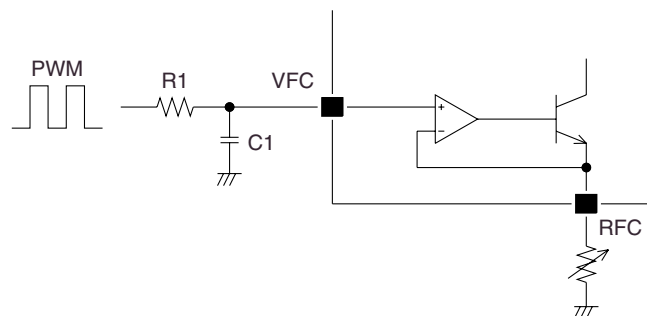
Constant-voltage control 2

Cutoff frequency control by adjusting the resistance connected to RFC.



PWM control

Cutoff frequency control by smoothing the PWM signal, using R_1 and C_1 , input to VFC.



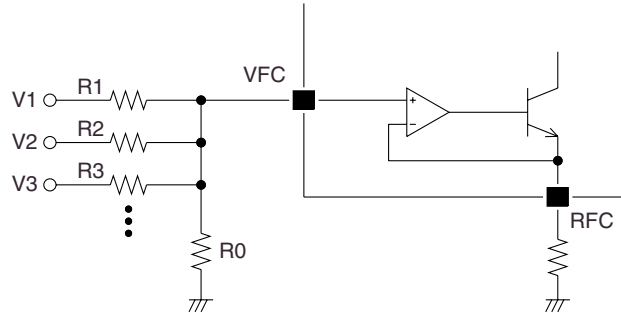
When $V_{FC} = 0.2V$ $V_{DD} = 3.3V$, 6% duty drive
 $V_{DD} = 5.0V$, 4% duty drive

When $V_{FC} = 1.6V$ $V_{DD} = 3.3V$, 48% duty drive
 $V_{DD} = 5.0V$, 32% duty drive

Note: The resistor connected to RFC can affect the cutoff frequency response, so a high-precision component should be used. It is recommended to set the RC filter cutoff frequency to $< 1/100f_c$ of the PWM waveform frequency.

Resistor switch control

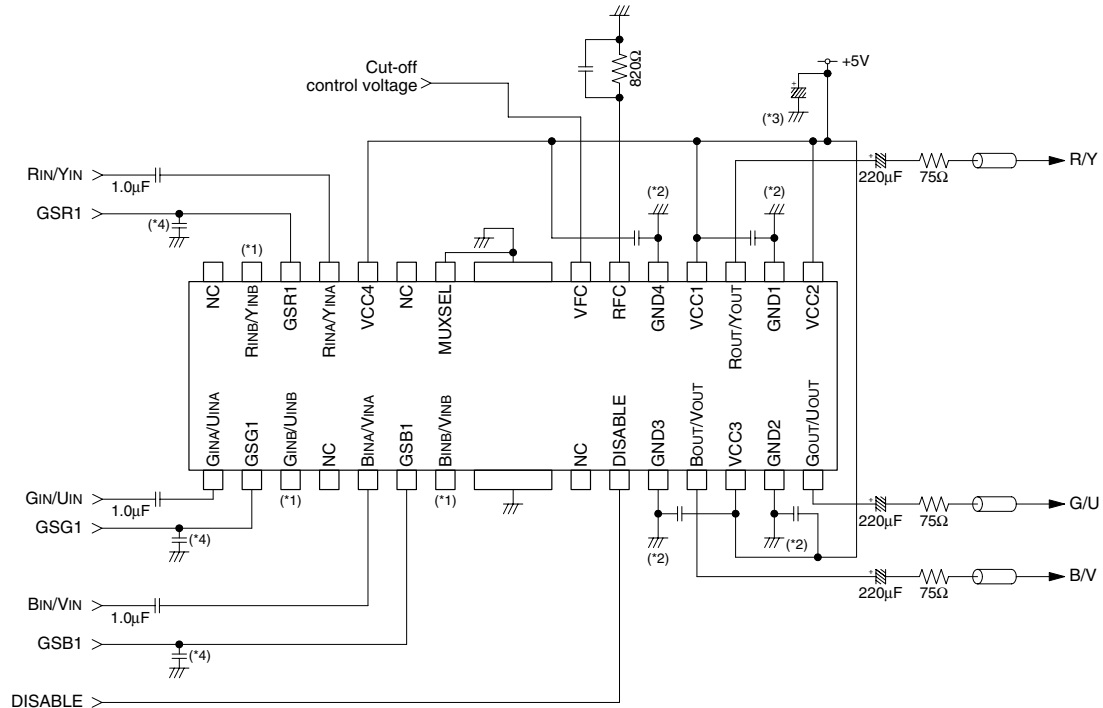
The VFC voltage can be controlled using multi-logic voltage levels switching inputs to a voltage divider resistor network.



The VFC voltage is determined by the logic voltage (V1, V2, V3) and the corresponding voltage divider resistor network.

TYPICAL APPLICATION CIRCUITS

ATSC Digital TV Application



- (*1) Pins without an input signal, set by MUXSEL, should be left open or tied to GND.
- (*2) Connect $4 \times 0.1\mu\text{F}$ capacitor between the supply pins close to the IC.
- (*3) Connect a $47\mu\text{F}$ capacitor between the supply pins close to the IC.
- (*4) GS \times 1 and GS \times 2 pins are 3-level pins. Connect a capacitor if an error occurs due to external noise. Also, if open-circuit, the internal impedance and external capacitance (C) form an RC network. When power is applied, the open-circuit potential rises with time constant $\tau = C \times 10\text{k}$ (sec).
- (*5) Printed circuit board supply wiring
- If the supply is used for other digital circuits, there is a possibility that noise will be introduced. Accordingly, these circuits should be connected to the application's analog supply.
 - Ground-plane wiring should be performed, as much as possible, to provide low GND line impedance.
 - If ground-plane wiring up to the GND pins is difficult, the ground plane should be as close to the IC as possible with a separate wire to each GND pin.
- (*6) The tab (radiation fin) between 7 pin and 8 pin and between 21 pin and 22 pin should be connected to the large ground plane as much as possible for radiation.

Input Capacitor and Cutoff Frequency

The capacitor connected to pins R_{iNA}/Y_{iNA} , R_{iNB}/Y_{iNB} , G_{iNA}/U_{iNB} , G_{iNB}/U_{iNB} , B_{iNA}/V_{iNA} , and B_{iNB}/V_{iNB} forms a highpass filter (HPF) with the internal impedance.

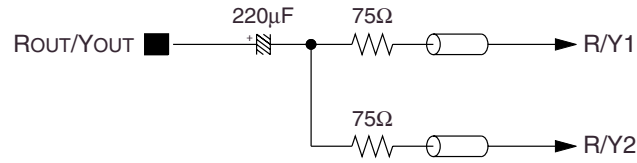
The HPF cutoff frequency is given by the following equation.

$$f_c = \frac{1}{2\pi CR}$$

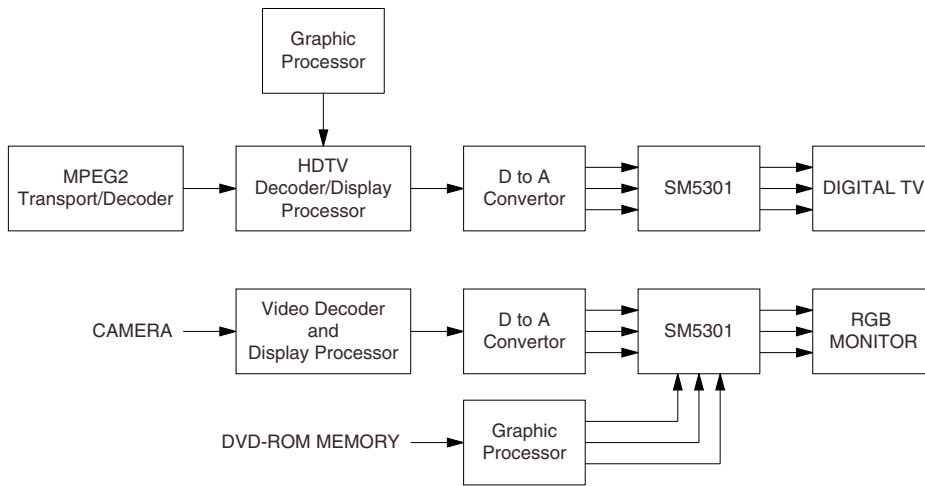
(C: input capacitance, R: signal input impedance = $12\text{M}\Omega$ (typ))

2-load Output Connection

R_{OUT}/Y_{OUT} output 2-load connection (similarly for G_{OUT}/U_{OUT}, B_{OUT}/V_{OUT} outputs)



Digital TV Receiver and HDTV Decoder Box



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