

## OVERVIEW

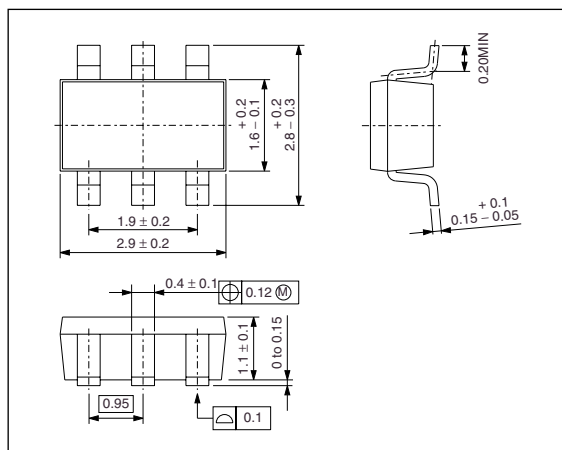
The SM5023 series are 3rd overtone crystal oscillator module ICs. They feature built-in oscillator capacitors with excellent frequency response. As cutoff frequency can be configured by using an external feedback resistor  $R_{fo}$ , a favorable 3rd overtone oscillation can be realized with a few external components. The oscillator circuit characteristics are optimized for a 3rd overtone oscillation by round blank. They also feature a built-in output buffer with high output drive capability and are available in miniature 6-pin package, making them ideal as DIP-type crystal oscillators.

## FEATURES

- Operating supply voltage range
  - 3V operation: 2.7 to 3.6V
  - 5V operation: 4.5 to 5.5V
- 4MHz to 70MHz operating frequency range  
(Oscillation frequency is settable by external components)
- $-40$  to  $85^{\circ}\text{C}$  operating temperature range
- Oscillator capacitors  $C_G$ ,  $C_D$  built-in  
(BN×H version only)
- Cutoff frequency setting using external feedback resistor  $R_{fo}$
- Output drive capability
  - 8mA ( $V_{DD} = 2.7\text{V}$ )
  - 16mA ( $V_{DD} = 4.5\text{V}$ )
- Output three-state function built-in
  - High impedance output in standby mode
- CMOS output duty level (1/2VDD)
- Molybdenum-gate CMOS process
- Package: SOT23-6 (SM5023×××H)

## PACKAGE DIMENSIONS

(Unit: mm)



## APPLICATIONS

- DIP-type crystal oscillator modules

## SERIES CONFIGURATION

Version	Operating Supply voltage range [V]	Recommended operating frequency range <sup>1</sup> [MHz]	Oscillator circuit constants				Output duty level	Standby mode	
			gm ratio	Built-in capacitance		Rf [kΩ]		Oscillator	Output state
				C <sub>G</sub> [pF]	C <sub>D</sub> [pF]				
SM5023BNDH	2.7 to 3.6	22 to 70	3	8	15	—	CMOS	Operation	Hi-Z
	4.5 to 5.5								
SM5023BNEH	2.7 to 3.6	50 to 70	4	8	12	—	CMOS	Operation	Hi-Z
SM5023CNDH	2.7 to 3.6	4 to 70	3	—	—	—	CMOS	Operation	Hi-Z
	4.5 to 5.5								

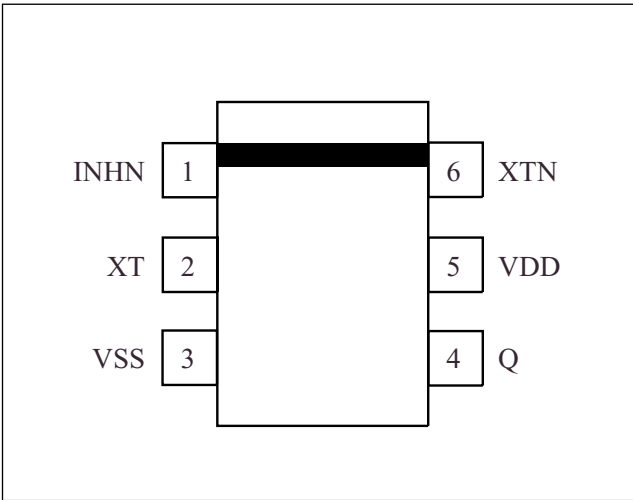
1. The 3rd overtone frequency range using an external resistor to set the cutoff frequency. The recommended operating frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillator frequency band is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

## ORDERING INFORMATION

Device	Package
SM5023×××H	SOT23-6

PINOUT

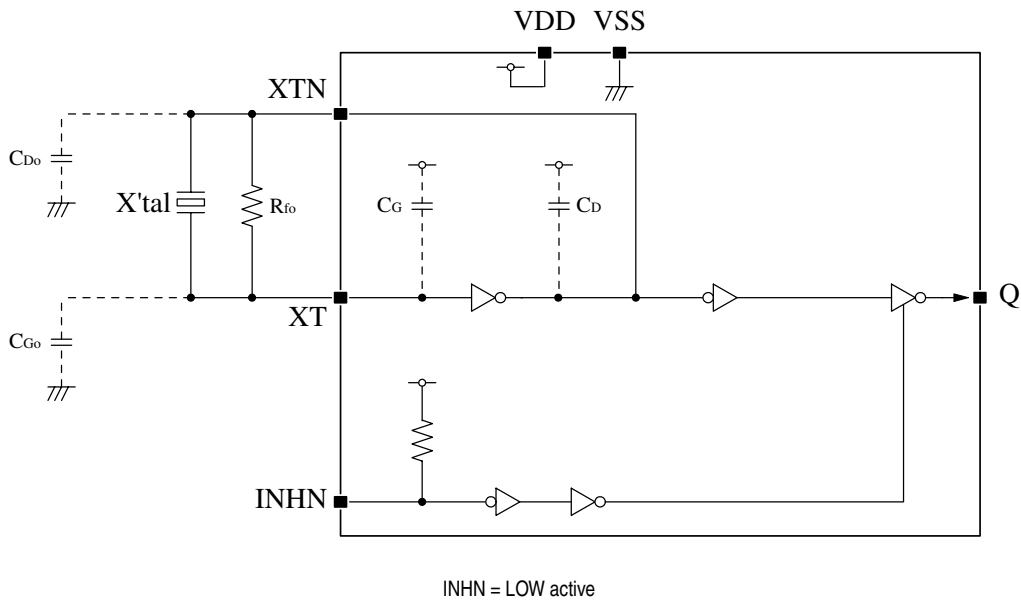
(Top view)



PIN DESCRIPTION

Name	I/O	Description	
INHN	I	Output state control input. High impedance when LOW. Pull-up resistor built-in.	
XT	I	Amplifier input	Crystal connection pins. Crystal is connected between XT and XTN.
XTN	O	Amplifier output	
VSS	–	Ground	
Q	O	Output. $f_O$ (XT pin input frequency)	
VDD	–	Supply voltage	

BLOCK DIAGRAM



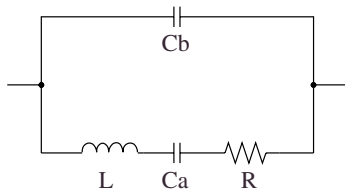
## FUNCTIONAL DESCRIPTION

### Standby Function

When INHN goes LOW, the oscillator output on Q becomes high impedance.

INHN	Q	Oscillator
HIGH (or open)	$f_0$	Normal operation
LOW	High impedance	Normal operation

### Current consumption and Output waveform with NPC's standard crystal



f [MHz]	R [ $\Omega$ ]	L [mH]	Ca [fF]	Cb [pF]
30	18.62	16.24	1.733	5.337
40	20.53	11.34	1.396	3.989
50	22.17	7.40	1.370	4.105
60	22.20	5.05	1.388	4.226
70	25.42	4.18	1.254	5.170

## SPECIFICATIONS

### Absolute Maximum Ratings

$V_{SS} = 0V$

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD}$	−0.5 to +7.0	V
Input voltage range	$V_{IN}$	−0.5 to $V_{DD} + 0.5$	V
Output voltage range	$V_{OUT}$	−0.5 to $V_{DD} + 0.5$	V
Operating temperature range	$T_{opr}$	−40 to +85	°C
Storage temperature range	$T_{STG}$	−55 to +125	°C
Output current	$I_{OUT}$	20	mA
Power dissipation	$P_D$	250	mW

### Recommended Operating Conditions

#### 3V operation: SM5023BNDH, BNEH, CNDH

$V_{SS} = 0V$ ,  $f \leq 70MHz$ ,  $C_L \leq 15pF$  unless otherwise noted.

Parameter	Symbol	Rating			Unit
Operating supply voltage	$V_{DD}$	2.7	–	3.6	V
Input voltage	$V_{IN}$	$V_{SS}$	–	$V_{DD}$	V
Operating temperature	$T_{OPR}$	−20	–	+80	°C

#### 5V operation: SM5023BNDH, CNDH

$V_{SS} = 0V$ ,  $f \leq 50MHz$ ,  $C_L \leq 50pF$  unless otherwise noted.

$V_{SS} = 0V$ ,  $f \leq 70MHz$ ,  $C_L \leq 15pF$  unless otherwise noted.

Parameter	Symbol	Rating			Unit
Operating supply voltage	$V_{DD}$	4.5	–	5.5	V
Input voltage	$V_{IN}$	$V_{SS}$	–	$V_{DD}$	V
Operating temperature	$T_{OPR}$	−40	–	+85	°C

## Electrical Characteristics

## 3V operation: SM5023BNDH, BNEH, CNDH

$V_{DD} = 2.7$  to  $3.6$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $+80^\circ\text{C}$  unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	$V_{OH}$	Q: Measurement cct 1, $V_{DD} = 2.7$ V, $I_{OH} = 8$ mA	2.1	2.4	–	V
LOW-level output voltage	$V_{OL}$	Q: Measurement cct 2, $V_{DD} = 2.7$ V, $I_{OL} = 8$ mA	–	0.3	0.5	V
HIGH-level input voltage	$V_{IH}$	INHN	2.0	–	–	V
LOW-level input voltage	$V_{IL}$	INHN	–	–	0.5	V
Output leakage current	$I_Z$	Q: Measurement cct 2, INHN = LOW, $V_{DD} = 3.3$ V				
		$V_{OH} = V_{DD}$	–	–	10	$\mu\text{A}$
		$V_{OL} = V_{SS}$	–	–	10	$\mu\text{A}$
Current consumption	$I_{DD}$	Measurement cct 3, load cct 1, INHN = open, $C_L = 15$ pF, $f = 70$ MHz	–	15	30	mA
INHN pull-up resistance	$R_{UP}$	Measurement cct 4	25	100	250	$k\Omega$
Built-in capacitance	$C_G$	Design value. A monitor pattern on a wafer is tested.				
		SM5023BNDH	7.44	8	8.56	pF
		SM5023BNEH				
	$C_D$	Design value. A monitor pattern on a wafer is tested.				
		SM5023BNDH	13.95	15	16.05	pF
		SM5023BNEH	11.16	12	12.84	pF

## 5V operation: SM5023BNDH, CNDH

$V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $+85^\circ\text{C}$  unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	$V_{OH}$	Q: Measurement cct 1, $V_{DD} = 4.5$ V, $I_{OH} = 16$ mA	3.9	4.2	–	V
LOW-level output voltage	$V_{OL}$	Q: Measurement cct 2, $V_{DD} = 4.5$ V, $I_{OL} = 16$ mA	–	0.3	0.5	V
HIGH-level input voltage	$V_{IH}$	INHN	2.0	–	–	V
LOW-level input voltage	$V_{IL}$	INHN	–	–	0.8	V
Output leakage current	$I_Z$	Q: Measurement cct 2, INHN = LOW, $V_{DD} = 5.5$ V				
		$V_{OH} = V_{DD}$	–	–	10	$\mu\text{A}$
		$V_{OL} = V_{SS}$	–	–	10	$\mu\text{A}$
Current consumption	$I_{DD1}$	Measurement cct 3, load cct 1, INHN = open				
	$I_{DD2}$					
		$C_L = 15$ pF $f = 70$ MHz	–	20	40	mA
		$C_L = 50$ pF $f = 50$ MHz	–	25	50	mA
INHN pull-up resistance	$R_{UP}$	Measurement cct 4	25	100	250	$k\Omega$
Built-in capacitance	$C_G$	Design value. A monitor pattern on a wafer is tested.				
		SM5023BNDH	7.44	8	8.56	pF
	$C_D$	Design value. A monitor pattern on a wafer is tested.				
		SM5023BNDH	13.95	15	16.05	pF

## Switching Characteristics

### 3V operation: SM5023BNDH, BNEH, CNDH

$V_{DD} = 2.7$  to  $3.6V$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $+80^\circ C$  unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	$t_{r1}$	Measurement cct 5, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$ , $C_L = 15pF$	–	2.5	5	ns
Output fall time	$t_{f1}$	Measurement cct 5, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$ , $C_L = 15pF$	–	2.5	5	ns
Output duty cycle <sup>1</sup>	Duty1	Measurement cct 5, load cct 1, $V_{DD} = 3.0V$ , $T_a = 25^\circ C$ , $C_L = 15pF$ , $f \leq 70MHz$	45	–	55	%
Output disable delay time	$t_{PLZ}$	Measurement cct 5, load cct 1, $V_{DD} = 3.0V$ , $T_a = 25^\circ C$ , $C_L = 15pF$	–	–	100	ns
Output enable delay time	$t_{PZL}$		–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

### 5V operation: SM5023BNDH, CNDH

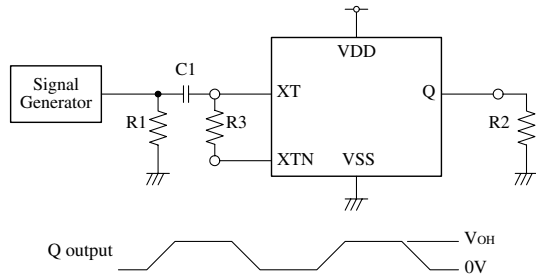
$V_{DD} = 4.5$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$  unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	$t_{r1}$	Measurement cct 5, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15pF$	–	1.5	3	ns
	$t_{r2}$		$C_L = 50pF$	–	3	6	
Output fall time	$t_{f1}$	Measurement cct 5, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15pF$	–	1.5	3	ns
	$t_{f2}$		$C_L = 50pF$	–	3	6	
Output duty cycle <sup>1</sup>	Duty1	Measurement cct 5, load cct 1, $V_{DD} = 5.0V$ , $T_a = 25^\circ C$	$C_L = 15pF$ $f \leq 70MHz$	45	–	55	%
	Duty2		$C_L = 50pF$ $f \leq 50MHz$	45	–	55	%
Output disable delay time	$t_{PLZ}$	Measurement cct 5, load cct 1, $V_{DD} = 5.0V$ , $T_a = 25^\circ C$ , $C_L = 15pF$		–	–	100	ns
Output enable delay time	$t_{PZL}$			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

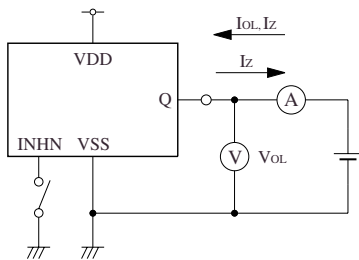
## MEASUREMENT CIRCUITS

### Measurement cct 1

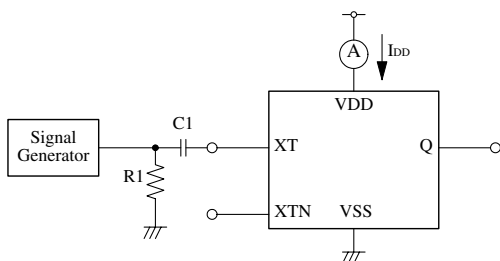


2.0Vp-p, 10MHz sine wave input signal (3V operation)  
 3.5Vp-p, 10MHz sine wave input signal (5V operation)  
 C1: 0.001μF  
 R1: 50Ω  
 R2: 263Ω (3V operation)  
 244Ω (5V operation)  
 R3: 100kΩ

### Measurement cct 2

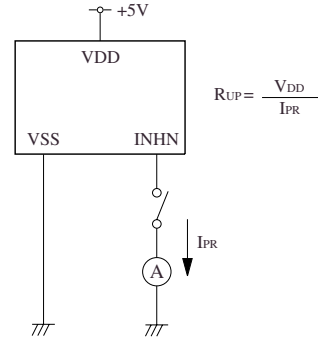


### Measurement cct 3

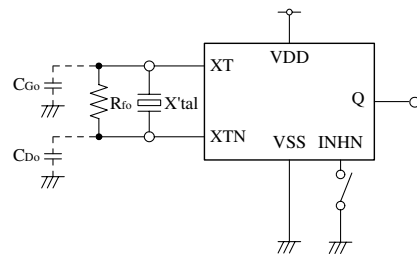


2.0Vp-p, 70MHz sine wave input signal (3V operation)  
 3.5Vp-p, 70MHz sine wave input signal (5V operation)  
 C1: 0.001μF  
 R1: 50Ω

### Measurement cct 4

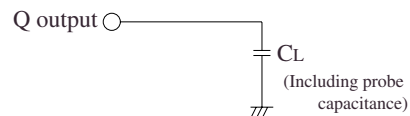


### Measurement cct 5



Crystal oscillation  
 $R_{fo}$ : 1.5kΩ (3V, 70MHz operation)  
 3.9kΩ (5V, 70MHz operation)  
 5.6kΩ (5V, 50MHz operation)  
 SM5023CNDH:  $C_{Go} = 8\text{pF}$ ,  $C_{Do} = 15\text{pF}$

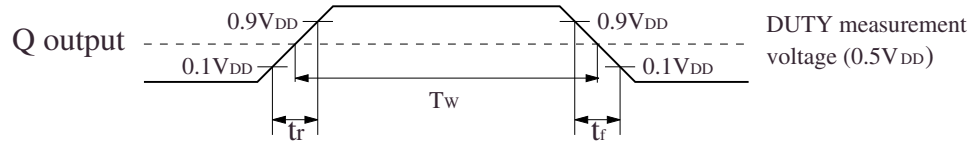
### Load cct 1



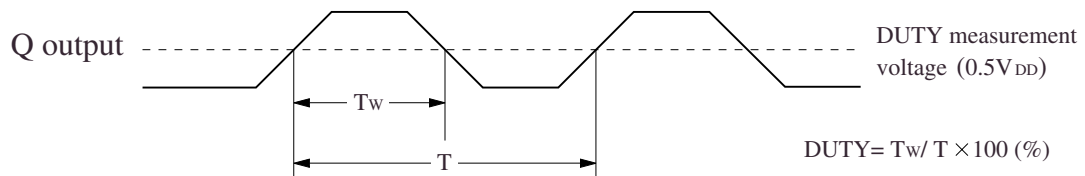
$C_L = 15\text{pF}$ :  $t_{r1}$ ,  $t_{f1}$ , Duty1,  $I_{DD1}$   
 $C_L = 50\text{pF}$ :  $t_{r2}$ ,  $t_{f2}$ , Duty2,  $I_{DD2}$

## Switching Time Measurement Waveform

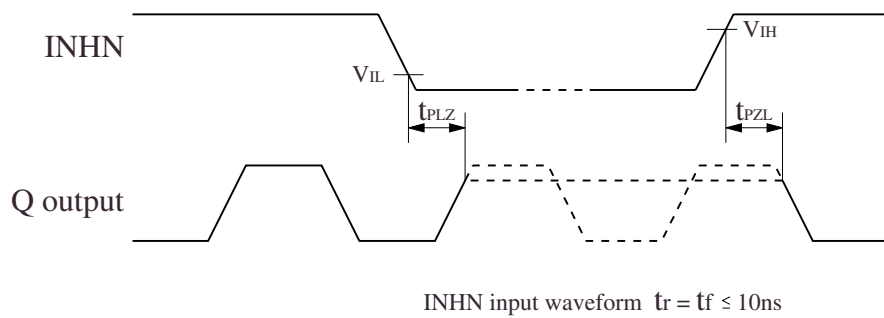
### Output duty level, $t_r$ , $t_f$



### Output duty cycle



### Output Enable/Disable Delay





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The logo for NPC (Seiko NPC Corporation) consists of the letters 'NPC' in a bold, stylized, sans-serif font. The 'N' and 'P' are connected, and the 'C' is a simple curve.

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