

## VCXO Module ICs with Built-in Varicap

#### **OVERVIEW**

The CF5073 series are VCXO ICs with built-in varicap diode. They use a recently developed negative-resistance switching oscillation circuit, at oscillation startup and during normal oscillation, for both good oscillation startup characteristics and wide pullrange. Furthermore, it employs a CMOS process varicap diode, and also features all the necessary VCXO structure circuit components on a single chip, forming a VCXO module with just the connection of an external crystal.

### **FEATURES**

- 3.0 to 3.6V supply voltage range
- 10MHz to 60MHz operating frequency (varies with version)
- Uses negative-resistance switching function
- Varicap diode built-in
- Frequency divider built-in (varies with version:  $f_O$ ,  $f_O/2$ ,  $f_O/4$ ,  $f_O/8$ ,  $f_O/16$ ,  $f_O/32$ )
- CMOS output level
- $50 \pm 10\%$  output duty
- 6mA (min) output drive capability
- 15pF output load capacitance C<sub>L</sub>
- Standby function (high impedance in standby mode)
- Chip form (CF5073××)

### **SERIES LINEUP**

Version	Typical oscillation		Output frequency					
version	frequency <sup>1</sup> [MHz]	CF5073×1	CF5073×2 <sup>2</sup>	CF5073×3 <sup>2</sup>	CF5073×4 <sup>2</sup>	CF5073×5 <sup>2</sup>	CF5073×6 <sup>2</sup>	
CF5073A×	16		f <sub>O</sub> /2	f <sub>O</sub> /4	f <sub>O</sub> /8	f <sub>O</sub> /16	£ /20	
CF5073B×	23							
CF5073C×	30	,						
CF5073D×	37	f <sub>O</sub>					f <sub>O</sub> /32	
CF5073E×	44							
CF5073F×	51							

<sup>1.</sup> The typical oscillation frequency is the oscillation frequency criteria for use when selecting the device version. Note that the oscillation characteristics and pullability vary with the crystal used and the mounting conditions. Even for the same frequency, the optimal version can vary with crystal characteristics, so careful evaluation should be exercised when selecting the device version.

#### **APPLICATIONS**

- VCXO modules
- Communications application
- Networking application
- Broadcasting application

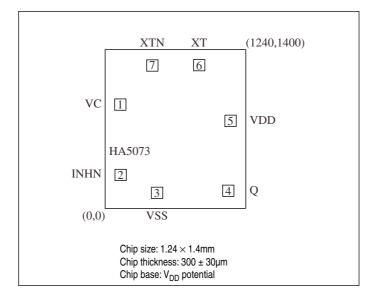
### **ORDERING INFORMATION**

Device	Package
CF5073××-1	Chip form

<sup>2.</sup> These versions are produced after receiving a purchase order. Please ask our Sales & Marketing section for further detail.

## **PAD LAYOUT**

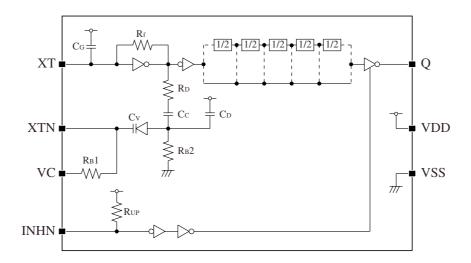
(Unit: µm)



### PAD DESCRIPTION AND DIMENSIONS

Pad No.	Name	1/0	December	Function	Pad dimensions [µm]		
Pau No.	Ivallie	1/0	Description	Function	Х	Υ	
1	VC	I	Oscillation frequency control voltage input pin	Positive polarity (frequency increases with increasing voltage)	134	915	
2	INHN	I	Output state control voltage input pin	High-impedance output when LOW, pull-up resistor built-in	137	295	
3	VSS	-	(–) supply pin		458	137	
4	Q	0	Output pin	Output frequency determined by internal circuit to one of f <sub>O</sub> , f <sub>O</sub> /2, f <sub>O</sub> /4, f <sub>O</sub> /8, f <sub>O</sub> /16, f <sub>O</sub> /32	1086	155	
5	VDD	-	(+) supply pin		1106	772	
6	XT	I	Amplifier input pin	Crystal connection pins.	829	1263	
7	XTN	0	Amplifier output pin	Crystal is connected between XT and XTN.	416	1260	

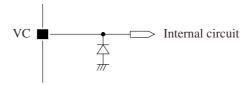
## **BLOCK DIAGRAM**



Note. ESD of XT pin is inferior to other pins.

ESD of all pins excluding XT pin is equivalent to that of our other oscillator products.

VC pin has no protection circuit at V<sub>DD</sub> side. (See figure below.)



### **ABSOLUTE MAXIMUM RATINGS**

 $V_{SS} = 0V$  unless otherwise noted.

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range	V <sub>DD</sub>		-0.5 to 7.0	V
Input voltage range	V	All input pins excluding VC pin	-0.5 to V <sub>DD</sub> + 0.5	V
	V <sub>IN</sub>	VC pin	-0.5 to V <sub>DD</sub> + 2.5 <sup>1</sup>	V
Output voltage range	V <sub>OUT</sub>		-0.5 to V <sub>DD</sub> + 0.5	V
Operating temperature range	T <sub>opr</sub>		-40 to +85	°C
Storage temperature range	T <sub>STG</sub>		-65 to +150	°C
Output current	I <sub>OUT</sub>		20	mA

<sup>1.</sup> It should not exceed + 7.0V.

## RECOMMENDED OPERATING CONDITIONS

 $V_{SS} = 0V$ , f = 10MHz to 60MHz,  $C_L \le 15pF$  unless otherwise noted.

Parameter	Symbol Conditions -	Conditions		Unit		
		Min	Тур	Max	Oilit	
Operating supply voltage	V <sub>DD</sub>		3.0	-	3.6	V
Input voltage	V <sub>IN</sub>		V <sub>SS</sub>	-	V <sub>DD</sub>	V
Operating temperature	T <sub>OPR</sub>		-40	-	+85	°C

## **ELECTRICAL CHARACTERISTICS**

## CF5073A×

Downwater	Complete	Conditions			Rating		Unit
Parameter	Symbol			Min	Тур	Max	
HIGH-level output voltage	V <sub>OH</sub>	Q: Measurement circuit 1, I <sub>OH</sub>	<sub>I</sub> = 6mA	2.5	2.75	-	٧
LOW-level output voltage	V <sub>OL</sub>	Q: Measurement circuit 1, I <sub>OL</sub>	= 6mA	-	0.2	0.4	٧
Output laakaga aurrant		Q: Measurement circuit 6,	$V_{OH} = V_{DD}$	-	-	10	μΑ
Output leakage current	I <sub>Z</sub>	INHN = LOW	V <sub>OL</sub> = V <sub>SS</sub>	-	-	10	μΑ
HIGH-level input voltage	V <sub>IH</sub>	NHN		0.7V <sub>DD</sub>	-	-	٧
LOW-level input voltage	V <sub>IL</sub>	INHN	NHN		-	0.3V <sub>DD</sub>	٧
			CF5073A1	-	8	20	mA
Current consumption		Measurement circuit 2, load circuit 1, INHN = open,	CF5073A2	-	7.5	19.5	mA
ounent consumption	I <sub>DD</sub>	C <sub>L</sub> = 15pF, f = 16MHz	CF5073A3	-	7	19.5	mA
		- ···-	CF5073A4 to 6	-	7	19	mA
INHN pull-up resistance	R <sub>UP</sub>	Measurement circuit 3	Measurement circuit 3		100	180	kΩ
	R <sub>f</sub>	Design value. A monitor pattern on a wafer is		150	300	540	kΩ
	R <sub>D</sub>	tested.		0.67	0.96	1.25	kΩ
Built-in resistance	R <sub>B1</sub>	Measurement circuit 4		100	200	360	kΩ
	R <sub>B2</sub>	Design value. A monitor patte tested.	rn on a wafer is	50	100	180	kΩ
		Design value. A monitor	V <sub>C</sub> = 0.3V	11.0	14.4	17.8	pF
	C <sub>V</sub>	pattern on a wafer is tested.	V <sub>C</sub> = 3.0V	2.4	4.0	5.6	pF
Built-in capacitance	C <sub>G</sub>		1	25.5	30	34.5	pF
	C <sub>D</sub>	Design value. A monitor pattern on a wafer is tested.		34	40	46	pF
	C <sub>C</sub>			8.5	10	11.5	pF

## CF5073B×

Davamatav	Complete	Conditions			Rating		Unit
Parameter	Symbol			Min	Тур	Max	
HIGH-level output voltage	V <sub>OH</sub>	Q: Measurement circuit 1, I <sub>OH</sub>	<sub>I</sub> = 6mA	2.5	2.75	-	٧
LOW-level output voltage	V <sub>OL</sub>	Q: Measurement circuit 1, I <sub>OL</sub>	= 6mA	-	0.2	0.4	٧
Output leakage current		Q: Measurement circuit 6,	$V_{OH} = V_{DD}$	-	-	10	μΑ
Output leakage current	I <sub>Z</sub>	INHN = LOW	V <sub>OL</sub> = V <sub>SS</sub>	-	-	10	μΑ
HIGH-level input voltage	V <sub>IH</sub>	NHN		0.7V <sub>DD</sub>	-	-	٧
LOW-level input voltage	V <sub>IL</sub>	NHN		-	-	0.3V <sub>DD</sub>	٧
			CF5073B1	-	9	22	mA
Current consumption		Measurement circuit 2, load circuit 1, INHN = open,	CF5073B2	-	8	21	mA
ounent consumption	I <sub>DD</sub>	C <sub>L</sub> = 15pF, f = 23MHz	CF5073B3	-	7.5	20.5	mA
		1 - 2011112	CF5073B4 to 6	-	7.5	20.5	mA
INHN pull-up resistance	R <sub>UP</sub>	Measurement circuit 3	Measurement circuit 3		100	180	kΩ
	R <sub>f</sub>	Design value. A monitor pattern on a wafer is		150	300	540	kΩ
	R <sub>D</sub>	tested.		0.50	0.72	0.94	kΩ
Built-in resistance	R <sub>B1</sub>	Measurement circuit 4		100	200	360	kΩ
	R <sub>B2</sub>	Design value. A monitor patte tested.	rn on a wafer is	50	100	180	kΩ
		Design value. A monitor	V <sub>C</sub> = 0.3V	11.0	14.6	18.2	pF
	C <sub>V</sub>	pattern on a wafer is tested.	V <sub>C</sub> = 3.0V	2.3	4.0	5.7	pF
Built-in capacitance	C <sub>G</sub>	Design value. A monitor pattern on a wafer is tested.		25.5	30	34.5	pF
	C <sub>D</sub>			34	40	46	pF
	C <sub>C</sub>			12.7	15	17.3	pF

## $\textbf{CF5073C}\times$

Davamatav	Complete	Conditions			Rating		Unit
Parameter	Symbol			Min	Тур	Max	
HIGH-level output voltage	V <sub>OH</sub>	Q: Measurement circuit 1, I <sub>OH</sub>	<sub>I</sub> = 6mA	2.5	2.75	-	٧
LOW-level output voltage	V <sub>OL</sub>	Q: Measurement circuit 1, I <sub>OL</sub>	= 6mA	-	0.2	0.4	٧
Output leakage current		Q: Measurement circuit 6,	$V_{OH} = V_{DD}$	-	-	10	μΑ
Output leakage current	I <sub>Z</sub>	INHN = LOW	V <sub>OL</sub> = V <sub>SS</sub>	-	-	10	μΑ
HIGH-level input voltage	V <sub>IH</sub>	NHN		0.7V <sub>DD</sub>	-	_	٧
LOW-level input voltage	V <sub>IL</sub>	INHN	NHN		-	0.3V <sub>DD</sub>	٧
			CF5073C1	-	10	24	mA
Current consumption		Measurement circuit 2, load circuit 1, INHN = open,	CF5073C2	-	9	23	mA
ounent consumption	I <sub>DD</sub>	C <sub>L</sub> = 15pF, f = 30MHz	CF5073C3	-	8.5	22.5	mA
			CF5073C4 to 6	-	8	22	mA
INHN pull-up resistance	R <sub>UP</sub>	Measurement circuit 3	Measurement circuit 3		100	180	kΩ
	R <sub>f</sub>	Design value. A monitor pattern on a wafer is		150	300	540	kΩ
	R <sub>D</sub>	tested.		0.50	0.72	0.94	kΩ
Built-in resistance	R <sub>B1</sub>	Measurement circuit 4		100	200	360	kΩ
	R <sub>B2</sub>	Design value. A monitor patte tested.	rn on a wafer is	50	100	180	kΩ
		Design value. A monitor	V <sub>C</sub> = 0.3V	11.0	14.6	18.2	pF
	C <sub>V</sub>	pattern on a wafer is tested.	V <sub>C</sub> = 3.0V	2.3	4.0	5.7	pF
Built-in capacitance	C <sub>G</sub>	Design value. A monitor pattern on a wafer is tested.		25.5	30	34.5	pF
	C <sub>D</sub>			25.5	30	34.5	pF
	C <sub>C</sub>			29.7	35	40.3	pF

## $\text{CF5073D}\times$

Davamatav	Complete	Conditions			Rating		Unit
Parameter	Symbol	Conditions	Min	Тур	Max		
HIGH-level output voltage	V <sub>OH</sub>	Q: Measurement circuit 1, I <sub>OH</sub>	<sub>I</sub> = 6mA	2.5	2.75	-	V
LOW-level output voltage	V <sub>OL</sub>	Q: Measurement circuit 1, I <sub>OL</sub>	= 6mA	-	0.2	0.4	V
Output leakage current		Q: Measurement circuit 6,	$V_{OH} = V_{DD}$	-	-	10	μΑ
Output leakage current	l <sub>Z</sub>	INHN = LOW	V <sub>OL</sub> = V <sub>SS</sub>	-	-	10	μΑ
HIGH-level input voltage	V <sub>IH</sub>	INHN		0.7V <sub>DD</sub>	-	-	V
LOW-level input voltage	V <sub>IL</sub>	INHN			-	0.3V <sub>DD</sub>	V
			CF5073D1	-	11	26	mA
Current consumption		Measurement circuit 2, load circuit 1, INHN = open,	CF5073D2	-	9.5	24.5	mA
Current consumption	I <sub>DD</sub>	C <sub>L</sub> = 15pF, f = 37MHz	CF5073D3	-	9	24	mA
		-	CF5073D4 to 6	-	8.5	23.5	mA
INHN pull-up resistance	R <sub>UP</sub>	Measurement circuit 3		50	100	180	kΩ
	R <sub>f</sub>	Design value. A monitor pattern on a wafer is		150	300	540	kΩ
	R <sub>D</sub>	tested.		0.25	0.36	0.47	kΩ
Built-in resistance	R <sub>B1</sub>	Measurement circuit 4		100	200	360	kΩ
	R <sub>B2</sub>	Design value. A monitor patte tested.	rn on a wafer is	50	100	180	kΩ
		Design value. A monitor	V <sub>C</sub> = 0.3V	11.0	14.6	18.2	pF
	C <sub>V</sub>	pattern on a wafer is tested.	V <sub>C</sub> = 3.0V	2.3	4.0	5.7	pF
Built-in capacitance	C <sub>G</sub>	Design value. A monitor pattern on a wafer is tested.		25.5	30	34.5	pF
	C <sub>D</sub>			25.5	30	34.5	pF
	C <sub>C</sub>			34	40	46	pF

## $\textbf{CF5073E}\times$

Davamatav	Complete	Conditions			Rating		Unit
Parameter	Symbol	Conditions	Min	Тур	Max		
HIGH-level output voltage	V <sub>OH</sub>	Q: Measurement circuit 1, I <sub>OH</sub>	= 6mA	2.5	2.75	-	V
LOW-level output voltage	V <sub>OL</sub>	Q: Measurement circuit 1, I <sub>OL</sub>	= 6mA	-	0.2	0.4	V
Output leakage current		Q: Measurement circuit 6,	$V_{OH} = V_{DD}$	-	-	10	μΑ
Output leakage current	l <sub>Z</sub>	INHN = LOW	V <sub>OL</sub> = V <sub>SS</sub>	-	-	10	μΑ
HIGH-level input voltage	V <sub>IH</sub>	INHN		0.7V <sub>DD</sub>	-	-	٧
LOW-level input voltage	V <sub>IL</sub>	INHN	IHN		-	0.3V <sub>DD</sub>	٧
			CF5073E1	-	12	28	mA
Current consumption		Measurement circuit 2, load circuit 1, INHN = open,	CF5073E2	-	10.5	26.5	mA
Current consumption	I <sub>DD</sub>	C <sub>L</sub> = 15pF, f = 44MHz	CF5073E3	-	9.5	25.5	mA
			CF5073E4 to 6	-	9	25	mA
INHN pull-up resistance	R <sub>UP</sub>	Measurement circuit 3		50	100	180	kΩ
	R <sub>f</sub>	Design value. A monitor pattern on a wafer is		150	300	540	kΩ
	R <sub>D</sub>	tested.		0.25	0.36	0.47	kΩ
Built-in resistance	R <sub>B1</sub>	Measurement circuit 4		100	200	360	kΩ
	R <sub>B2</sub>	Design value. A monitor patte tested.	rn on a wafer is	50	100	180	kΩ
		Design value. A monitor	V <sub>C</sub> = 0.3V	11.0	14.6	18.2	pF
	C <sub>V</sub>	pattern on a wafer is tested.	V <sub>C</sub> = 3.0V	2.3	4.0	5.7	pF
Built-in capacitance	C <sub>G</sub>	Design value. A monitor pattern on a wafer is tested.		21.2	25	28.8	pF
	C <sub>D</sub>			21.2	25	28.8	pF
	C <sub>C</sub>			42.5	50	57.5	pF

## $\textbf{CF5073F} \times$

Parameter	Compleal	Conditions			Rating		Unit
Parameter	Symbol	Conditions	Min	Тур	Max		
HIGH-level output voltage	V <sub>OH</sub>	Q: Measurement circuit 1, I <sub>OH</sub>	<sub>I</sub> = 6mA	2.5	2.75	-	٧
LOW-level output voltage	V <sub>OL</sub>	Q: Measurement circuit 1, I <sub>OL</sub>	= 6mA	-	0.2	0.4	V
Output leakage current		Q: Measurement circuit 6,	$V_{OH} = V_{DD}$	-	-	10	μΑ
Output leakage current	l <sub>Z</sub>	INHN = LOW	V <sub>OL</sub> = V <sub>SS</sub>	-	-	10	μΑ
HIGH-level input voltage	V <sub>IH</sub>	INHN		0.7V <sub>DD</sub>	-	-	٧
LOW-level input voltage	V <sub>IL</sub>	INHN	IHN		-	0.3V <sub>DD</sub>	٧
			CF5073F1	-	13	30	mA
Current consumption		Measurement circuit 2, load circuit 1, INHN = open,	CF5073F2	-	11	28	mA
Current consumption	I <sub>DD</sub>	C <sub>L</sub> = 15pF, f = 51MHz	CF5073F3	-	10	27	mA
			CF5073F4 to 6	-	9.5	26.5	mA
INHN pull-up resistance	R <sub>UP</sub>	Measurement circuit 3		50	100	180	kΩ
	R <sub>f</sub>	Design value. A monitor pattern on a wafer is		150	300	540	kΩ
	R <sub>D</sub>	tested.		0.25	0.36	0.47	kΩ
Built-in resistance	R <sub>B1</sub>	Measurement circuit 4		100	200	360	kΩ
	R <sub>B2</sub>	Design value. A monitor patte tested.	rn on a wafer is	50	100	180	kΩ
		Design value. A monitor	V <sub>C</sub> = 0.3V	9.5	12.5	15.5	pF
	C <sub>V</sub>	pattern on a wafer is tested.	V <sub>C</sub> = 3.0V	2.0	3.5	5.0	pF
Built-in capacitance	C <sub>G</sub>		•	17	20	23	pF
	C <sub>D</sub>	Design value. A monitor pattern on a wafer is tested.		17	20	23	pF
	C <sub>C</sub>			42.5	50	57.5	pF

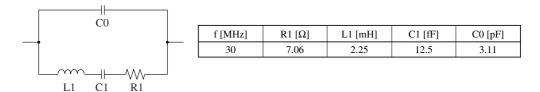
#### **SWITCHING CHARACTERISTICS**

 $V_{DD}$  = 3.0 to 3.6V,  $V_{C}$  = 1.65V,  $V_{SS}$  = 0V, Ta = -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions				Unit
raidilletei	Syllibol	Conditions		Тур	Max	Offic
Output rise time	t <sub>r1</sub>		_	2.5	6	ns
Output fall time	t <sub>f1</sub>		-	2.5	6	ns
Output duty cycle	Duty	Measurement circuit 2, load circuit 1, V <sub>DD</sub> = 3.3V, Ta = 25°C, C <sub>L</sub> = 15pF	40	50	60	%
Output disable delay time	t <sub>PLZ</sub>	Measurement circuit 5, load circuit 1,	-	-	100	ns
Output enable delay time	t <sub>PZL</sub>	$V_{DD} = 3.3V$ , Ta = 25°C, $C_L \le 15pF$	_	_	100	ns

<sup>1.</sup> The switching characteristics apply for normal output waveforms. Note that, depending on the matching of the CF5073 series version and crystal, normal waveform output may not be continuous.

# Current consumption and Output waveform with NPC's standard crystal



### **FUNCTIONAL DESCRIPTION**

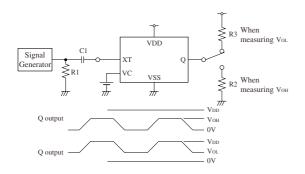
### **Standby Function**

When INHN goes LOW, the Q output pin becomes high impedance.

INHN	Q	Oscillator
HIGH (or open)	Any $f_0$ , $f_0/2$ , $f_0/4$ , $f_0/8$ , $f_0/16$ , or $f_0/32$	Operating
LOW	High impedance	Operating

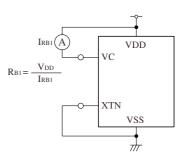
### **MEASUREMENT CIRCUITS**

### **Measurement Circuit 1**

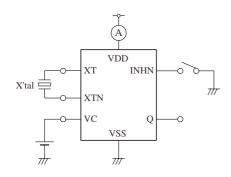


XT input signal: 2.5Vp-p, 10MHz, sine wave C1 = 0.001 $\mu$ F, R1 = 50 $\Omega$ , R2 = 417 $\Omega$ , R3 = 434 $\Omega$ , V<sub>C</sub> = 1.65V

### **Measurement Circuit 4**

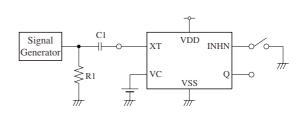


### **Measurement Circuit 2**



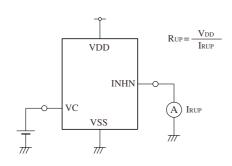
 $V_C$  = 1.65V, INHN = open, crystal oscillation

### **Measurement Circuit 5**



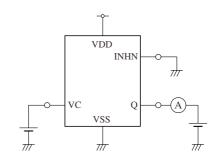
XT input signal: 2.5Vp-p, 10MHz, sine wave C1 = 0.001  $\mu F,$  R1 =  $50\Omega,$   $V_C$  = 1.65V

### **Measurement Circuit 3**



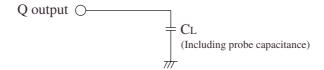
 $V_{C} = 1.65V$ 

### **Measurement Circuit 6**



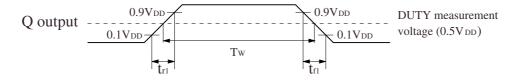
$$V_{C} = 1.65V$$

### **Load Circuit 1**

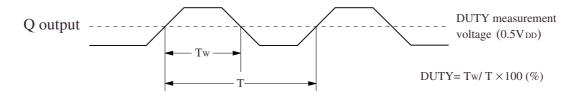


## **Switching Time Measurement Waveform**

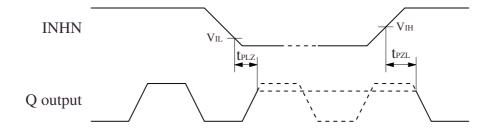
## Output duty level, t<sub>r</sub>, t<sub>f</sub>



### **Output duty cycle**



## **Output Enable/Disable Delay Times**



INHN input waveform  $tr = tf \le 10$ ns

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