

OVERVIEW

The SM5010 series are crystal oscillator module ICs. They incorporate oscillator and output buffer circuits, employing built-in oscillator capacitors and feedback resistors with excellent frequency response, eliminating the need for external components to form a stable crystal oscillator. There are 7 oscillator configurations available for design and application optimization.

FEATURES

- 7 types of oscillation circuit structure
 - For fundamental oscillator**
 - 5010A××: Simple structure with low frequency variation
 - 5010B××: Low crystal current type with R_D built-in oscillation circuit
 - 5010CL×: Oscillation stop function built-in
 - 5010DN×: External capacitors, C_G and C_D required
 - 5010EA×: Low current consumption type
 - For 3rd overtone oscillator**
 - 5010F××: Suitable for round blank
 - 5010H××: External resistor, R_f required
- 2.7 to 5.5V operating supply voltage
- Capacitors C_G , C_D built-in
- Inverter amplifier feedback resistor built-in
- Output duty level
 - TTL level: AK×, BK×, HK×
 - CMOS level: AN×, AH×, BN×, BH×, CL×, DN×, EA×, FN×, FH×, HN×
- Oscillator frequency output (f_O , $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$ determined by internal connection)
- Standby function
- Pull-up resistor built-in
- 8-pin SOP (SM5010×××S)
- Chip form (CF5010×××)

SERIES CONFIGURATION

For Fundamental Oscillator

Version ¹	Operating supply voltage range [V]	Built-in capacitance		R_D [Ω]	Output current ($V_{DD} = 5V$) [mA]	Output duty level	Output frequency	INHN input level ($V_{DD} = 5V$)	Standby mode	
		C_G [pF]	C_D [pF]						Oscillator stop function	Output state
CF5010AN1	2.7 to 5.5	29	29	–	16	CMOS	f_O	TTL	No	High impedance
CF5010AN2						CMOS/TTL	$f_O/2$			
CF5010AN3							$f_O/4$			
CF5010AN4							$f_O/8$			
CF5010AK1	4.5 to 5.5	29	29	–	16	TTL	f_O	TTL	No	High impedance
CF5010AH1	2.7 to 5.5	29	29	–	4	CMOS	f_O	TTL	No	High impedance
CF5010AH2							$f_O/2$			
CF5010AH3							$f_O/4$			
CF5010AH4							$f_O/8$			
CF5010BN1	2.7 to 5.5	22	22	820	16	CMOS	f_O	TTL	No	High impedance
CF5010BN2						CMOS/TTL	$f_O/2$			
CF5010BN3							$f_O/4$			
CF5010BN4							$f_O/8$			
CF5010BN5							$f_O/16$			
CF5010BK1	4.5 to 5.5	22	22	820	16	TTL	f_O	TTL	No	High impedance
CF5010BH1	2.7 to 5.5	22	22	820	4	CMOS	f_O	TTL	No	High impedance
CF5010BH2							$f_O/2$			
CF5010BH3							$f_O/4$			
CF5010BH4							$f_O/8$			
CF5010CL1	2.7 to 5.5	18	18	–	16	CMOS	f_O	CMOS	Yes	High impedance
CF5010CL2							$f_O/2$			
CF5010CL3							$f_O/4$			
CF5010CL4							$f_O/8$			
CF5010CL5							$f_O/16$			
CF5010DN1	2.7 to 5.5	–	–	820	16	CMOS	f_O	TTL	No	High impedance
CF5010EA1	2.7 to 5.5	10	15	820	4	CMOS	f_O	TTL	Yes	LOW
CF5010EA2							$f_O/2$			

1. Package devices have designation SM5010×××S.

SERIES CONFIGURATION

For 3rd Overtone Oscillator

Version	Operating supply voltage range [V]	gm ratio	Built-in capacitance		R_f [k Ω]	Output current ($V_{DD} = 5V$) [mA]	Output duty level
			C_G [pF]	C_D [pF]			
CF5010FNA	2.7 to 5.5	1.00	13	15	4.2	16	CMOS
CF5010FNC			11	17	3.1		
CF5010FND			13	17	2.2		
CF5010FNE	4.5 to 5.5		8	15	2.2		
CF5010FHA	4.5 to 5.5	1.00	13	15	4.2	4	CMOS
CF5010FHC			11	17	3.1		
CF5010FHD			13	17	2.2		
CF5010FHE			8	15	2.2		
CF5010HN1	4.5 to 5.5	1.17	13	17	200	16	CMOS
CF5010HK1	4.5 to 5.5	1.17	13	17	200	16	TTL

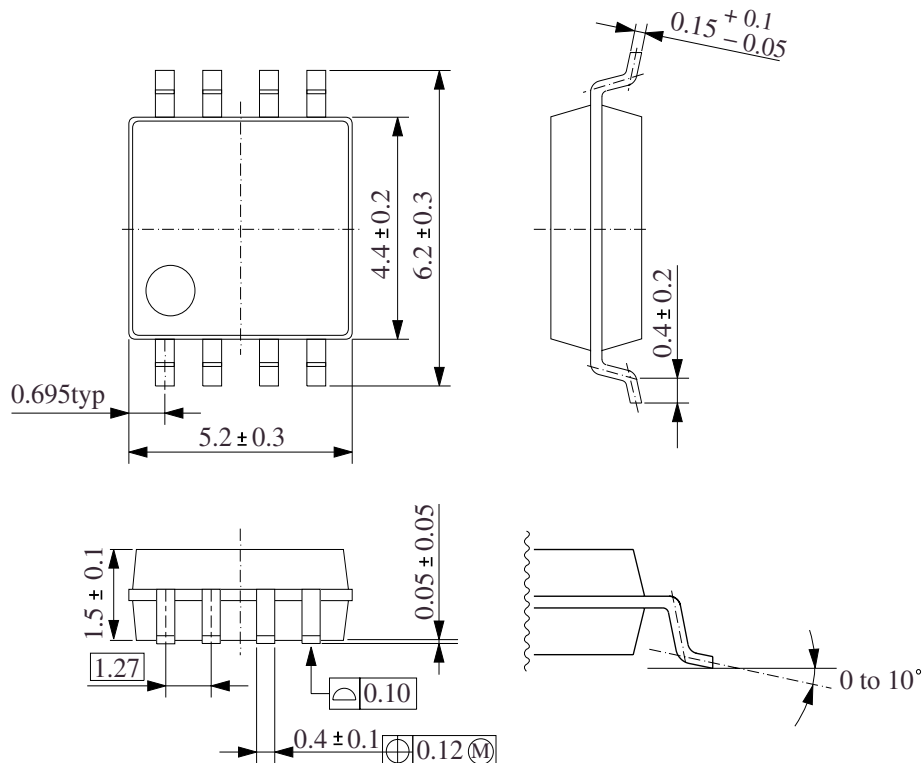
ORDERING INFORMATION

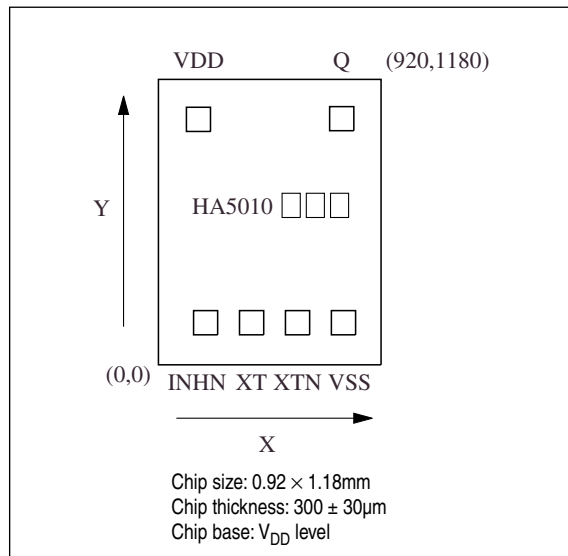
Device	Package
SM5010xxxS	8-pin SOP
CF5010xxx-1	Chip form

PACKAGE DIMENSIONS

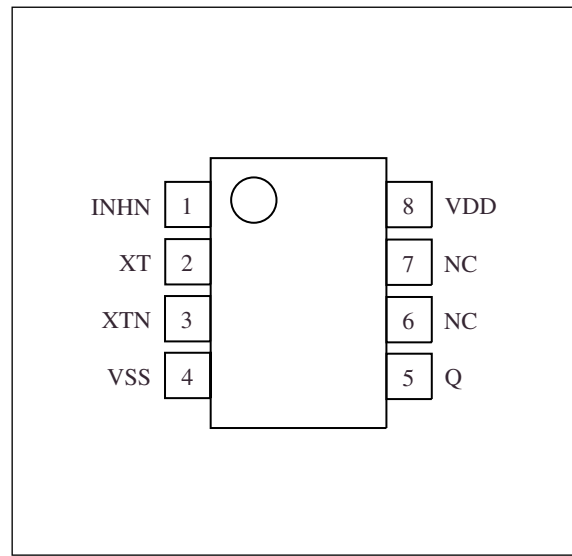
(Unit: mm)

- 8-pin SOP



PAD LAYOUT(Unit: μm)**PINOUT**

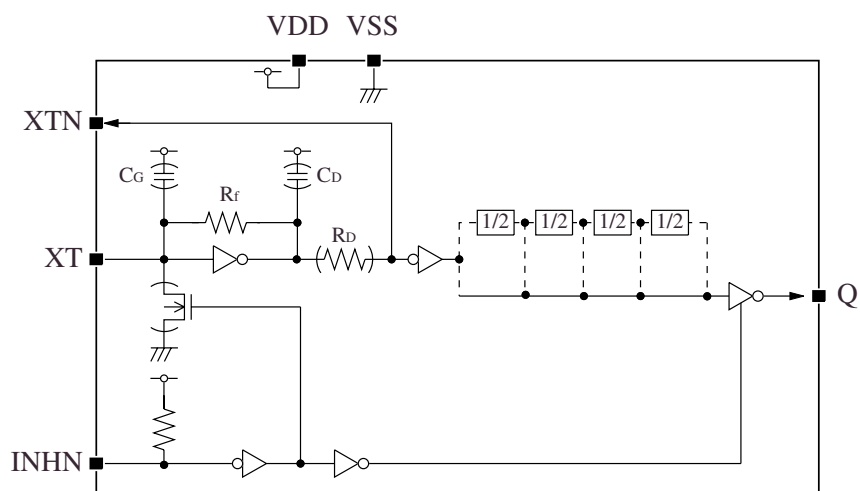
(Top view)

**PIN DESCRIPTION and PAD DIMENSIONS**

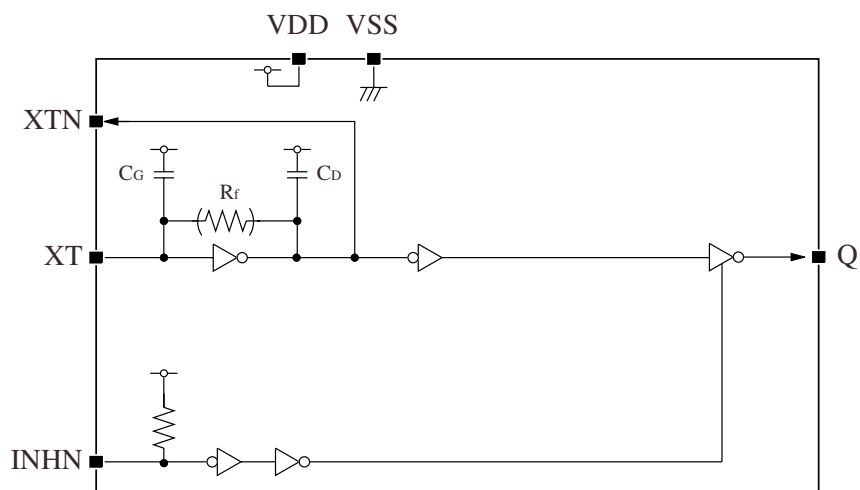
Number	Name	I/O	Description	Pad dimensions [μm]	
				X	Y
1	INH N	I	Output state control input. Standby mode when LOW, pull-up resistor built in. In the case of the 5010CL $\times$, the oscillator stops and Power-saving pull-up resistor is built-in to reduce current consumption at standby mode.	195	174.4
2	XT	I	Amplifier input.	385	174.4
3	XTN	O	Amplifier output.	575	174.4
4	VSS	–	Ground	765	174.4
5	Q	O	Output. Output frequency (f_O , $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$) determined by internal connection	757.6	1017.6
6	NC	–	No connection	–	–
7	NC	–	No connection	–	–
8	VDD	–	Supply voltage	165.4	1014.6

BLOCK DIAGRAM**For Fundamental Oscillator**

- 5010Axx, Bxx, CLx, DNx, EAx series

**For 3rd Overtone Oscillator**

- 5010Fxx, Hxx series



FUNCTIONAL DESCRIPTION

Standby Function

5010AH×, AK×, AN×, BH×, BK×, BN×, DN×, FN×, FH×, HN×, HK× series

When INHN goes LOW, the output on Q becomes high impedance, but internally the oscillator does not stop.

5010CL× series

When INHN goes LOW, the oscillator stops and the oscillator output on Q becomes high impedance.

5010EA× series

When INHN goes LOW, the oscillator stops and the oscillator output on Q becomes LOW.

Version	INHN	Q	Oscillator
AH×, AK×, AN×, BH×, BK×, BN×, DN×, FH×, FN×, HN×, HK× series	HIGH (or open)	Any f_O , $f_O/2$, $f_O/4$, $f_O/8$ or $f_O/16$ output frequency	Normal operation
	LOW	High impedance	Normal operation
CL× series	HIGH (or open)	Any f_O , $f_O/2$, $f_O/4$, $f_O/8$ or $f_O/16$ output frequency	Normal operation
	LOW	High impedance	Stopped
EA× series	HIGH (or open)	Either f_O or $f_O/2$ output frequency	Normal operation
	LOW	LOW	Stopped

Power-saving Pull-up Resistor (CL series only)

The INHN pull-up resistance changes in response to the input level (HIGH or LOW). When INHN goes LOW (standby state), the pull-up resistance becomes large to reduce the current consumption during standby.

SPECIFICATIONS

Absolute Maximum Ratings

 $V_{SS} = 0V$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		-0.5 to +7.0	V
Input voltage range	V_{IN}		-0.5 to $V_{DD} + 0.5$	V
Output voltage range	V_{OUT}		-0.5 to $V_{DD} + 0.5$	V
Operating temperature range	T_{opr}		-40 to +85	°C
Storage temperature range	T_{stg}	Chip form	-65 to +150	°C
		8-pin SOP	-55 to +125	
Output current	I_{OUT}	AH×, BH×, FH×, EA×	10	mA
		AN×, AK×, BN×, BK×, CL×, DN×, FN×, HN×, HK×	25	
Power dissipation	P_D	8-pin SOP	500	mW

Recommended Operating Conditions

3V operation

 $V_{SS} = 0V$

Parameter	Symbol	Version	Condition	Rating	Unit
Operating supply voltage	V _{DD}	All version		2.7 to 3.6	V
Input voltage	V _{IN}	All version		V _{SS} to V _{DD}	V
Operating temperature	T _{OPR}	5010AN×		−10 to +70	°C
		5010AH×			
		5010BN×			
		5010BH×			
		5010CL×		−20 to +80	
		5010DN1		−10 to +70	
		5010EA×			
		5010FN×			
Operating frequency	f	5010AN×	C _L ≤ 15pF	2 to 30	MHz
		5010AH×		2 to 16	
		5010BN×		2 to 30	
		5010BH×		2 to 16	
		5010CL×		2 to 30	
		5010DN1			
		5010EA×			
		5010FN×		22 to 40	

5V operation $V_{SS} = 0V$

Parameter	Symbol	Version	Condition	Rating	Unit
Operating supply voltage	V _{DD}	All version		4.5 to 5.5	V
Input voltage	V _{IN}	All version		V _{SS} to V _{DD}	V
Operating temperature	T _{OPR}	5010AN×		−40 to +85	°C
		5010AK×			
		5010AH×			
		5010BN×			
		5010BK×			
		5010BH×			
		5010CL×			
		5010DN1			
		5010EA×	C _L ≤ 15pF, f = 2 to 30MHz	−10 to +70	
			C _L ≤ 15pF, f = 2 to 40MHz		
		5010FN×	C _L ≤ 50pF, 30MHz ≤ f ≤ 50MHz	−20 to +80	
			C _L ≤ 15pF, 50MHz ≤ f ≤ 70MHz	−15 to +75	
		5010FH×	C _L ≤ 15pF, 30MHz ≤ f ≤ 50MHz	−20 to +80	
			C _L ≤ 15pF, 50MHz ≤ f ≤ 60MHz	−15 to +75	
		5010HN1		−40 to +85	
		5010HK1			
Operating frequency	f	5010AN×	C _L ≤ 50pF	2 to 30	MHz
		5010AK×	C _L ≤ 15pF		
		5010AH×			
		5010BN×	C _L ≤ 50pF		
		5010BK×	C _L ≤ 15pF		
		5010BH×			
		5010CL×	C _L ≤ 50pF		
		5010DN1			
		5010EA×	C _L ≤ 15pF, Ta = − 40 to + 85°C	2 to 40	
		5010FN×	C _L ≤ 50pF, Ta = − 20 to + 80°C	30 to 50	
			C _L ≤ 15pF, Ta = − 15 to + 75°C	50 to 70	
		5010FH×	C _L ≤ 15pF, Ta = − 20 to + 80°C	30 to 50	
			C _L ≤ 15pF, Ta = − 15 to + 75°C	50 to 60	
		5010HN1	C _L ≤ 50pF	22 to 50	
		5010HK1	C _L ≤ 15pF		

Electrical Characteristics

5010AN×, BN×, DN× series

3V operation: $V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -10$ to $+70^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 2.7V, I _{OH} = 8mA		2.1	2.4	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 2.7V, I _{OL} = 8mA		–	0.3	0.4	V
HIGH-level input voltage	V _{IH}	INH		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH		–	–	0.5	V
Output leakage current	I _Z	Q: Measurement cct 2, INH = LOW, V _{DD} = 3.6V	V _{OH} = V _{DD}	–	–	10	μA
			V _{OL} = V _{SS}	–	–	10	
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INH = open, C _L = 15pF, f = 30MHz	5010×N1	–	5	10	mA
			5010×N2	–	3.5	7	
			5010×N3	–	2.5	5	
			5010×N4	–	2	4	
			5010×N5	–	2	4	
INH pull-up resistance	R _{UP2}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value	5010B××	690	820	940	Ω
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.	5010A××	26	29	32	pF
			5010B××	20	22	24	
	C _D		5010A××	26	29	32	
			5010B××	20	22	24	

5010AN×, AK×, BN×, BK×, DN× series

5V operation: $V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 4.5V, I _{OH} = 16mA		3.9	4.2	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 4.5V, I _{OL} = 16mA		–	0.3	0.4	V
HIGH-level input voltage	V _{IH}	INH		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH		–	–	0.8	V
Output leakage current	I _Z	Q: Measurement cct 2, INH = LOW, V _{DD} = 5.5V	V _{OH} = V _{DD}	–	–	10	μA
			V _{OL} = V _{SS}	–	–	10	
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INH = open, C _L = 50pF, f = 30MHz	5010×N1	–	15	30	mA
			5010×N2	–	9	18	
			5010×N3	–	6	12	
			5010×N4	–	5	10	
			5010×N5	–	5	10	
		Measurement cct 3, load cct 2, INH = open, C _L = 15pF, f = 30MHz	5010×K1	–	10	20	
INH pull-up resistance	R _{UP2}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value	5010B××	690	820	940	Ω
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.	5010A××	26	29	32	pF
			5010B××	20	22	24	
	C _D		5010A××	26	29	32	
			5010B××	20	22	24	

SM5010 series

5010AH×, BH× series

3V operation: $V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -10$ to $+70^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 2.7V, I _{OH} = 2mA		2.1	2.4	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 2.7V, I _{OL} = 2mA		–	0.3	0.5	V
HIGH-level input voltage	V _{IH}	INH N		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH N		–	–	0.5	V
Output leakage current	I _Z	Q: Measurement cct 2, INHN = LOW, V _{DD} = 3.6V	V _{OH} = V _{DD}	–	–	10	μA
			V _{OL} = V _{SS}	–	–	10	
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INHN = open, C _L = 15pF, f = 16MHz	5010×H1	–	3	6	mA
			5010×H2	–	2	4	
			5010×H3	–	1.5	3	
			5010×H4	–	1.5	2.5	
INH N pull-up resistance	R _{UP2}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value	5010B××	690	820	940	Ω
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.	5010A××	26	29	32	pF
			5010B××	20	22	24	
	C _D		5010A××	26	29	32	
			5010B××	20	22	24	

5V operation: $V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 4.5V, I _{OH} = 4mA		3.9	4.2	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 4.5V, I _{OL} = 4mA		–	0.3	0.5	V
HIGH-level input voltage	V _{IH}	INH N		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH N		–	–	0.8	V
Output leakage current	I _Z	Q: Measurement cct 2, INHN = LOW, V _{DD} = 5.5V	V _{OH} = V _{DD}	–	–	10	μA
			V _{OL} = V _{SS}	–	–	10	
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INHN = open, C _L = 15pF, f = 30MHz	5010×H1	–	9	18	mA
			5010×H2	–	6	12	
			5010×H3	–	5	10	
			5010×H4	–	4	8	
INH N pull-up resistance	R _{UP2}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value	5010B××	690	820	940	Ω
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.	5010A××	26	29	32	pF
			5010B××	20	22	24	
	C _D		5010A××	26	29	32	
			5010B××	20	22	24	

SM5010 series

5010CL× series

3V operation: $V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+80^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, $V_{DD} = 2.7V$, $I_{OH} = 8mA$	2.2	2.4	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, $V_{DD} = 2.7V$, $I_{OL} = 8mA$	–	0.3	0.4	V
HIGH-level input voltage	V_{IH}	INH N	$0.7V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	INH N	–	–	$0.3V_{DD}$	V
Output leakage current	I_Z	Q: Measurement cct 2, INHN = LOW, $V_{DD} = 3.6V$	$V_{OH} = V_{DD}$	–	–	10
			$V_{OL} = V_{SS}$	–	–	10
Current consumption	I_{DD}	Measurement cct 3, load cct 1, INHN = open, $C_L = 15pF$, $f = 30MHz$	5010CL1	–	5	10
			5010CL2	–	3.5	7
			5010CL3	–	2.5	5
			5010CL4	–	2	4
			5010CL5	–	2	4
Standby current	I_{ST}	Measurement cct 6, INHN = LOW	–	–	5	μA
INH N pull-up resistance	R_{UP1}	Measurement cct 4	2	4	15	$M\Omega$
	R_{UP2}		40	100	250	$k\Omega$
Feedback resistance	R_f	Measurement cct 5	80	200	500	$k\Omega$
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.	16	18	20	pF
	C_D		16	18	20	

5V operation: $V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, $V_{DD} = 4.5V$, $I_{OH} = 16mA$	4.0	4.2	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, $V_{DD} = 4.5V$, $I_{OL} = 16mA$	–	0.3	0.4	V
HIGH-level input voltage	V_{IH}	INH N	$0.7V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	INH N	–	–	$0.3V_{DD}$	V
Output leakage current	I_Z	Q: Measurement cct 2, INHN = LOW, $V_{DD} = 5.5V$	$V_{OH} = V_{DD}$	–	–	10
			$V_{OL} = V_{SS}$	–	–	10
Current consumption	I_{DD}	Measurement cct 3, load cct 1, INHN = open, $C_L = 50pF$, $f = 30MHz$	5010CL1	–	15	30
			5010CL2	–	9	18
			5010CL3	–	6	12
			5010CL4	–	5	10
			5010CL5	–	5	10
Standby current	I_{ST}	Measurement cct 6, INHN = LOW	–	–	10	μA
INH N pull-up resistance	R_{UP1}	Measurement cct 4	1	2	8	$M\Omega$
	R_{UP2}		40	100	250	$k\Omega$
Feedback resistance	R_f	Measurement cct 5	80	200	500	$k\Omega$
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.	16	18	20	pF
	C_D		16	18	20	

5010EA× series

3V operation: $V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -10$ to $+70^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 2.7V, I _{OH} = 2mA		2.1	2.4	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 2.7V, I _{OL} = 2mA		–	0.3	0.5	V
HIGH-level input voltage	V _{IH}	INH N		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH N		–	–	0.5	V
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INH N = open, C _L = 15pF, f = 30MHz	5010EA1	–	4	8	mA
			5010EA2	–	2.5	5	
INH N pull-up resistance	R _{UP2}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value		690	820	940	Ω
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.		9	10	11	pF
	C _D			13	15	17	

5V operation: $V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 4.5V, I _{OH} = 3.2mA		3.9	4.2	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 4.5V, I _{OL} = 3.2mA		–	0.3	0.4	V
HIGH-level input voltage	V _{IH}	INH N		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH N		–	–	0.8	V
Current consumption	I _{DD1}	Measurement cct 3, load cct 1, INHN = open, C _L = 15pF, f = 30MHz	5010EA1	–	6	12	mA
			5010EA2	–	5	10	
	I _{DD2}	Measurement cct 3, load cct 1, INHN = open, C _L = 15pF, f = 40MHz	5010EA1	–	9	18	
			5010EA2	–	6	12	
INH N pull-up resistance	R _{UP2}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5		80	200	500	kΩ
Oscillator amplifier output resistance	R _D	Design value		690	820	940	Ω
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.		9	10	11	pF
	C _D			13	15	17	

SM5010 series

5010FN× series

3V operation: $V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -10$ to $+70^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 2.7V, I _{OH} = 8mA		2.2	2.4	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 2.7V, I _{OL} = 8mA		–	0.3	0.4	V
HIGH-level input voltage	V _{IH}	INH N		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH N		–	–	0.5	V
Output leakage current	I _Z	Q: Measurement cct 2, INHN = LOW, V _{DD} = 3.6V	V _{OH} = V _{DD}	–	–	10	μA
			V _{OL} = V _{SS}	–	–	10	
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INHN = open, C _L = 15pF	5010FNA, FNC f = 30MHz	–	8	16	mA
			5010FND f = 40MHz	–	10	20	
INH N pull-up resistance	R _{UP}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5	5010FNA	3.57	4.2	4.83	kΩ
			5010FNC	2.63	3.1	3.57	
			5010FND	1.87	2.2	2.53	
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.	5010FNA	11.7	13	14.3	pF
			5010FNC	9.9	11	12.1	
			5010FND	11.7	13	14.3	
	C _D		5010FNA	13.5	15	16.5	
			5010FNC	15.3	17	18.7	
			5010FND	15.3	17	18.7	

SM5010 series

5V operation: $V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$

$30 \leq f \leq 50MHz$: $T_a = -20$ to $+80^\circ C$, $50 < f \leq 70MHz$: $T_a = -15$ to $+75^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 4.5V, I _{OH} = 16mA		3.9	4.2	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 4.5V, I _{OL} = 16mA		–	0.3	0.4	V
HIGH-level input voltage	V _{IH}	INH N		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH N		–	–	0.8	V
Output leakage current	I _Z	Q: Measurement cct 2, INHN = LOW, V _{DD} = 5.5V	V _{OH} = V _{DD}	–	–	10	μA
			V _{OL} = V _{SS}	–	–	10	
Current consumption	I _{DD1}	Measurement cct 3, load cct 1, INHN = open, C _L = 15pF	5010FNE f = 70MHz	–	25	50	mA
	I _{DD2}	Measurement cct 3, load cct 1, INHN = open, C _L = 50pF	5010FNA, FNC f = 40MHz	–	23	45	
			5010FND f = 50MHz	–	25	50	
INH N pull-up resistance	R _{UP}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5	5010FNA	3.57	4.2	4.83	kΩ
			5010FNC	2.63	3.1	3.57	
			5010FND	1.87	2.2	2.53	
			5010FNE	1.87	2.2	2.53	
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.	5010FNA	11.7	13	14.3	pF
			5010FNC	9.9	11	12.1	
			5010FND	11.7	13	14.3	
			5010FNE	7.2	8	8.8	
	C _D		5010FNA	13.5	15	16.5	
			5010FNC	15.3	17	18.7	
			5010FND	15.3	17	18.7	
			5010FNE	13.5	15	16.5	

SM5010 series

5010FH× series

5V operation: $V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$

$30 \leq f \leq 50MHz$: $T_a = -20$ to $+80^\circ C$, $50 < f \leq 60MHz$: $T_a = -15$ to $+75^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V _{OH}	Q: Measurement cct 1, V _{DD} = 4.5V, I _{OH} = 4mA		3.9	4.2	–	V
LOW-level output voltage	V _{OL}	Q: Measurement cct 2, V _{DD} = 4.5V, I _{OL} = 4mA		–	0.3	0.5	V
HIGH-level input voltage	V _{IH}	INH-N		2.0	–	–	V
LOW-level input voltage	V _{IL}	INH-N		–	–	0.8	V
Output leakage current	I _Z	Q: Measurement cct 2, INH-N = LOW, V _{DD} = 5.5V	V _{OH} = V _{DD}	–	–	10	μA
			V _{OL} = V _{SS}	–	–	10	
Current consumption	I _{DD}	Measurement cct 3, load cct 1, INH-N = open, C _L = 15pF	5010FHA, FHC f = 40MHz	–	13	26	mA
			5010FHD f = 50MHz	–	15	30	
			5010FHE f = 60MHz	–	17	34	
INH-N pull-up resistance	R _{UP}	Measurement cct 4		40	100	250	kΩ
Feedback resistance	R _f	Measurement cct 5	5010FHA	3.57	4.2	4.83	kΩ
			5010FHC	2.63	3.1	3.57	
			5010FHD	1.87	2.2	2.53	
			5010FHE	1.87	2.2	2.53	
Built-in capacitance	C _G	Design value. A monitor pattern on a wafer is tested.	5010FHA	11.7	13	14.3	pF
			5010FHC	9.9	11	12.1	
			5010FHD	11.7	13	14.3	
			5010FHE	7.2	8	8.8	
	C _D		5010FHA	13.5	15	16.5	
			5010FHC	15.3	17	18.7	
			5010FHD	15.3	17	18.7	
			5010FHE	13.5	15	16.5	

5010HN×, HK× series

5V operation: $V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, $V_{DD} = 4.5V$, $I_{OH} = 16mA$		3.9	4.2	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, $V_{DD} = 4.5V$, $I_{OL} = 16mA$		–	0.3	0.4	V
HIGH-level input voltage	V_{IH}	INH-N		2.0	–	–	V
LOW-level input voltage	V_{IL}	INH-N		–	–	0.8	V
Output leakage current	I_Z	Q: Measurement cct 2, INH-N = LOW, $V_{DD} = 5.5V$	$V_{OH} = V_{DD}$	–	–	10	μA
			$V_{OL} = V_{SS}$	–	–	10	
Current consumption	I_{DD1}	Measurement cct 3, load cct 2, INH-N = open, $C_L = 15pF$, $f = 50MHz$	5010HK1	–	20	40	mA
	I_{DD2}	Measurement cct 3, load cct 1, INH-N = open, $C_L = 50pF$, $f = 50MHz$	5010HN1	–	25	50	
INH-N pull-up resistance	R_{UP}	Measurement cct 4		40	100	250	$k\Omega$
Feedback resistance	R_f	Measurement cct 5		80	200	500	$k\Omega$
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		11.7	13	14.3	pF
	C_D			15.3	17	18.7	

Switching Characteristics

5010AN×, BN×, DN× series

3V operation/Duty level: CMOS

$V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -10$ to $+70^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $C_L = 15pF$, $0.1V_{DD}$ to $0.9V_{DD}$	–	3.0	6.0	ns
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $C_L = 15pF$, $0.9V_{DD}$ to $0.1V_{DD}$	–	3.0	6.0	ns
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 3.0V$, $T_a = 25^\circ C$, $C_L = 15pF$, $f = 30MHz$	40	–	60	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 3.0V$, $T_a = 25^\circ C$, $C_L = 15pF$	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

5010AN×, AK×, BN×, BK×, DN× series

5V operation/Duty level: CMOS (5010AN×, BN×, DN1)

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15pF$	–	2.0	4.0	ns
	t_{r2}		$C_L = 50pF$	–	4.0	8.0	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15pF$	–	2.0	4.0	ns
	t_{f2}		$C_L = 50pF$	–	4.0	8.0	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 50pF$, $f = 30MHz$		45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

5V operation/Duty level: TTL (5010×K1, AN2, AN3, AN4, BN2, BN3, BN4, BN5)

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r3}	Measurement cct 6, load cct 2, $C_L = 15pF$, $0.4V$ to $2.4V$	–	1.5	3.0	ns
Output fall time	t_{f3}	Measurement cct 6, load cct 2, $C_L = 15pF$, $2.4V$ to $0.4V$	–	1.5	3.0	ns
Output duty cycle ¹	Duty	Measurement cct 6, load cct 2, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$, $f = 30MHz$	45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 2, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

5010AH×, BH× series**3V operation/Duty level: CMOS**

$V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -10$ to $+70^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $C_L = 15pF$, $0.1V_{DD}$ to $0.9V_{DD}$	–	8	16	ns
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $C_L = 15pF$, $0.9V_{DD}$ to $0.1V_{DD}$	–	8	16	ns
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 3.0V$, $T_a = 25^\circ C$, $C_L = 15pF$, $f = 16MHz$	40	–	60	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 3.0V$, $T_a = 25^\circ C$, $C_L = 15pF$	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

5V operation/Duty level: CMOS

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15pF$	–	5	10	ns
	t_{r2}		$C_L = 50pF$	–	13	26	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15pF$	–	5	10	ns
	t_{f2}		$C_L = 50pF$	–	13	26	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$, $f = 30MHz$		45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

5010CL× series**3V operation/Duty level: CMOS**

$V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+80^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t _{r1}	Measurement cct 6, load cct 1, 0.1V _{DD} to 0.9V _{DD}	C _L = 15pF	–	2.0	4.0	ns
	t _{r4}		C _L = 30pF	–	3.0	6.0	
Output fall time	t _{f1}	Measurement cct 6, load cct 1, 0.9V _{DD} to 0.1V _{DD}	C _L = 15pF	–	2.0	4.0	ns
	t _{f4}		C _L = 30pF	–	3.0	6.0	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, V _{DD} = 3.0V, Ta = 25°C, C _L = 15pF, f = 30MHz		45	–	55	%
Output disable delay time ²	t _{PLZ}	Measurement cct 7, load cct 1, V _{DD} = 3.0V, Ta = 25°C, C _L = 15pF		–	–	100	ns
Output enable delay time ²	t _{PZL}			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

5V operation/Duty level: CMOS

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t _{r1}	Measurement cct 6, load cct 1, 0.1V _{DD} to 0.9V _{DD}	C _L = 15pF	–	1.5	3.0	ns
	t _{r2}		C _L = 50pF	–	4.0	8.0	
Output fall time	t _{f1}	Measurement cct 6, load cct 1, 0.9V _{DD} to 0.1V _{DD}	C _L = 15pF	–	1.5	3.0	ns
	t _{f2}		C _L = 50pF	–	4.0	8.0	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, V _{DD} = 5.0V, Ta = 25°C, C _L = 50pF, f = 30MHz		40	–	60	%
Output disable delay time ²	t _{PLZ}	Measurement cct 7, load cct 1, V _{DD} = 5.0V, Ta = 25°C, C _L = 15pF		–	–	100	ns
Output enable delay time ²	t _{PZL}			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

5010EA× series**3V operation/Duty level: CMOS**

$V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -10$ to $+70^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $C_L = 15pF$, $0.1V_{DD}$ to $0.9V_{DD}$	–	8	16	ns
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $C_L = 15pF$, $0.9V_{DD}$ to $0.1V_{DD}$	–	8	16	ns
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 3.0V$, $T_a = 25^\circ C$, $C_L = 15pF$, $f = 30MHz$	40	–	60	%
Output disable delay time ²	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 3.0V$, $T_a = 25^\circ C$, $C_L = 15pF$	–	–	100	ns
Output enable delay time ²	t_{PZL}		–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

5V operation/Duty level: CMOS

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15pF$	–	5	10	ns
	t_{r2}		$C_L = 50pF$	–	13	26	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15pF$	–	5	10	ns
	t_{f2}		$C_L = 50pF$	–	13	26	
Output duty cycle ¹	Duty1	Measurement cct 6, load cct 1, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$	$f = 30MHz$	45	–	55	%
	Duty2		$f = 40MHz$	40	–	60	
Output disable delay time ²	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$		–	–	100	ns
Output enable delay time ²	t_{PZL}			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

5010FN× series**3V operation/Duty level: CMOS**

$V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -10$ to $+70^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $C_L = 15pF$, $0.1V_{DD}$ to $0.9V_{DD}$	–	3.0	6.0	ns
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $C_L = 15pF$, $0.9V_{DD}$ to $0.1V_{DD}$	–	3.0	6.0	ns
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 3.0V$, $T_a = 25^\circ C$, $C_L = 15pF$, $f = 40MHz$	40	–	60	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 3.0V$, $T_a = 25^\circ C$, $C_L = 15pF$	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

5V operation/Duty level: CMOS

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$

$30 \leq f \leq 50MHz$: $T_a = -20$ to $+80^\circ C$, $50 < f \leq 70MHz$: $T_a = -15$ to $+75^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15pF$	–	1.5	3.0	ns
	t_{r2}		$C_L = 50pF$	–	3.0	6.0	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15pF$	–	1.5	3.0	ns
	t_{f2}		$C_L = 50pF$	–	3.0	6.0	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 5.0V$, $T_a = 25^\circ C$	$C_L = 50pF$ $f = 50MHz$	45	–	55	%
			$C_L = 15pF$ $f = 70MHz$	40	–	60	
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

5010FH× series**5V operation/Duty level: CMOS**
 $V_{DD} = 4.5 \text{ to } 5.5\text{V}$, $V_{SS} = 0\text{V}$
 $30 \leq f \leq 50\text{MHz}$: $T_a = -20 \text{ to } +80^\circ\text{C}$, $50 < f \leq 60\text{MHz}$: $T_a = -15 \text{ to } +75^\circ\text{C}$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15\text{pF}$	–	4	8	ns
	t_{r2}		$C_L = 50\text{pF}$	–	11	21	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15\text{pF}$	–	4	8	ns
	t_{f2}		$C_L = 50\text{pF}$	–	11	21	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$, $C_L = 15\text{pF}$	$f = 50\text{MHz}$	45	–	55	%
			$f = 60\text{MHz}$	40	–	60	
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$, $C_L = 15\text{pF}$		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

5010HN× series**5V operation/Duty level: CMOS**
 $V_{DD} = 4.5 \text{ to } 5.5\text{V}$, $V_{SS} = 0\text{V}$, $T_a = -40 \text{ to } +85^\circ\text{C}$ unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L = 15\text{pF}$	–	1.5	3.0	ns
	t_{r2}		$C_L = 50\text{pF}$	–	3.0	6.0	
Output fall time	t_{f1}	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L = 15\text{pF}$	–	1.5	3.0	ns
	t_{f2}		$C_L = 50\text{pF}$	–	3.0	6.0	
Output duty cycle ¹	Duty	Measurement cct 6, load cct 1, $V_{DD} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$, $C_L = 50\text{pF}$, $f = 50\text{MHz}$		45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, $V_{DD} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$, $C_L = 15\text{pF}$		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

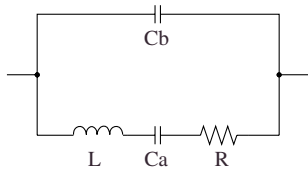
1. The duty cycle characteristic is checked the sample chips of each production lot.

5010HK× series**5V operation/Duty level: TTL**

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r3}	Measurement cct 6, load cct 2, 0.4V to 2.4V	—	1.2	2.4	ns
	t_{r5}					
Output fall time	t_{f3}	Measurement cct 6, load cct 2, 2.4V to 0.4V	—	1.2	2.4	ns
	t_{f5}					
Output duty cycle ¹	Duty	Measurement cct 6, load cct 2, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$, $f = 50MHz$	45	—	55	%
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 2, $V_{DD} = 5.0V$, $T_a = 25^\circ C$, $C_L = 15pF$	—	—	100	ns
Output enable delay time	t_{PZL}		—	—	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.

Current consumption and Output waveform with NPC's standard crystal

for Fundamental oscillator

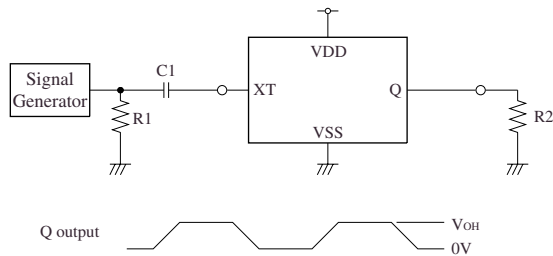
f [MHz]	R [Ω]	L [mH]	Ca [fF]	Cb [pF]
30	17.2	4.36	6.46	2.26
40	16.8	2.90	5.47	2.08

for 3rd overtone oscillator

f [MHz]	R [Ω]	L [mH]	Ca [fF]	Cb [pF]
30	18.62	16.24	1.733	5.337
40	20.53	11.34	1.396	3.989
50	22.17	7.40	1.370	4.105
60	15.37	3.83	1.836	5.191
70	25.42	4.18	1.254	5.170

MEASUREMENT CIRCUITS

Measurement cct 1



2.0V_{P-P}, 10MHz sine wave input signal (3V operation)

3.5V_{P-P}, 10MHz sine wave input signal (5V operation)

C1 : 0.001μF

R1 : 50Ω

R2 : 5010AN×, BN×, DN×, AK×, BK×

3V operation: 263Ω

5V operation: 245Ω

5010FN×, HN×, HK×

3V operation: 275Ω

5V operation: 245Ω

5010CL×

3V operation: 275Ω

5V operation: 250Ω

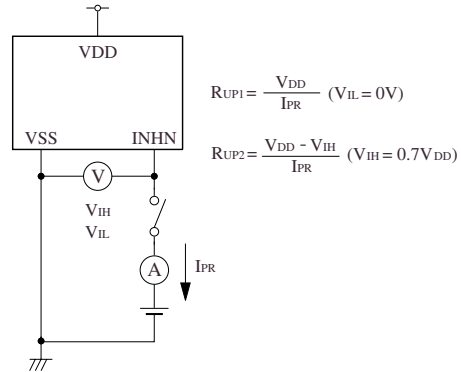
5010EA×, AH×, BH×

3V operation: 1050Ω

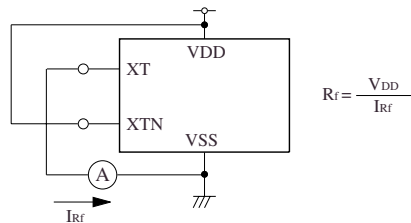
5010EA×, AH×, BH×, FH×

5V operation: 975Ω

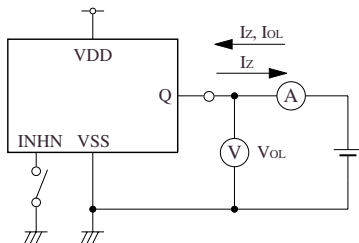
Measurement cct 4



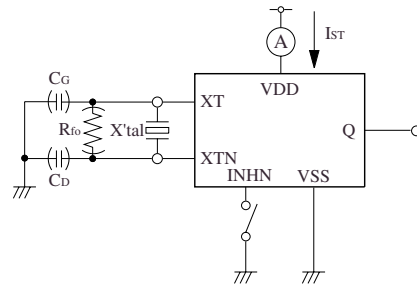
Measurement cct 5



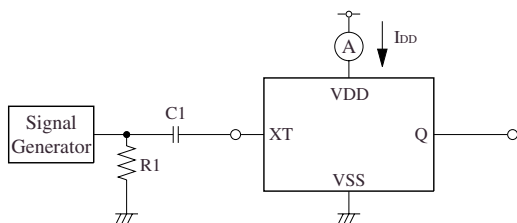
Measurement cct 2



Measurement cct 6



Measurement cct 3



2.0V_{P-P}, 30MHz sine wave input signal (3V operation)

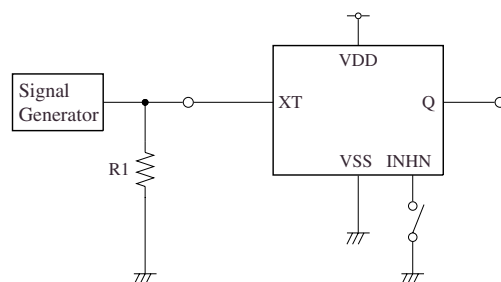
3.5V_{P-P}, 30MHz sine wave input signal (5V operation)

C1 : 0.001μF

R1 : 50Ω

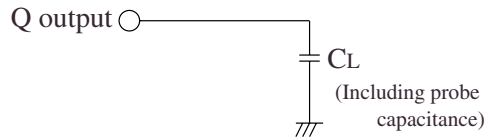
Crystal oscillation
C_G, C_D: 22pF (5010DN×)
R_{f0}: 3.0kΩ (5010H××)

Measurement cct 7



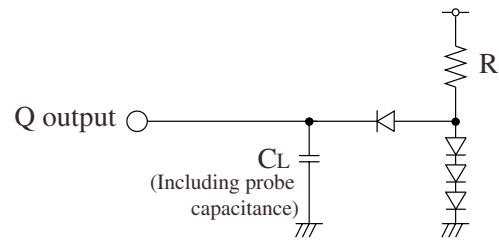
R1 : 50Ω

Load cct 1



$C_L = 15\text{pF}$: DUTY, I_{DD} , t_{r1} , t_{f1}
 $C_L = 30\text{pF}$: t_{r4} , t_{f4}
 $C_L = 50\text{pF}$: t_{r2} , t_{f2}

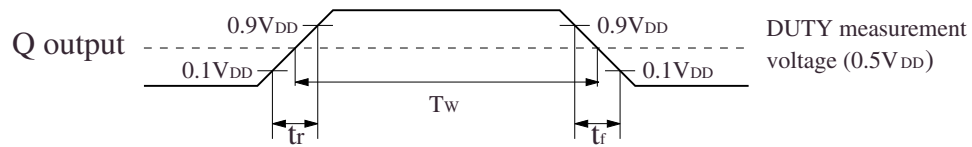
Load cct 2



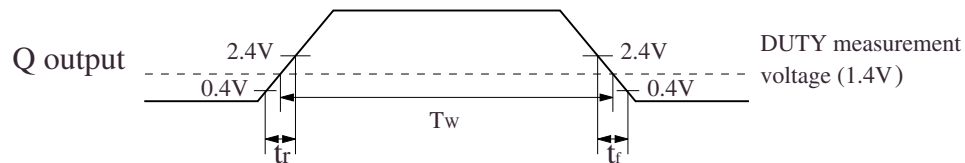
$C_L = 15\text{pF}$: DUTY, I_{DD} , t_{r3} , t_{f3}
 $C_L = 50\text{pF}$: t_{r5} , t_{f5}
 $R = 400\Omega$

Switching Time Measurement Waveform

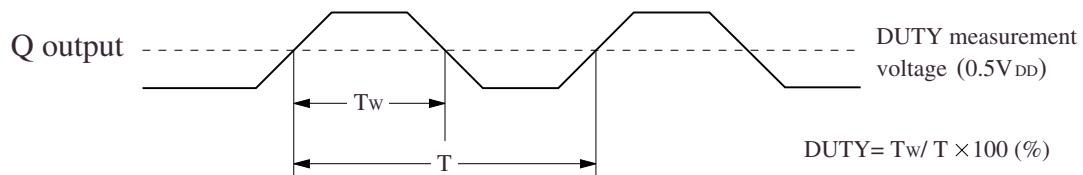
Output duty level (CMOS)



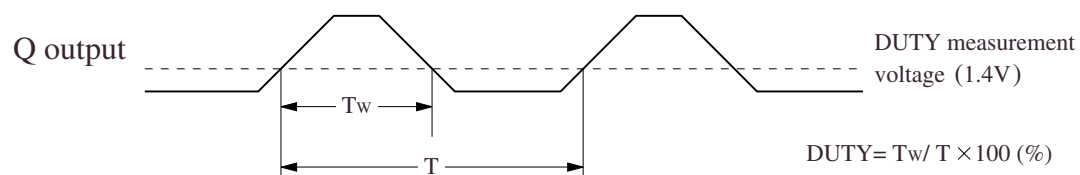
Output duty level (TTL)

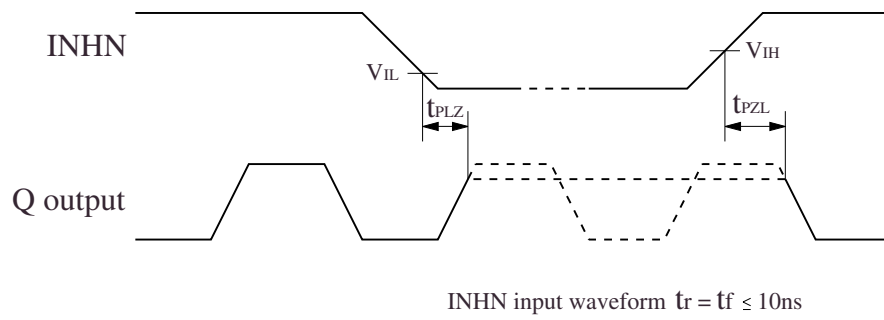


Output duty cycle (CMOS)



Output duty cycle (TTL)



Output Enable/Disable Delay

Note (CL×/EA× series only): when the device is in standby, the oscillator stops. When standby is released, the oscillator starts and stable oscillator output occurs after a short delay.

Please pay your attention to the following points at time of using the products shown in this document.

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The logo for NPC (Seiko NPC Corporation) consists of the letters 'NPC' in a bold, stylized, sans-serif font. The 'N' and 'P' are connected, and the 'C' is a simple curve.

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