SA7120A: 128 Bit Read-only Biphase Coded Transponder for ISO 11784 / 11785 FDX-B (Full Duplex) Application

FEATURES

- EEPROM flexibility of data configuration
- 128 bits of OTP data factory programmed and locked
- Customer specific configuration of stored data
- Data output in Biphase mode
- Biphase data readout conforming to ISO 11784 / 11785 FDX-B full duplex
- Carrier frequency 100 to 300 kHz
- On-chip resonance capacitor
- No external charge storage capacitor required
- On-chip full wave rectifier
- On-chip data modulator
- On-chip high voltage protection / regulation
- On-chip RF frequency clock extractor / prescaler
- Low power dissipation

DESCRIPTION

This device is manufactured in the SAMES 1.2µm N-well EEPROM process. It has 128 bits, factory pre-programmed and locked in EEPROM memory. Read data is Biphase coded.

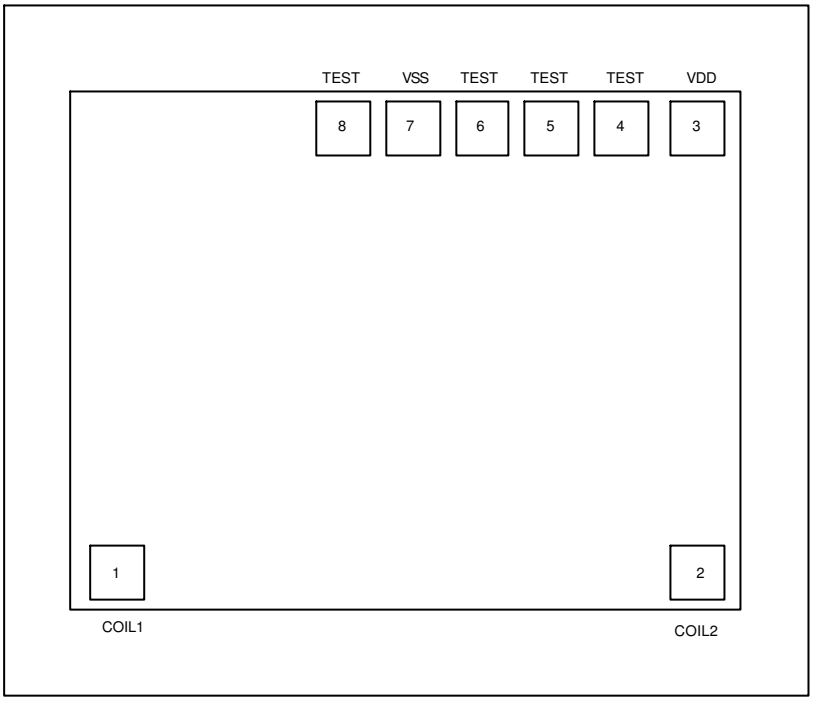
The device has an on-chip rectification circuit that converts the incoming rf signal to DC power feeding V_{DD}. There is also an on-chip data modulator which works in conjunction with the rectifier. The time base is extracted by an on-chip RF clock extractor. High voltage protection across the coil inputs is provided internally. The energy is stored on capacitance on chip due to low internal power consumption. The device has an on-chip resonance capacitor connected between the COIL1 and COIL2 pads. These features result in a single external component count, comprised of, only the coil.

Data is read at the RF interface by means of the on-chip modulator. The stored bits are clocked out sequentially during the read operation. An internal power-on reset is provided which allows the device to start reading out data at low voltages for improved tag range.

APPLICATIONS

- Animal ID ear tag
- Animal ID bolus tag
- Industrial automation
- Asset tracking

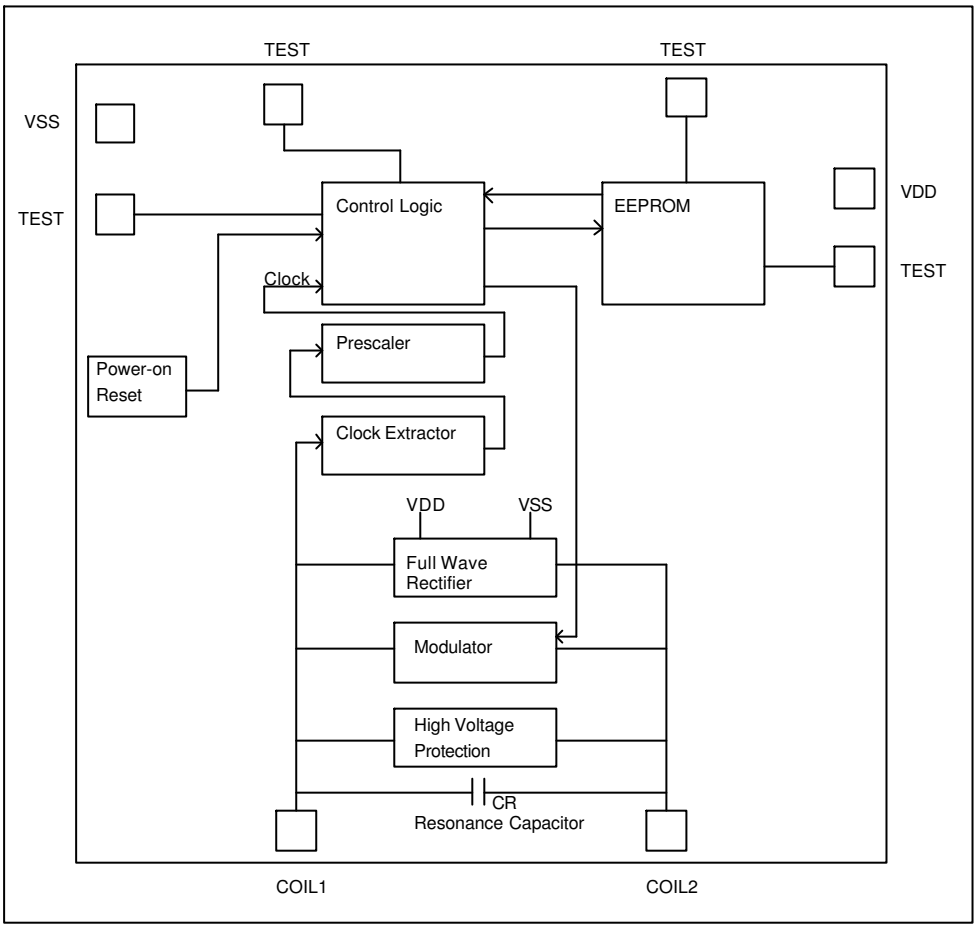
PAD CONNECTIONS



PAD DESCRIPTION

PAD No.	NAME	DESCRIPTION
1	COIL1	External coil connection
2	COIL2	External coil connection
3	V_{DD}	Supply voltage
4	TEST	Test Pad
5	TEST	Test Pad
6	TEST	Test Pad
7	V_{SS}	Ground
8	TEST	Test Pad

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	-0.3	9.4	V	1,2,3,4,5
ESD protection C= 100pF R = 1.5Kohm , Human body model. MIL-STD-883C method 3015	Vpesd	-	TBD	V	3,8
Peak voltage across COIL1 or COIL2 to V_{SS}	$V_{COIL1,2}$ - V_{SS}	-10	+10	V	3,6
Peak current through COIL 1,2	$I_{COIL1,2}$	-30	+30	mA	3,7
Storage temperature	Tst	-55	+125	°C	3

Note 1: Duration not to exceed 10 seconds, and no logic switching.

Note 2: Referenced to Vss

Note 3: Stresses above those listed under " absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating conditions section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Note 4: VDD level when absolute maximum current goes through coil inputs.

Note 5: VDD level when absolute maximum voltage is across coil inputs.

Note 6: Maximum peak voltage at COIL1 or COIL2 of incoming RF signal with V_{SS} as reference. Clamping by front end protection circuitry.

Note 7: Maximum allowed peak current of incoming RF signal.

Note 8: TBD - To be determined.

HANDLING PROCEDURES

Although the device has built-in ESD protection, adherence to anti-static procedures for CMOS devices is required.

ELECTRICAL CHARACTERISTICS

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Dynamic current	I_{DD}		3	6	µA	V_{DD} = 3V
Static current	I_{DDS}			1	µA	V_{DD} = 3V, clock stopped, COIL1 & COIL2 shorted to V_{SS}
Voltage when power-on reset comes out of reset	V_{POR}	1.2	1.6	2	V	During power-up V_{DD} – V_{SS} rising
Histereses on power-on rest	V_{PORH}	200	-	600	mV	Between coming out of reset and going back into reset
Data retention	T_{DR}	10	-	-	years	programmed
Supply voltage	V_{DD}	2	-	5.5 1)	V	At specified current at COIL1 or COIL2,
Operating temperature	Top	-40		+70	°C	

Note: 1) maximum voltage is defined when forcing 10 mA on the coil inputs.

AC Operating Conditions

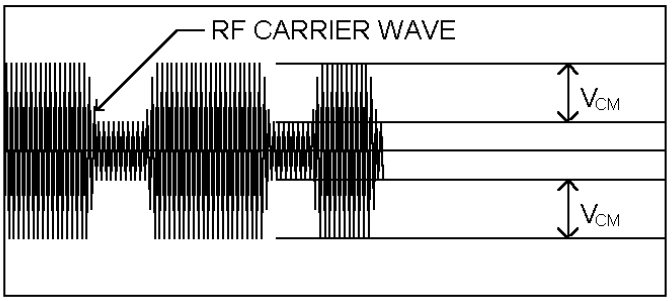
Clocking

Parameter	Symbol	Min	Typ	Max	Unit	Condition
RF carrier frequency at COIL1,2	f_{RF}	50	134	300	kHz	Sustained RF from base station
Number of rf carrier cycles per bit	N_B	-	32	64		Note that for ISO 11784/85 32 cycles must be used. As an option 64 cycles may be used for other custom applications.

Coil Inputs

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Negative excursion of COIL1 or COIL2	V_{CN}	-0.6	-0.65	-0.7	V	Peak level referenced to VSS
Modulated voltage drop	V_{CM}	TBD	3.3	TBD	V	Unmodulated COIL1 or COIL2 voltage referenced to V_{SS} = 5.5V
Modulated voltage drop	V_{CM}	TBD	3.0	TBD	V	Unmodulated COIL1 or COIL2 voltage referenced to V_{SS} = 5.0V
Modulated voltage drop	V_{CM}	TBD	0.875	TBD	V	Unmodulated COIL1 or COIL2 voltage referenced to V_{SS} = 2.5
Resonance Capacitor	C_R	1)	75	1)	pF	Measured between COIL1 and COIL2

Note: 1) for a single batch the tolerance is ±3%. From batch to batch the tolerance is ±30%.
TBD - To be determined.



FUNCTIONAL DESCRIPTION

The circuit is built up out of several functional blocks, control logic, coil interface, the power-on reset, and the memory module (EEPROM), The chip activates automatically during power-up as a result of the built in power-on reset.

Coil Interface

Power is derived from a full wave rectifier bridge. Data modulation takes place by loading the coil inputs to the bridge with a modulating circuit. The coil interface includes on-chip high voltage protection. The system clock for the chip is derived by means of a clock extractor coupled to the rectifier circuit. The Clock extractor / prescaler is the time base generator for data reading. Data is read from the EEPROM to the coil interface where the rf signal is modulated by the data in the Biphase coded mode.

Memory Array

Data storage:

The data EEPROM is arranged in an 16X8 bit array composed of 16 columns of 8 bit bytes. The 128 bits of data stored in the array can be configured in any way as agreed with the client, and is factory programmed and locked in that way. This gives OTP (One Time Programmable) security.

Memory map

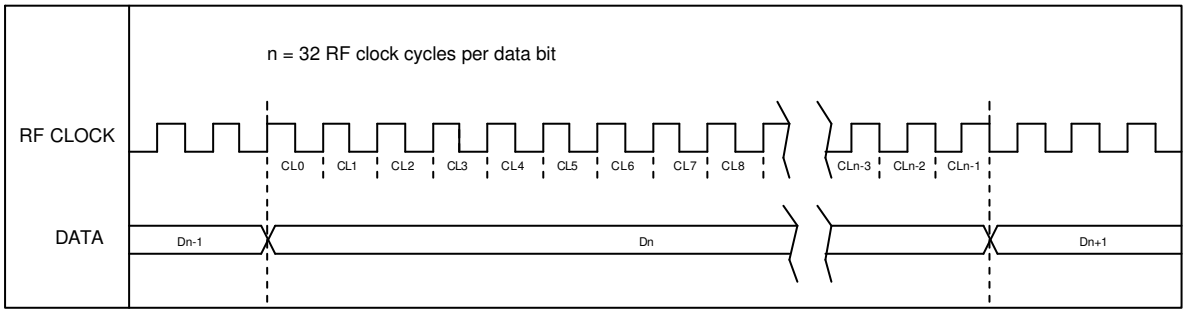
The memory is mapped as described in ISO 11784 code structure and the code is programmed during wafer test. For other special requirements the flexibility of programming allows custom memory mapping.

Control logic

The control logic gets its clock from the clock extractor / prescaler and facilitates the reading of the data stored in the data EEPROM.

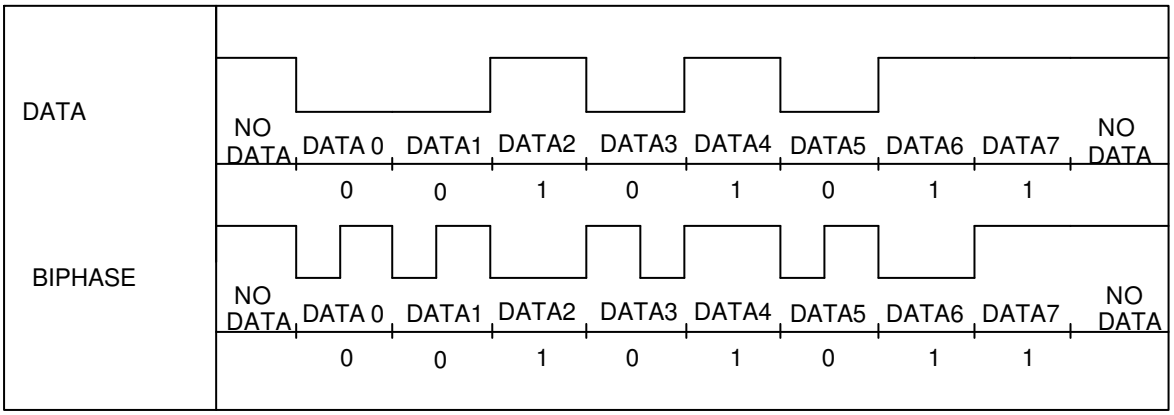
TIMING SPECIFICATIONS

The COIL1 and COIL2 pads modulate the incoming rf signal with Biphase encoded data. The data will repeatedly be read out serially until the power is reduced sufficiently to activate the power on reset again. There are 32 rf carrier cycles for each data bit. This is the nominal setting to comply with ISO 11784/11785. An optional setting of 64 rf cycles per bit can be selected during wafer manufacture.



DATA OUTPUT

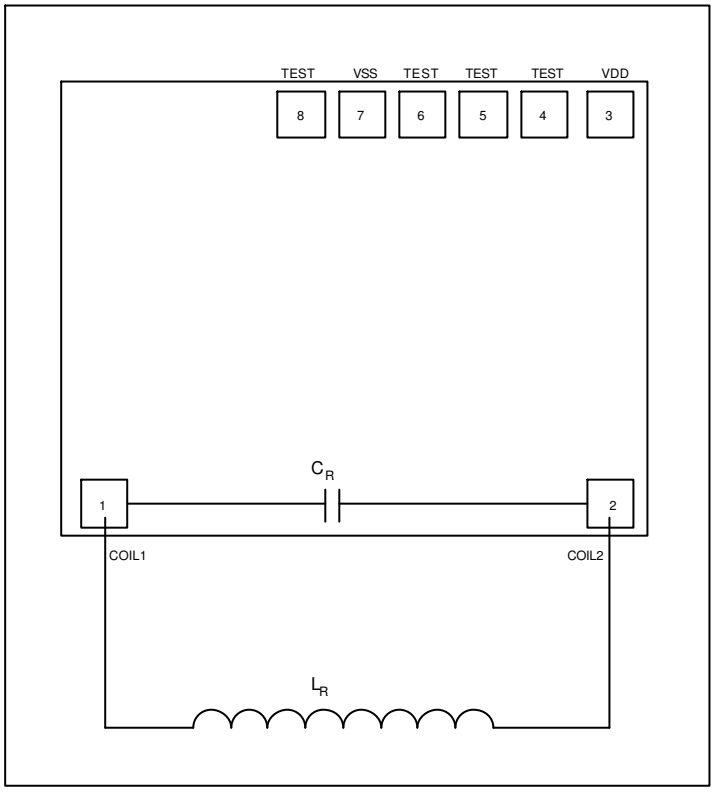
Data output takes place according to biphase encoding.



TYPICAL APPLICATION

The chip powers up via the COIL1 and COIL2 pads, deriving its energy from the rf carrier wave through the resonating tank circuit made up by the external inductor, L_R, and internal capacitor, C_R. An optional additional external capacitor can be added for special requirements.

The data will automatically start modulating the rf signal as soon as the chip has powered up to the power-on reset level. The built in voltage protection and regulation insures protection against high voltage from the tank circuit.



The value of L_R is determined by the following relationship.

$f_R = 1 / (2 \pi \sqrt{L_R \cdot C_R})$

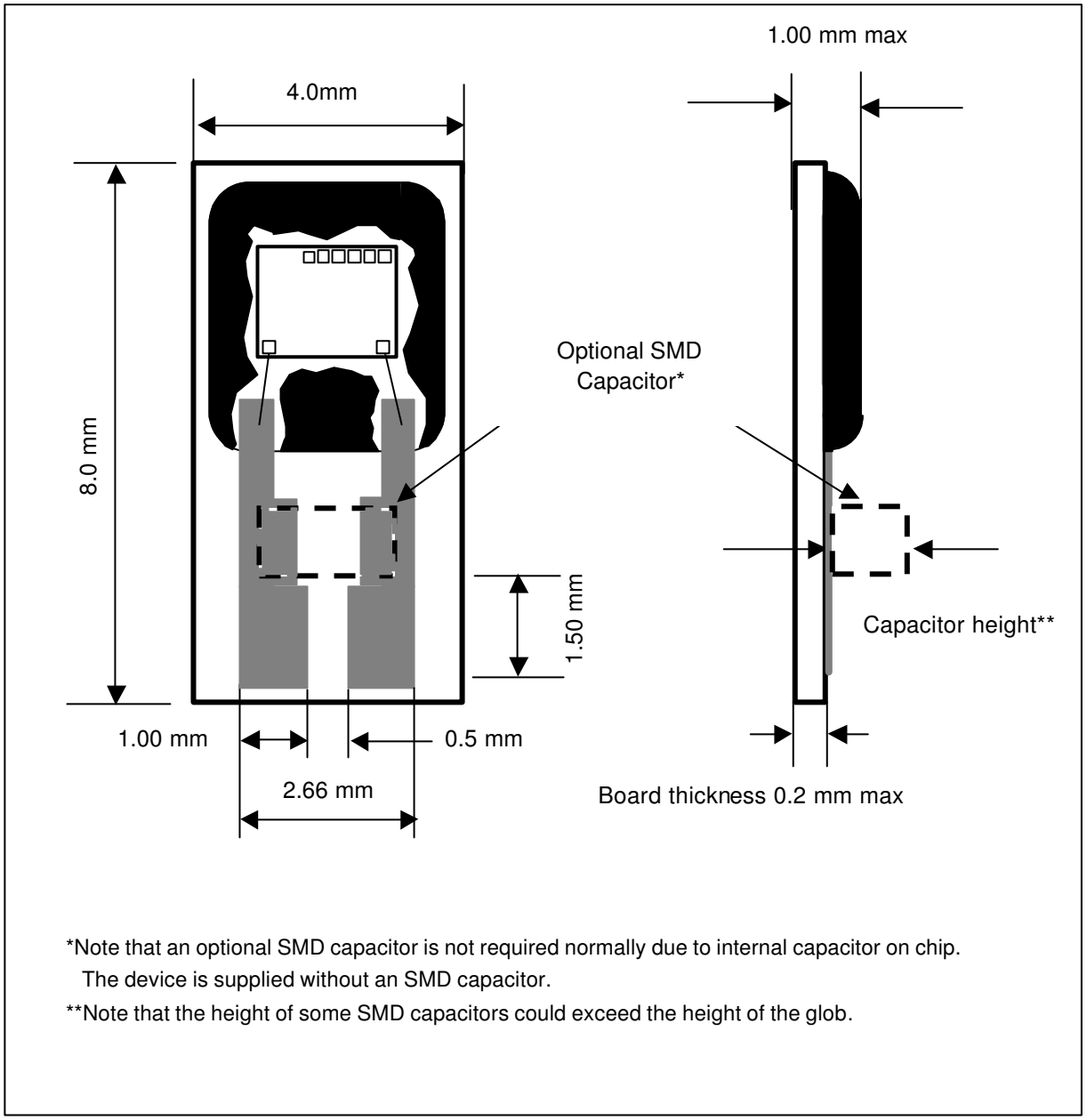
Where f_R is the resonance frequency.

For a typical internal C_R of 75 pf and for f_R at 134.2 kHz,

L_R = 18.75 mH

PACKAGE AND ORDERING INFORMATION

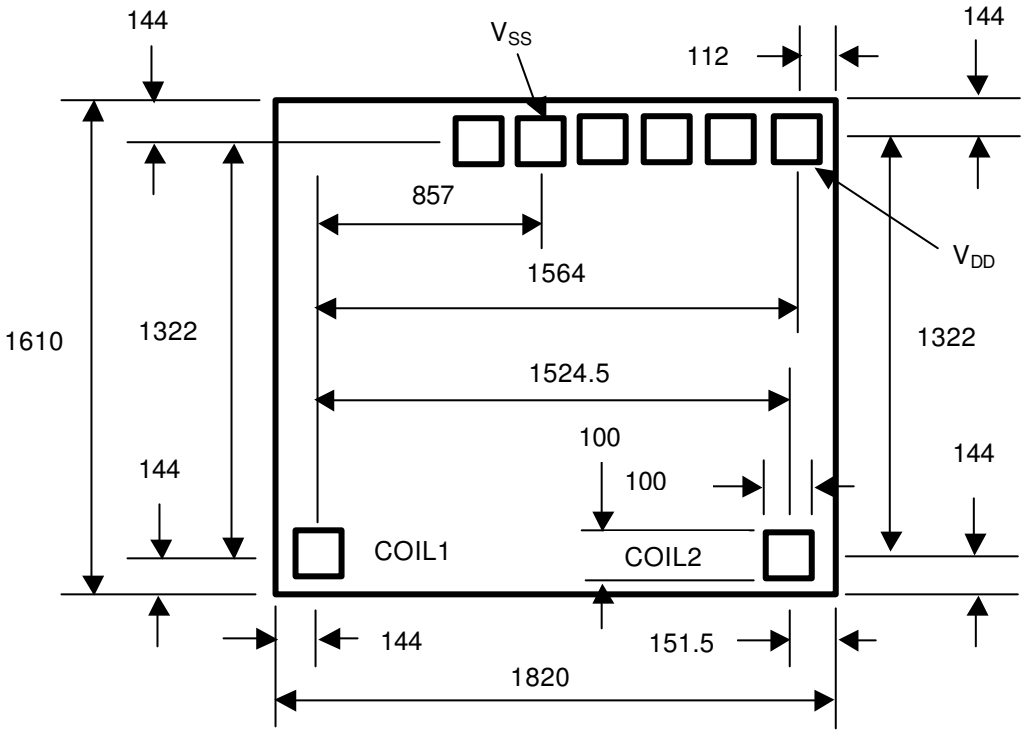
PCB FORM



*Note that an optional SMD capacitor is not required normally due to internal capacitor on chip.
The device is supplied without an SMD capacitor.

**Note that the height of some SMD capacitors could exceed the height of the glob.

CHIP FORM



Dimensions are in micrometers
IC Thickness is 280 micrometers ±25 micrometers
The outer dimensions of the IC is given as the distance from saw channel centre to saw channel centre and will be smaller than indicated due to material removed during sawing

ORDERING INFORMATION

Data rate at 32 clocks per bit (compulsory for ISO 11784/85)
In Chip form SA7120 32 IC
In PCB form SA7120 32 COB

Data rate at 64 clocks per bit (custom option which is not ISO 11784/85)
In Chip form SA7120 64 IC
In PCB form SA7120 64 COB

Any sales or technical questions may be posted to our e-mail address below:
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For the latest updates on datasheets, please visit our web site:
http://www.sames.co.za

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