Freescale Semiconductor
Technical Data

Document Number: MML09231H
Rev. 0, 5/2013

RoHS

Enhancement Mode pHEMT Technology (E−pHEMT)

Low Noise Amplifier

MML09231HT1

700−1400 MHz, 17.2 dB
24.5 dBm, 0.36 dB NF
E−pHEMT

DFN 2 × 2
PLASTIC

The MML09231H is a single−stage low noise amplifier (LNA) with active bias and high isolation for use in cellular infrastructure applications. It is designed for a range of low noise, high linearity applications such as small cell, tower mounted amplifiers (TMA) and receiver front−end circuits. It operates from a single voltage supply and is suitable for applications with frequencies from 700 to 1400 MHz such as ISM, GSM, W−CDMA and LTE.

Features

- Ultra Low Noise Figure: 0.36 dB @ 900 MHz
- Frequency: 700−1400 MHz
- Unconditionally Stable Over Temperature
- High Reverse Isolation: −21 dB @ 900 MHz
- P1dB: 24.5 dBm @ 900 MHz
- Small−Signal Gain: 17.2 dB @ 900 MHz (adjustable externally)
- Third Order Output Intercept Point: 37.4 dBm @ 900 MHz
- Single 5 Volt Supply
- Power−down Pin
- Supply Current: 55 mA
- 50 Ohm Operation (some external matching required)
- Cost−effective 8−pin, 2 mm DFN Surface Mount Plastic Package
- In Tape and Reel. T1 Suffix = 1,000 Units, 12 mm Tape Width, 7−inch Reel.

Table 1. Typical Performance (1)

Characteristic	Symbol	700 MHz	900 MHz	1400 MHz	Unit
Noise Figure (2a)	NF	0.46(b)	0.36(b)	0.45(b)	dB
Input Return Loss (S11)	IRL	−17	−15	−14	dB
Output Return Loss (S22)	ORL	−14	−15	−15	dB
Small−Signal Gain (S21)	G_p	19	17.2	13.2	dB
Power Output @ 1dB Compression	P1dB	24	24.5	24	dBm
Third Order Input Intercept Point	IIP3	17	20.2	23.8	dBm
Third Order Output Intercept Point	OIP3	36	37.4	37	dBm

1. V_{DD} = 5 Vdc, T_A = 25°C, 50 ohm system, application circuit tuned for specified frequency.
2. (a) Noise figure value calculated with connector losses removed. (b) Z_{in} = 50 Ω.

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	6	V
Supply Current	I_{DD}	150	mA
RF Input Power	P_{in}	20	dBm
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature (3)	T_J	150	°C

3. For reliable operation, the junction temperature should not exceed 150°C.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value (4)	Unit
Thermal Resistance, Junction to Case Case Temperature 95°C, 5 Vdc, 55 mA, no RF applied	$R_{\theta JC}$	77	°C/W

4. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1955.

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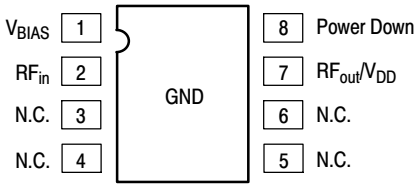
Table 4. Electrical Characteristics (V_{DD} = 5 Vdc, 900 MHz, T_A = 25°C, 50 ohm system, in Freescale Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Small−Signal Gain (S21)	G_p	15.8	17.2	—	dB
Input Return Loss (S11)	IRL	—	−15	—	dB
Output Return Loss (S22)	ORL	—	−15	—	dB
Power Output @ 1dB Compression	P1dB	—	24.5	—	dBm
Third Order Input Intercept Point	IIP3	—	20.2	—	dBm
Third Order Output Intercept Point	OIP3	—	37.4	—	dBm
Reverse Isolation (S12)	|S12|	—	−21	—	dB
Noise Figure (1)	NF	—	0.36	—	dB
Supply Current (2,3)	I_{DD}	40	55	70	mA
Supply Voltage (2)	V_{DD}	—	5	—	V
Supply Current in Power Down Mode	I_{PD}	—	1.1	—	mA
Logic Voltage for Power Down (4) Input High Voltage Input Low Voltage	V_{PD}	 2.2 0	 — —	 V_{DD} 0.5	V

1. Noise figure value calculated with connector losses removed.
2. For reliable operation, the junction temperature should not exceed 150°C.
3. DC current measured with no RF signal applied.
4. Limits derived from device characterization.

Table 5. Functional Pin Description

Pin Number	Pin Function
1	V_{BIAS}
2	RF_{in}
3	No Connection
4	No Connection
5	No Connection
6	No Connection
7	RF_{out}/Supply Voltage
8	Power Down (active high)



(Top View)

Note: Exposed backside of the package is DC and RF ground.

Figure 1. Pin Connections

Table 6. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD 22−A114)	1B, passes 700 V
Machine Model (per EIA/JESD 22−A115)	A
Charge Device Model (per JESD 22−C101)	IV

Table 7. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22−A113, IPC/JEDEC J−STD−020	1	260	°C

50 OHM APPLICATION CIRCUIT: 900 MHz

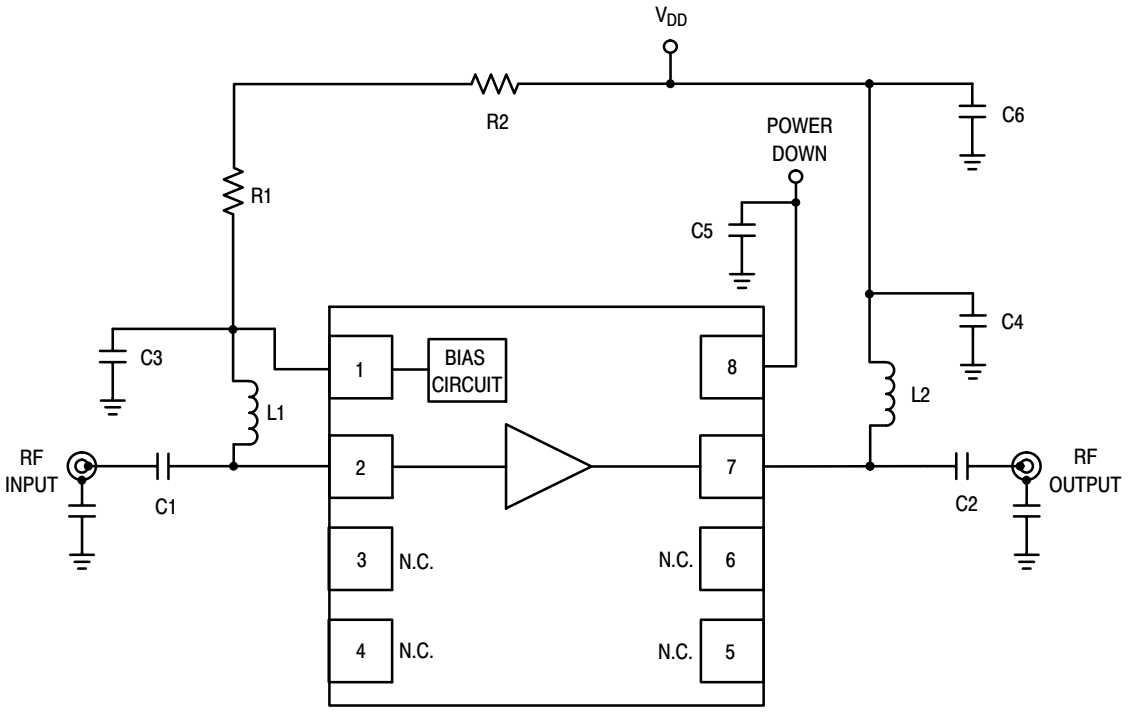
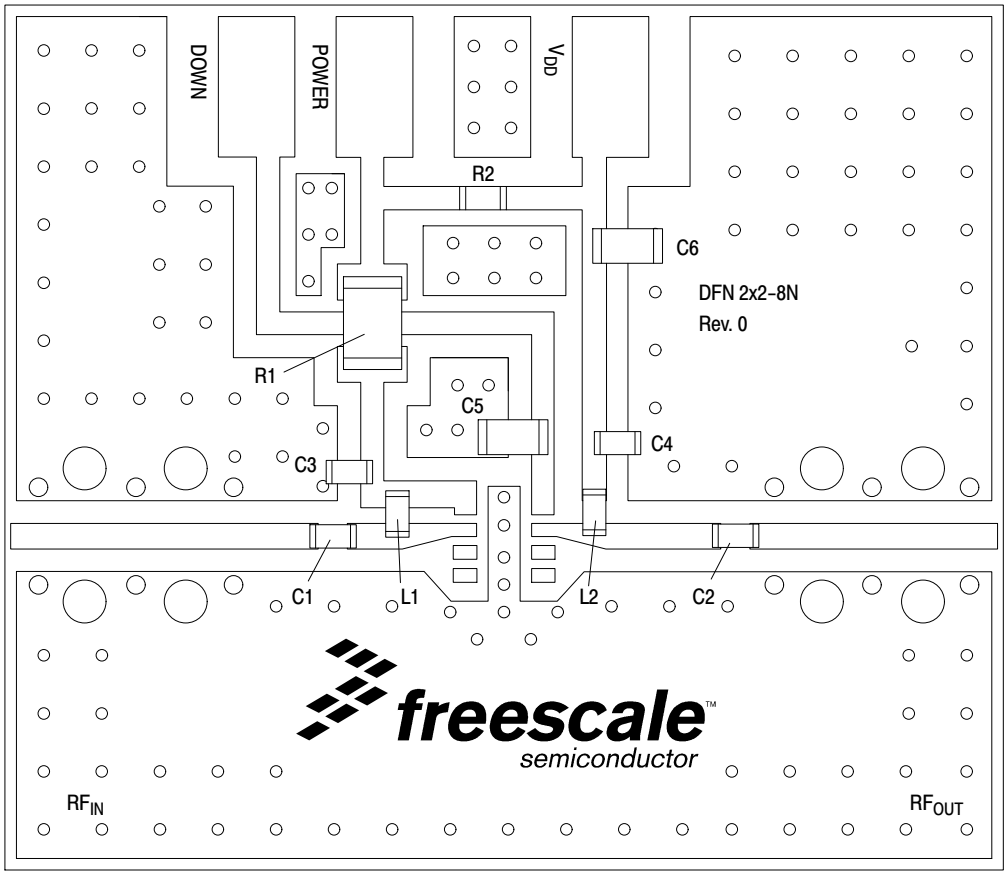


Figure 2. MML09231H Test Circuit Schematic

Table 8. MML09231H Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	100 pF Chip Capacitor	GRM1555C1H101JA01	Murata
C2	180 pF Chip Capacitor	GRM1555C1H181JA01	Murata
C3	27 pF Chip Capacitor	GRM1555C1H270JA01	Murata
C4	220 pF Chip Capacitor	GRM1555C1H221JA01	Murata
C5, C6	1000 pF Chip Capacitors	GRM1885C1H102JA01	Murata
L1	20 nH Chip Inductor	0402HP-20NXGLW	Coilcraft
L2	47 nH Chip Inductor	0402HP-47NXGLW	Coilcraft
R1	4.7 kΩ, 1/10 W Chip Resistor	CR21-472J-B	Kyocera
R2	0 Ω, 1 A Chip Resistor	CR0402-J/-000GLFCT	Bourns
PCB	0.02″, ε_r = 3.50	RO4350B	Rogers

50 OHM APPLICATION CIRCUIT: 900 MHz



NOTE: To achieve optimal noise performance, it is critical that proper biasing, input matching, supply decoupling and grounding are employed.

Figure 3. MML09231H Test Circuit Component Layout

Table 8. MML09231H Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	100 pF Chip Capacitor	GRM1555C1H101JA01	Murata
C2	180 pF Chip Capacitor	GRM1555C1H181JA01	Murata
C3	27 pF Chip Capacitor	GRM1555C1H270JA01	Murata
C4	220 pF Chip Capacitor	GRM1555C1H221JA01	Murata
C5, C6	1000 pF Chip Capacitors	GRM1885C1H102JA01	Murata
L1	20 nH Chip Inductor	0402HP-20NXGLW	Coilcraft
L2	47 nH Chip Inductor	0402HP-47NXGLW	Coilcraft
R1	4.7 kΩ, 1/10 W Chip Resistor	CR21-472J-B	Kyocera
R2	0 Ω, 1 A Chip Resistor	CR0402-J/-000GLFCT	Bourns
PCB	0.02″, ε_r = 3.50	RO4350B	Rogers

(Test Circuit Component Designations and Values repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 900 MHz

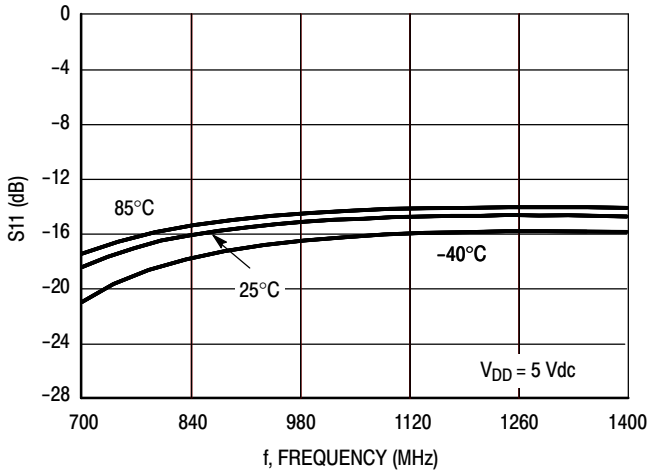


Figure 4. S11 versus Frequency versus Temperature

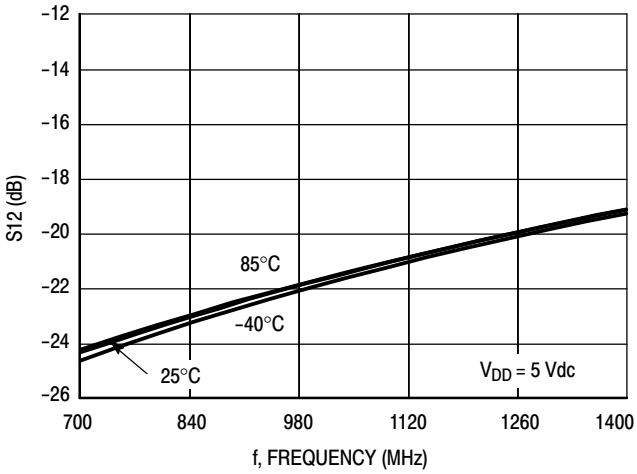


Figure 5. S12 versus Frequency versus Temperature

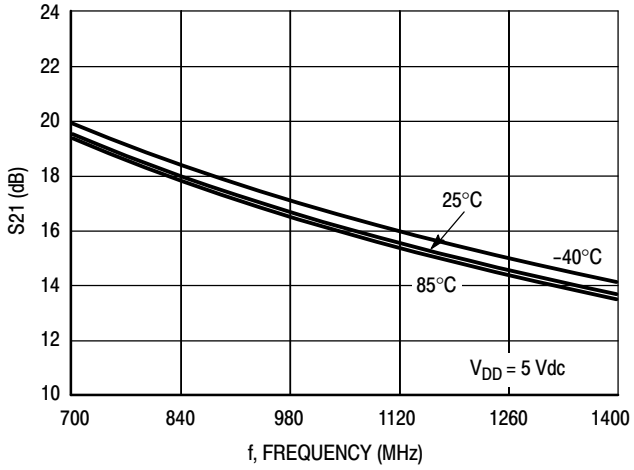


Figure 6. S21 versus Frequency versus Temperature

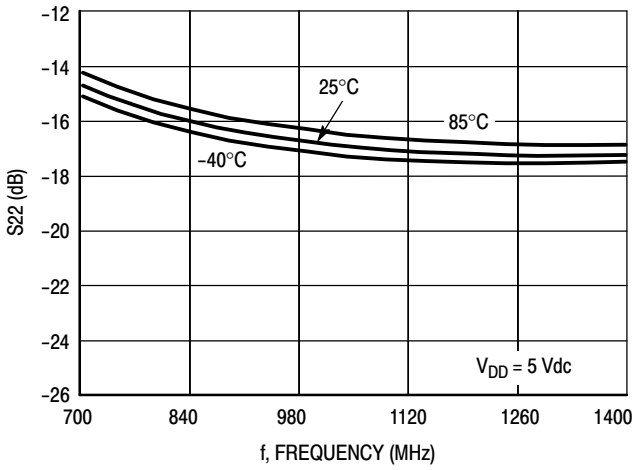


Figure 7. S22 versus Frequency versus Temperature

50 OHM TYPICAL CHARACTERISTICS: 900 MHz

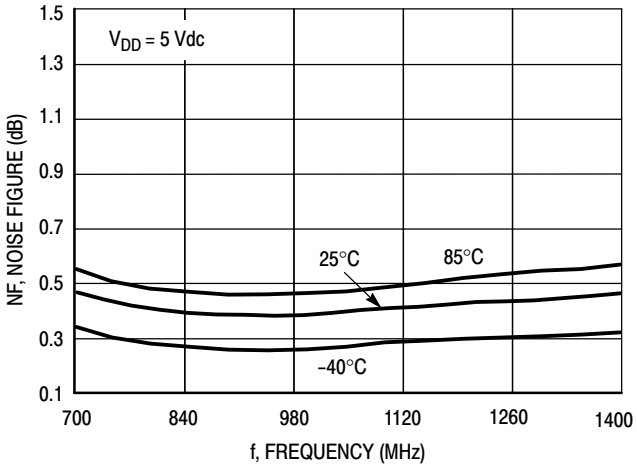


Figure 8. Noise Figure versus Frequency versus Temperature

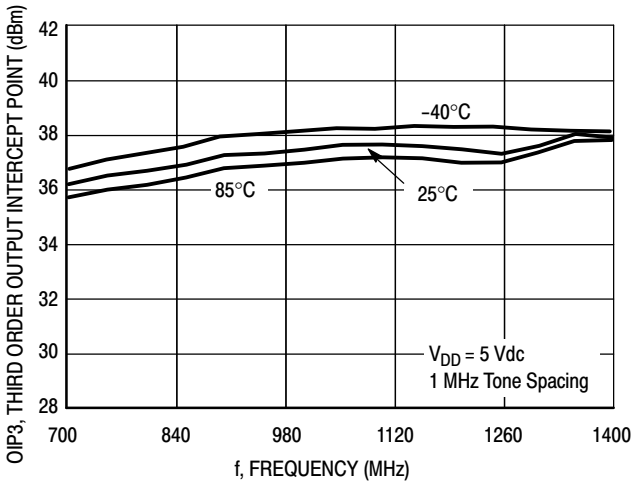


Figure 9. Third Order Output Intercept Point (Two−Tone) versus Frequency versus Temperature

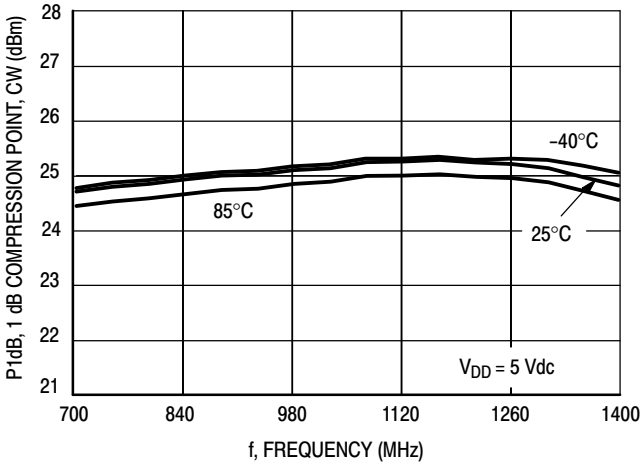


Figure 10. P1dB versus Frequency versus Temperature, CW

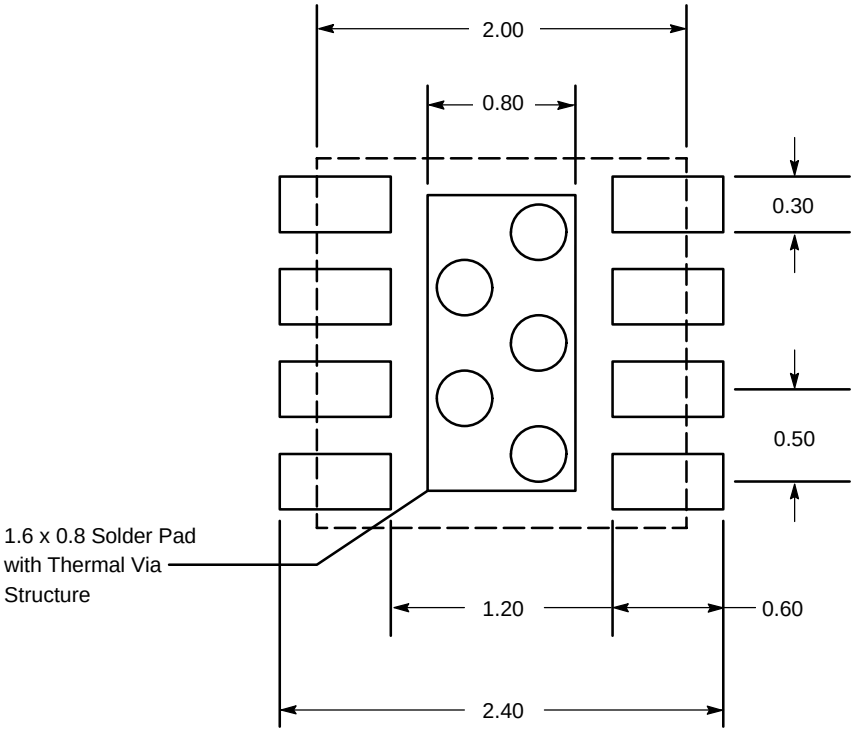


Figure 11. PCB Pad Layout for DFN 2 × 2

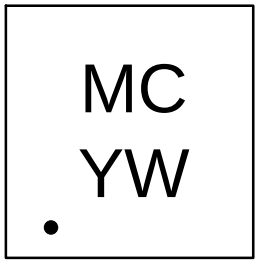
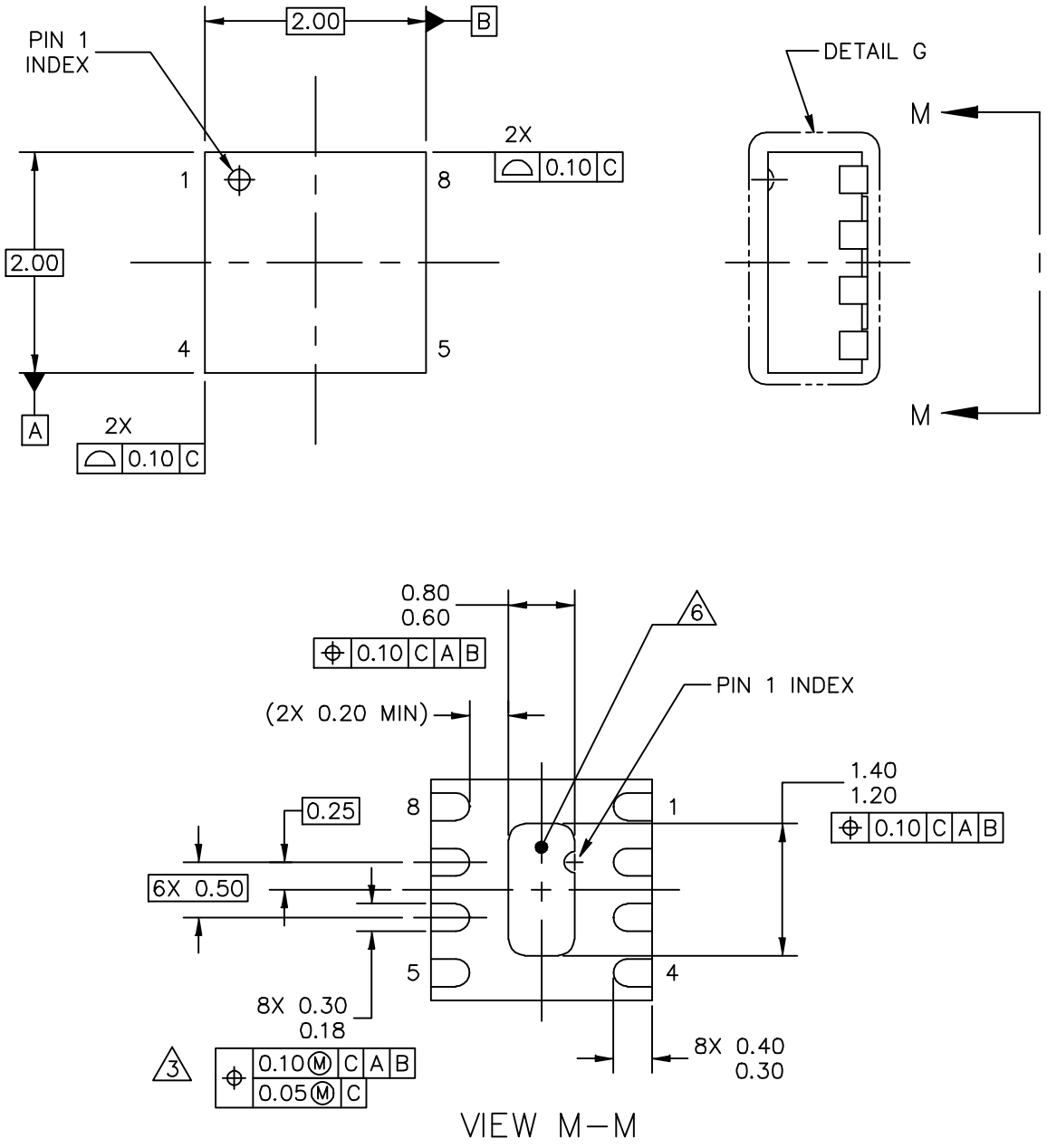


Figure 12. Product Marking

PACKAGE DIMENSIONS



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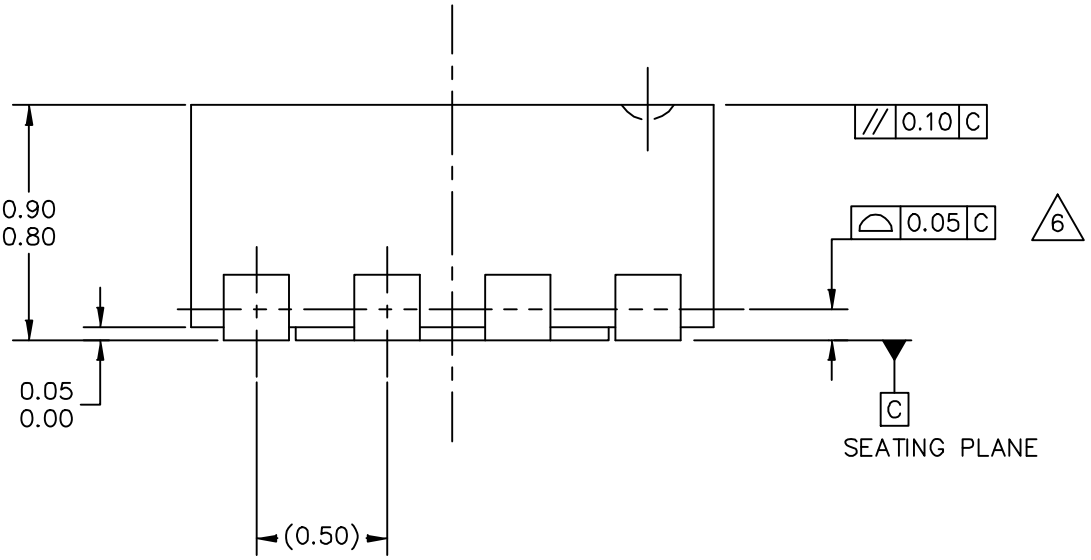
TITLE: THERMALLY ENHANCED DUAL FLAT NON–LEADED PACKAGE (DFN) 8 TERMINAL, 0.5 PITCH (2 X 2 X 0.85)	DOCUMENT NO: 98ASA00228D	REV: O
	CASE NUMBER: 2132–01	14 MAY 2010
	STANDARD: NON–JEDEC	



DETAIL G
VIEW ROTATED 90° CW

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	STANDARD: NON–JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 – 2009

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMIMAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THIS DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

4. MAX. PACKAGE WARPAGE IS 0.05 mm.

5. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.

6. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where Freescale is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local Freescale Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2013	• Initial Release of Data Sheet

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