

Legacy Device: Philips/Signetics S8X371

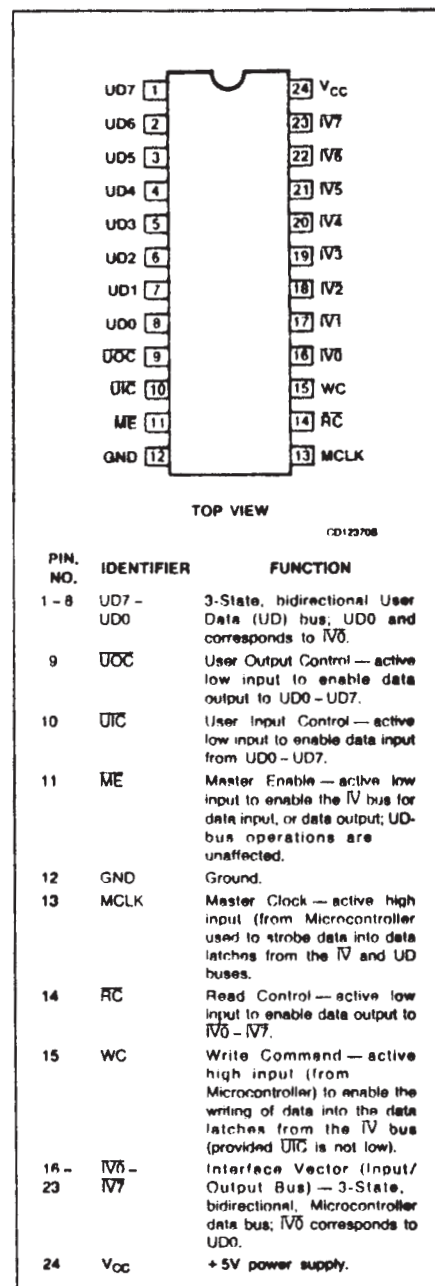
#### DESCRIPTION

The 8X371 I/O Port is a bidirectional device designed for use as an interface element in systems that use TTL-compatible busses. Typically, the 8X371 is used with the 8X305 Microcontroller and its associated interface Vector ( $\overline{IV}$ ) bus; however, it can also be used with the 8X300 Microcontroller or an equivalent microprocessor. The 8X371 is functionally the same and pin-for pin compatible with the older 8T31/8X31 but features improved performance and increased drive current. As shown in the logic diagram of Figure 1, the 8X371 consists of eight identical data latches — bits 0 through 7. The latches are accessed from either of two 8-bit busses — the Microcontroller ( $\overline{IV}$  bus) and the user data (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time; in such situations, the user bus always has priority. A Master Enable ( $\overline{ME}$ ) input over the  $\overline{IV}$  bus. The data latches are transparent, in that, while either bus is enabled for input, all input-data transitions are propagated to the other bus, if enabled for output.

#### FEATURES

- Two bidirectional 8-bit busses
- Independent bus operation (user-bus priority for data entry)
- User data input synchronous with respect to MCLK
- 3-State TTL outputs with high-drive capabilities
- Power-up to predetermined logic state
- Directly compatible with 8X305 (or 8X300) Microcontrollers
- Single +5V supply
- 0.4" 24-pin DIP

#### PIN CONFIGURATION





**Figure 1. Logic Diagram for 8X371 I/O Port**

## FUNCTIONAL OPERATION

### UD Bus Control

As shown in Table 1, the User Data (UD) bus interface is controlled by the  $\overline{UI\overline{C}}$  and  $\overline{UOC}$  inputs. Data input to the UD bus is synchronous with MCLK, that is, with  $\overline{UI\overline{C}}$  low, information is written into the data latches only when MCLK is high. Output drivers on the UD bus are enabled when  $\overline{UOC}$  is low and  $\overline{UI\overline{C}}$  is high.

Table 1. Input/Output Control of UD Bus

$\overline{UI\overline{C}}$	$\overline{UOC}$	MCLK	FUNCTION OF UD BUS
H	L	X	Output data
L	X	H	Input data
L	X	L	Inactive
H	H	X	Inactive

#### NOTE:

X = don't care

### $\overline{IV}$ Bus Control

Input/output control of the  $\overline{IV}$  bus is shown in Table 2; this bus is controlled by  $\overline{RC}$ , WC,  $\overline{ME}$ ,

Table 2. Input/Output Control of  $\overline{IV}$  Bus

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{UI\overline{C}}$	FUNCTION OF $\overline{IV}$ BUS
L	L	L	X	X	Output Data
L	X	H	H	H	Input Data
L	H	L	X	X	Inactive
L	X	H	X	L	Inactive
L	X	H	L	H	Inactive
H	X	X	X	X	Inactive

and MCLK. The  $\overline{IV}$  bus is enabled for output (Microcontroller read operation) when  $\overline{ME}$ ,  $\overline{RC}$ , and WC are all low. Data is written into the data latches from the  $\overline{IV}$  bus when  $\overline{ME}$  is low and both WC and MCLK are high. To avoid data-input conflicts, inputs from the  $\overline{IV}$  bus are inhibited when  $\overline{UI\overline{C}}$  is low; under all other conditions, the  $\overline{IV}$  and UD busses operate independently. The Microcontroller Left Bank ( $\overline{LB}$ ) and Right Bank ( $\overline{RB}$ ) outputs can control the  $\overline{ME}$  inputs for two banks of I/O devices, thus acting as a ninth address bit. If more than one I/O Port (including the addressable parts — 8X372, 8X376, 8X382, etc.) are to be connected to the same bank

( $\overline{LB}$  or  $\overline{RB}$ ) of the Microcontroller, selection of each 8X371 must be accomplished with external logic to avoid bus conflicts.

### Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note: A logic "1" in Microcontroller software corresponds to a high-level on the UD bus even though the  $\overline{IV}$  bus is inverted.) The 8X371 wakes up in the unselected state with all data bits latched at the "logic 1" level (UD) bus outputs high if enabled).

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Power supply voltage	+7	$V_{DC}$
$V_I$	Input voltage	+5.5	$V_{DC}$
$T_{STG}$	Storage temperature range	-65 to +150	$^{\circ}C$

**DC ELECTRICAL CHARACTERISTICS (Military)**  $4.75V \leq V_{CC} \leq 5.25V$ ,  $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$V_{CC}$	Supply voltage		4.5	5.0	5.5	V
$V_{IH}$	High level input voltage		2.0			V
$V_{IL}$	Low level input voltage				0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}; I_I = -10\text{mA}$			-1.5	V
$I_{IH}$	High level input current <sup>1</sup>	$V_{CC} = \text{MAX}; V_{IH} = 2.7V$			100	$\mu\text{A}$
$I_{IL}$	Low level input current <sup>1</sup>	$V_{CC} = \text{MAX}; V_{IL} = 0.5V$			-550	$\mu\text{A}$
$V_{OL}$	Low level output voltage	$V_{CC} = \text{MIN}; I_{OL} = 16\text{mA}$			0.55	V
	$\overline{IV}$ bus ( $\overline{IV0}=\overline{IV7}$ ), User bus (UD4 - UD7)	$V_{CC} = \text{MIN}; I_{OL} = 24\text{mA}$			0.55	V
$V_{OH}$	High level output voltage	$V_{CC} = \text{MIN}; I_{OH} = -3.2\text{mA}$	2.4			V
$I_{OS}$	Short circuit output current <sup>2</sup>	$V_{CC} = \text{MAX}$	-20			mA
	$\overline{IV}$ bus ( $\overline{IV0}=\overline{IV7}$ ), UD bus (UD4 - UD7)	$V_{CC} = \text{MAX}$	-10			mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}; \overline{ME} = \overline{UOC} = V_{CC}$			150	mA

**MILITARY ONLY****DC ELECTRICAL CHARACTERISTICS (Commercial)**  $4.75V \leq V_{CC} \leq 5.25V$ ,  $-0^{\circ}C \leq T_C \leq +70^{\circ}C$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$V_{CC}$	Supply voltage		4.75	5.0	5.25	V
$V_{IH}$	High level input voltage		2.0			V
$V_{IL}$	Low level input voltage				0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}; I_I = -10\text{mA}$			-1.5	V
$I_{IH}$	High level input current <sup>1</sup>	$V_{CC} = \text{MAX}; V_{IH} = 2.7V$		5	100	$\mu\text{A}$
$I_{IL}$	Low level input current <sup>1</sup>	$V_{CC} = \text{MAX}; V_{IL} = 0.5V$		-350	-550	$\mu\text{A}$
$V_{OL}$	Low level output voltage	$V_{CC} = \text{MIN}; I_{OL} = 16\text{mA}$			0.55	V
	$\overline{IV}$ bus ( $\overline{IV0}=\overline{IV7}$ ), User bus (UD4 - UD7)	$V_{CC} = \text{MIN}; I_{OL} = 24\text{mA}$			0.55	V
$V_{OH}$	High level output voltage	$V_{CC} = \text{MIN}; I_{OH} = -3.2\text{mA}$	2.4			V
$I_{OS}$	Short circuit output current <sup>2</sup>	$V_{CC} = \text{MAX}$	-20			mA
	$\overline{IV}$ bus ( $\overline{IV0}=\overline{IV7}$ ), UD bus (UD4 - UD7)	$V_{CC} = \text{MAX}$	-10			mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}; \overline{ME} = \overline{UOC} = V_{CC}$		90	150	mA

**COMMERCIAL ONLY****NOTES:**

1. The input current includes the 3-State leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.

**AC ELECTRICAL CHARACTERISTICS**  $4.5V \leq V_{CC} \leq 5.5V$ ,  $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ 

SYMBOL	PARAMETER	REFERENCES		TEST CONDITIONS	LIMITS		UNIT
		From	To		Min	Max	
Pulse Widths:							
T <sub>w1</sub>	Clock high	↑MCLK	↓MCLK		30		ns
t <sub>w2</sub>	User input control	↓UIC	↑UIC	MCLK = High	35		ns
Propagation Delays:							
t <sub>PD1</sub>	UD propagation delay	UD	IV	MCLK = High RC = WC = ME = UIC = Low		45	ns
t <sub>PD2</sub>	UD clock delay	↑MCLK	IV	UD = stable, RC = WC = ME = UIC = Low		55	ns
t <sub>PD3</sub>	UD input delay	↓UIC	IV	UD = Stable; MCLK = High RC = WC = ME = Low		55	ns
t <sub>PD4</sub>	IV data propagation delay	IV	UD	MCLK = WC = UIC = High; ME = UOC = RC = Low		45	ns
t <sub>PD5</sub>	IV data clock delay	↑MCLK	UD	WC = UIC = High; IV = Stable ME = UOC = RC = Low		55	ns
Output Enable Timing:							
t <sub>OE1</sub>	UD output enable	↓UOC	UD	UIC = High		45	ns
t <sub>OE2</sub>	UD input recovery	↑UIC	UD	UOC = Low		45	ns
t <sub>OE3</sub>	IV data master enable	↓ME	IV	WC = RC = Low		45	ns
t <sub>OE4</sub>	IV data read enable	↓RC	IV	WC = ME = Low		45	ns
t <sub>OE5</sub>	IV data write recovery	↓WC	IV	RC = ME = Low		45	ns
Output Disable Timing:							
t <sub>OD1</sub>	UD output disable	↑UOC	UD	UIC = High		40	ns
t <sub>OD2</sub>	UD input override	↓UIC	UD	UOC = Low		45	ns
t <sub>OD3</sub> <sup>3</sup>	IV data master disable	↑ME	IV	WC = RC = Low		40	ns
t <sub>OD4</sub> <sup>3</sup>	IV data read disable	↑RC	IV	WC = ME = Low		40	ns
t <sub>OD5</sub> <sup>3</sup>	IV data write override	↑WC	IV	RC = ME = Low		40	ns
Setup Time:							
t <sub>S1</sub>	UD clock setup time	UD	↓MCLK	UIC = Low	15		ns
t <sub>S2</sub>	UD setup time	UD	↑UIC	MCLK = High	25		ns
t <sub>S3</sub>	User input control setup time	↓UIC	↓MCLK		25		ns
t <sub>S4</sub>	IV data setup time	IV	↓MCLK	WC = UIC = High; ME = Low	15		ns
t <sub>S5</sub> <sup>4</sup>	IV master enable setup time	↓ME	↓MCLK	WC = UIC = High	20		ns
t <sub>S6</sub>	IV write control setup time	↑WC	↓MCLK	ME = Low; UIC = High	40		ns
Hold Times:							
t <sub>H1</sub>	UD clock hold time	↓MCLK	UD	UIC = Low	20		ns
t <sub>H2</sub>	UD control hold time	↑UIC	UD	MCLK = High	10		ns
t <sub>H3</sub>	User input control hold time	↓MCLK	↑UIC		0		ns
t <sub>H4</sub>	IV data hold time	↓MCLK	IV	WC = UIC = High; ME = Low	25°C	5	ns
					Temp.	20	ns
t <sub>H5</sub> <sup>4</sup>	IV master enable hold time	↓MCLK	↓ME	WE = UIC = High	0		ns
t <sub>H6</sub>	IV write control hold time	↓MCLK	↓WC	ME = Low; UIC = High	0		ns

**NOTES:**

1. The input current includes the 3-State leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.
3. These parameters are measured with a capacitive loading of 50pF and represent the output driver turn-off time.
4. If ME is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.

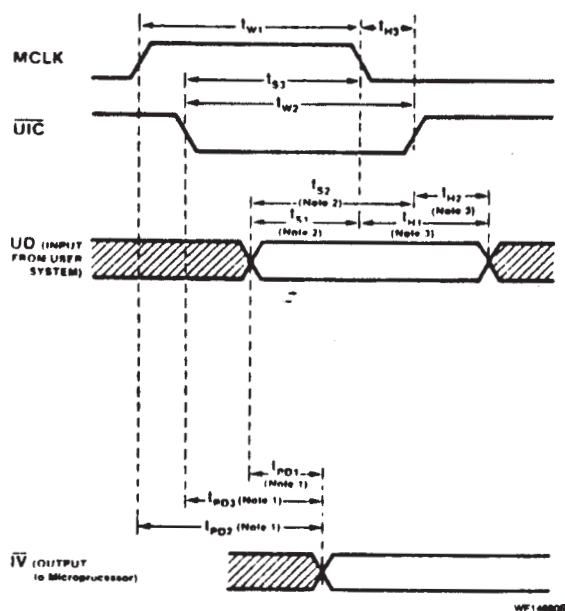


**AC ELECTRICAL CHARACTERISTICS**  $4.75 \leq V_{CC} \leq 5.25V$ ,  $0^{\circ}C \leq T_A \leq 70^{\circ}C$ 

SYMBOL	PARAMETER	REFERENCES		TEST CONDITIONS	LIMITS			UNIT
		From	To		Min	Typ	Max	
Pulse Widths								
t <sub>W1</sub>	Clock high	↑ MCLK	↓ MCLK		35			ns
t <sub>W2</sub>	User input control	↓ $\overline{UIC}$	↑ $\overline{UIC}$	MCLK = High	35			ns
Propagation Delays								
t <sub>PD1</sub>	UD propagation delay	UD	$\overline{IV}$	MCLK = High $\overline{RC} = \overline{WC} = \overline{ME} = \overline{UIC} = \text{Low}$			30	ns
t <sub>PD2</sub>	UD clock delay	↑ MCLK	$\overline{IV}$	UD = Stable; $\overline{RC} = \overline{WC} = \overline{ME} = \overline{UIC} = \text{Low}$			50	ns
t <sub>PD3</sub>	UD input delay	↓ $\overline{UIC}$	$\overline{IV}$	UD = Stable; MCLK = High $\overline{RC} = \overline{WC} = \overline{ME} = \text{Low}$			50	ns
t <sub>PD4</sub>	$\overline{IV}$ data propagation delay	$\overline{IV}$	UD	MCLK = WC = $\overline{UIC}$ = High; $\overline{ME} = \overline{UOC} = \overline{RC} = \text{Low}$			45	ns
t <sub>PD5</sub>	$\overline{IV}$ data clock delay	↑ MCLK	UD	WC = $\overline{UIC}$ = High; $\overline{IV}$ = Stable $\overline{ME} = \overline{UOC} = \overline{RC} = \text{Low}$			55	ns
Output Enable Timing								
t <sub>OE1</sub>	UD output enable	↓ $\overline{UOC}$	UD	$\overline{UIC}$ = High			30	ns
t <sub>OE2</sub>	UD input recovery	↑ $\overline{UIC}$	UD	$\overline{UOC}$ = Low			30	ns
t <sub>OE3</sub>	$\overline{IV}$ data master enable	↓ $\overline{ME}$	$\overline{IV}$	WC = $\overline{RC}$ = Low			22	ns
t <sub>OE4</sub>	$\overline{IV}$ data read enable	↓ $\overline{RC}$	$\overline{IV}$	WC = $\overline{ME}$ = Low			25	ns
t <sub>OE5</sub>	$\overline{IV}$ data write recovery	↓ WC	$\overline{IV}$	$\overline{RC} = \overline{ME}$ = Low			25	ns
Output Disable Timing								
t <sub>OD1</sub>	UD output disable	↑ $\overline{UOC}$	UD	$\overline{UIC}$ = High			25	ns
t <sub>OD2</sub>	UD input override	↓ $\overline{UIC}$	UD	$\overline{UOC}$ = Low			30	ns
t <sub>OD3</sub> <sup>1</sup>	$\overline{IV}$ data master disable	↑ $\overline{ME}$	$\overline{IV}$	WC = $\overline{RC}$ = Low			20	ns
t <sub>OD4</sub> <sup>1</sup>	$\overline{IV}$ data read disable	↑ $\overline{RC}$	$\overline{IV}$	WC = $\overline{ME}$ = Low			20	ns
t <sub>OD5</sub> <sup>1</sup>	$\overline{IV}$ data write override	↑ WC	$\overline{IV}$	$\overline{RC} = \overline{ME}$ = Low			20	ns
Setup Time								
t <sub>S1</sub>	UD clock setup time	UD	↓ MCLK	$\overline{UIC}$ = Low	15			ns
t <sub>S2</sub>	UD setup time	UD	↑ $\overline{UIC}$	MCLK = High	15			ns
t <sub>S3</sub>	User input control setup time	↓ $\overline{UIC}$	↓ MCLK		25			ns
t <sub>S4</sub>	$\overline{IV}$ data setup time	$\overline{IV}$	↓ MCLK	WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low	35			ns
t <sub>S5</sub> <sup>2</sup>	$\overline{IV}$ master enable setup time	↓ $\overline{ME}$	↓ MCLK	WC = $\overline{UIC}$ = High	30			ns
t <sub>S6</sub>	$\overline{IV}$ write control setup time	↑ WC	↓ MCLK	$\overline{ME}$ = Low; $\overline{UIC}$ = High	30			ns
Hold Times								
t <sub>H1</sub>	UD clock hold time	↓ MCLK	UD	$\overline{UIC}$ = Low	15			ns
t <sub>H2</sub>	UD control hold time	↑ $\overline{UIC}$	UD	MCLK = High	15			ns
t <sub>H3</sub>	User input control hold time	↓ MCLK	↑ $\overline{UIC}$		0			ns
t <sub>H4</sub>	$\overline{IV}$ data hold time	↓ MCLK	$\overline{IV}$	WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low	5			ns
t <sub>H5</sub> <sup>2</sup>	$\overline{IV}$ master enable hold time	↓ MCLK	↑ $\overline{ME}$	WC = $\overline{UIC}$ = High	0			ns
t <sub>H6</sub>	$\overline{IV}$ write control hold time	↓ MCLK	↓ WC	$\overline{ME}$ = Low; $\overline{UIC}$ = High	0			ns

**NOTES:**

- These parameters are measured with a capacitive loading of 50pf and represent the output driver turn-off time.
- If  $\overline{ME}$  is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.





STATIC CONDITIONS:  
SC = WC = ME = Low; UOC = High

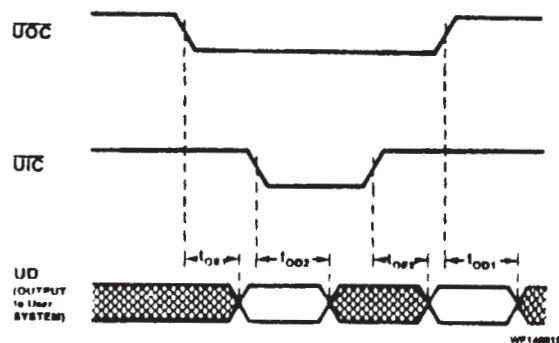
**NOTES:**

1. The actual time for stable data on the  $\overline{V}$  bus is the latest propagation from  $t_{PD1}$ ,  $t_{PD2}$ ,  $t_{PD3}$ , and  $t_{PD4}$ .
2. The  $\overline{V}$  input must satisfy the setup-time requirements for both  $I_{S1}$  and  $I_{S2}$ .
3. Minimum hold-time required for the  $\overline{V}$  input is the earlier of the times specified by  $t_{H1}$  and  $t_{H2}$ .

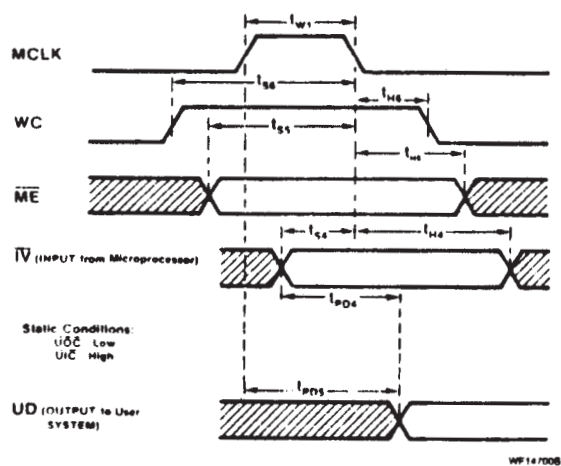
**Legend:**

 = 3-STATE

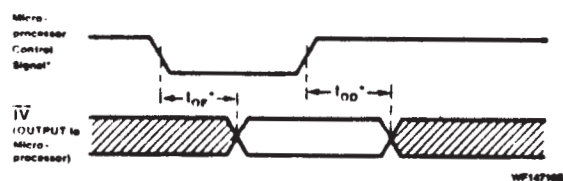
 = CHANGING DATA



#### a. User Data Input Timing



### b. User Data Output Timing



**\*PARAMETER KEY**

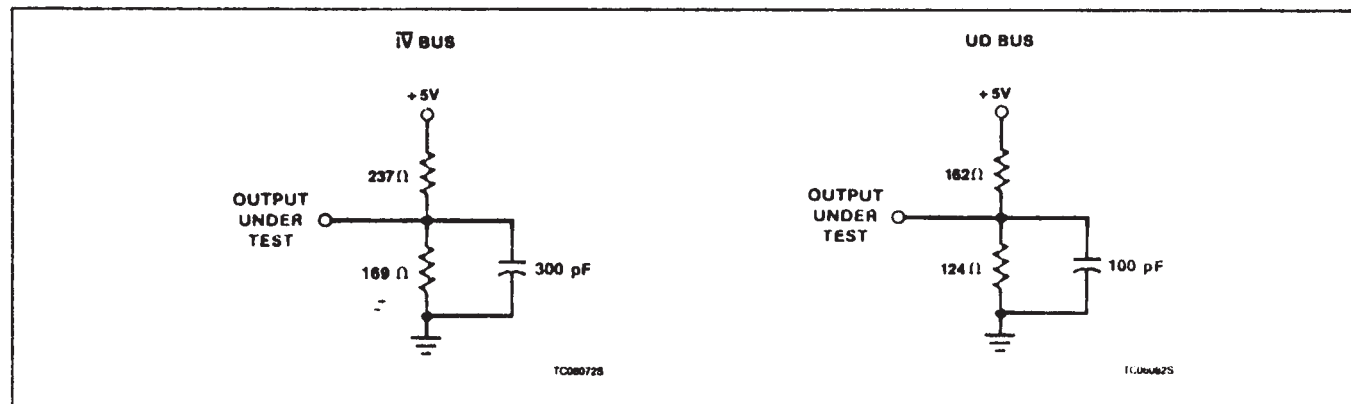
MICROPROCESSOR CONTROL SIGNAL	AC TIMING PARAMETERS	STATIC CONDITIONS
ME	tOE3 tOD3	SC = WC = Low
AC	tOE4 tOD4	SC = ME = Low
SC	tOE5 tOD5	AC = ME = Low

### c. Microcontroller Write Cycle Timing

#### d. Microcontroller Select Cycle Timing

### Figure 2. Timing Diagram

## AC TEST LOADING CIRCUITS



## APPLICATIONS

In some applications, performance of a Microcontroller system can be enhanced by using the 8X371 I/O Port instead of an addressable 8X372 port. Using a technique referred to as Extended Microcode or Fast TV Select, the address select cycles which normally precede a read or write operation when using an 8X372 can be eliminated by use of the 8X371.

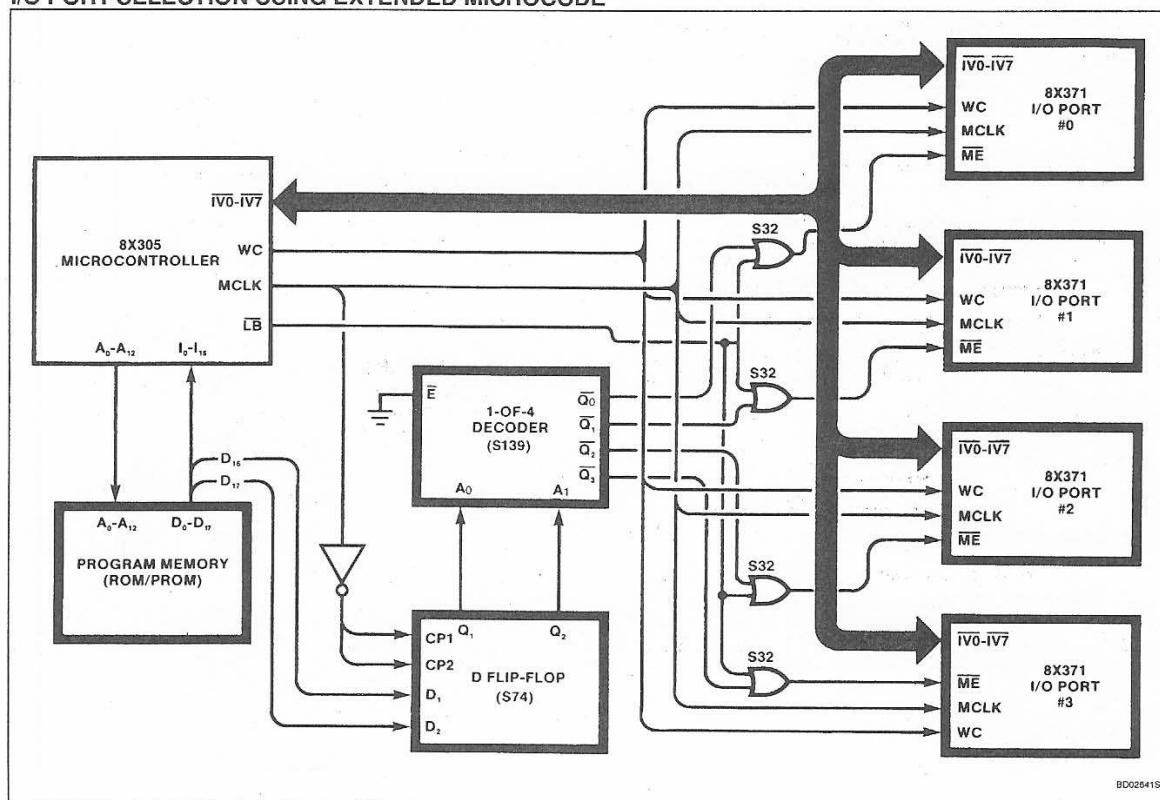
This technique is often used in bit slice microprocessor designs and involves widening the

program memory beyond the normal 16-bit requirement of the Microcontroller. the extra bits are used as enable signals for the 8X371 ports. Thus, the 8X371 is enabled during the instruction cycle in which it is required for input/output operations. Since the software overhead of separate address select cycles is eliminated, the overall system performance is improved.

As shown in the accompanying diagram, the program memory is extended by two bit

positions ( $D_{16}$  and  $D_{17}$ ), permitting any one of four 8X371 ports to be enabled during those instructions. Because of timing considerations, latches must be used to hold the Extended Microcode through the end of the instruction cycle. A decoder is used to obtain four enable signals from the two extra bits. The decoder outputs are ORed with the  $\overline{LB}$  output of the 8X305; thus, all four I/O ports are placed on the Left Bank of the TV bus.

## I/O PORT SELECTION USING EXTENDED MICROCODE



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