

Legacy Device: *Signetics S8270, S8271*

DESCRIPTION

The 8270 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

The internal design uses level sensitive binaries which respond to the negative-going clock transition. A buffer clock driver has been included to minimize input clock loading.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control. The truth table for the control modes is shown below.

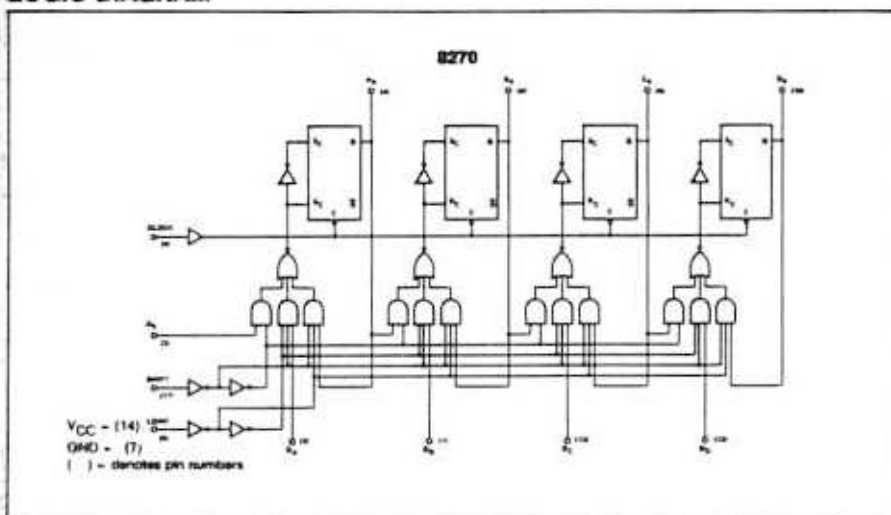
For applications not requiring the hold mode, the load input may be tied high and the shift input used as the mode control.

The 8271 provides a direct reset (R_D), and a $\overline{D}_{out}$ line in addition to the available outputs of the 8270 element. The fan-out specification for this output is the same as the true outputs of the 8270 element.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+75^{\circ}C$		$V_{CC}=5V \pm 5\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	Fig.A	N8270N	• N82S70N	
	Fig.C	N8271N	• N82S71N	
Ceramic DIP	Fig.A	N8270F	• N82S70F	S8270F
	Fig.C	N8271F	• N82S71F	S8271F
Flatpak	Fig.B Fig.A			S8270W S8271W

LOGIC DIAGRAM



PIN CONFIGURATIONS

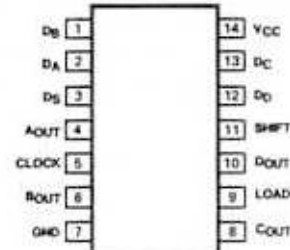


Figure A

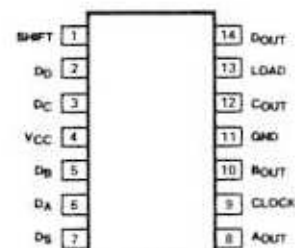


Figure B

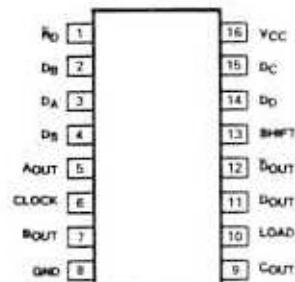


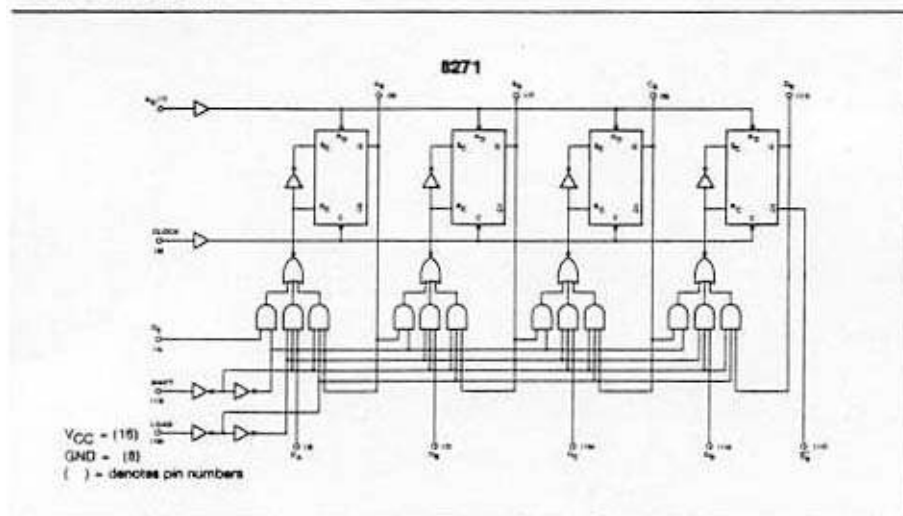
Figure C

MODE SELECT— FUNCTION TABLE

CONTROL STATE	LOAD	SHIFT
Hold	L	L
Parallel Entry	H	L
Shift Right	L	H
Shift Right	H	H

H = HIGH voltage level
L = LOW voltage level

LOGIC DIAGRAM

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	8270		8271		UNIT
		Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -800μA		2.6		V
V _{OL}	Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 11.2mA			0.4	V
I _{IH}	Input HIGH current Reset 8271 only	V _{CC} = 5.25V, V _{IN} = 4.5V			40	μA
I _{IL}	Input LOW current	V _{CC} = 5.25V, V _{IN} = 0.4V			-1.2	mA
V _{BD}	Voltage breakdown	V _{CC} = 5.25V, I _{IN} = 10mA		5.5		V
I _{CC}	Supply current	V _{CC} = 5.25V		47	65	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	82S70		82S71		UNIT
		Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = 1.0mA		2.7		V
V _{OL}	Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 20mA			0.5	V
I _{IH}	Input HIGH current Reset 82S71 only	V _{CC} = 5.25V			10	μA
I _{IL}	Input LOW current Load, Data, Clock inputs Shift, Reset(82S71 only)	V _{CC} = 5.25V, V _{IN} = 0.5V			-400 -800	μA
V _{BD}	Voltage breakdown	V _{CC} = 4.75V, I _{IN} = 1mA		5.5		V
V _{CD}	Input clamp voltage	V _{CC} = 4.75, I _{IN} = -18mA			-1.2	V
I _{CC}	Supply current	V _{CC} = 5.25V		90	90	mA

Note

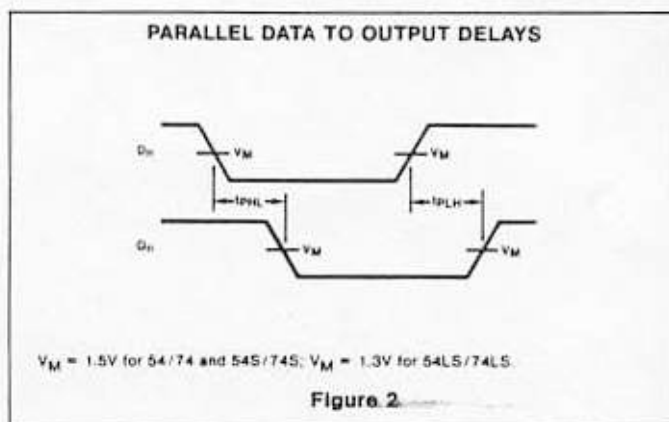
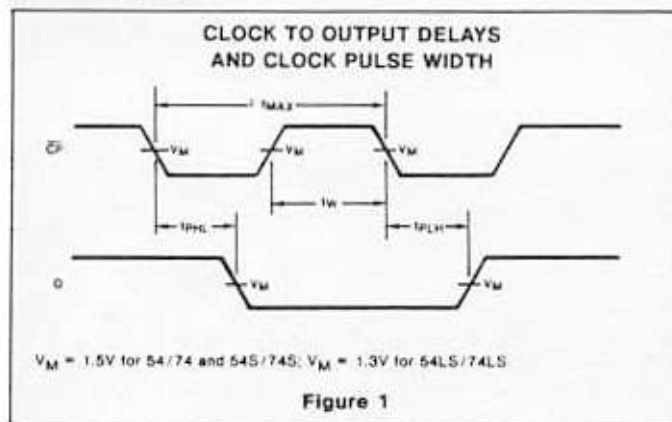
3. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

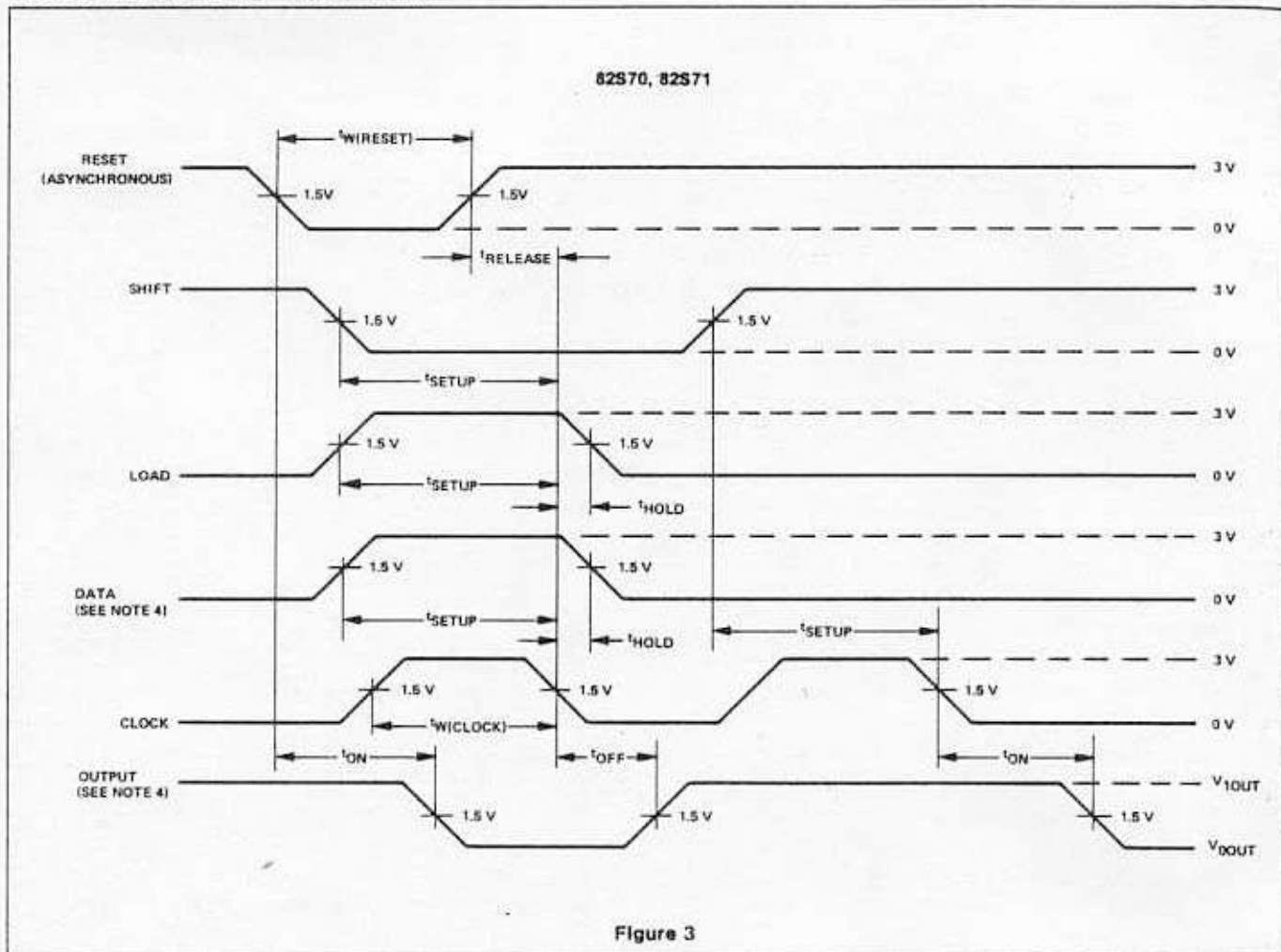
PARAMETER	TEST CONDITIONS	8270/71		82S70/S71		UNIT
		$C_L = 21\text{pF}$ $R_1 = \infty\Omega$ $R_2 = 127\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Figure 1	15		40		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Figure 1		40 40		20 20	ns ns
t_{PLH} Propagation delay t_{PHL} Reset to output	Figure 2		40 40		16 16	ns ns

AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8270/71		82S70/S71		UNIT
		Min	Max	Min	Max	
t_W Clock pulse width	Figure 1	20		8.0		ns
t_W Reset pulse width	Figure 2	30		9.0		ns
t_s Set-up time Data to clock	Figure 3	30		3.0		ns
t_h Hold time Data to clock	Figure 3	0		2.0		ns
t_s Set-up time Load or Shift to clock	Figure 3	15		6.0		ns
t_h Hold time Load or Shift to clock	Figure 3	0		0		ns
t_{rec} Recovery time MR to clock	Figure 3	30		10		ns

AC WAVEFORMS

AC TEST FIGURE AND WAVEFORMS



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