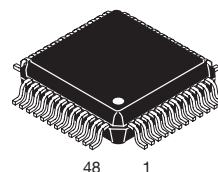


LOW POWER INTEGRATED RECEIVER FOR ISM BAND APPLICATIONS
SEMICONDUCTOR TECHNICAL DATA

Legacy Device: Motorola MC13145

The ML13145 is a dual conversion integrated RF receiver intended for ISM band applications. It features a Low Noise Amplifier (LNA), two 50 Ω linear Mixers with linearity control, Voltage Controlled Oscillator (VCO), second LO amplifier, divide by 64/65 dual modulus Prescaler, split IF Amplifier and Limiter, RSSI output, Coilless FM/FSK Demodulator and power down control. Together with the transmit chip (ML13146) and the baseband chip (MC33410 or MC33411A/B), a complete 900 MHz cordless phone system can be implemented. This device may be used in applications up to 1.8 GHz, and operating temperature $T_A = -20^\circ$ to $+70^\circ\text{C}$.

- Low (<1.8 dB @ 900 MHz) Noise Figure LNA with 14 dB Gain
- Externally Programmable Mixer linearity: IIP3 = 10(nom.) to 17 dBm (Mixer1); IIP3 = 10 (nom.) to 17 dBm (Mixer2)
- 50 Ω Mixer Input Impedance and Open Collector Output (Mixer 1 and Mixer 2); 50 Ω Second LO (LO2) Input Impedance
- Low Power 64/65 Dual Modulus Prescaler (ML12054A type)
- Split IF for Improved Filtering and Extended RSSI Range
- Internal 330 Ω Terminations for 10.7 MHz Filters
- Linear Coilless FM/FSK Demodulator with Externally Programmable Bandwidth, Center Frequency and Audio level
- 2.7 to 6.5 V Operation, Low Current Drain (<27 mA, Typ @ 3.6 V) with Power Down Mode (<10 μA , Typ)
- 2.4 GHz RF, 1.0 GHz IF1 and 50 MHz IF2 Bandwidth



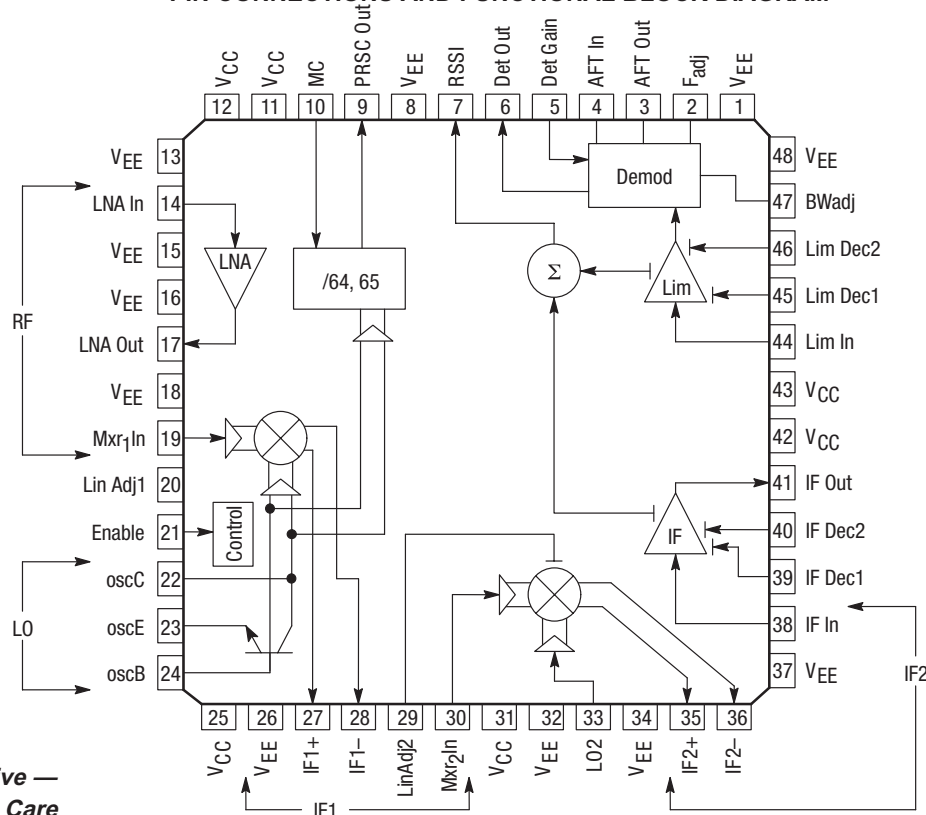
LQFP 48 = -9P
PLASTIC PACKAGE
CASE 932

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
LQFP 48	MC13145FTA	ML13145-9P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



**ESD Sensitive —
Handle with Care**

This device contains
626 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	7.0	Vdc
Junction Temperature	$T_J(max)$	150	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C
Maximum Input Signal	P_{in}	5.0	dBm

NOTES: 1. Meets Human Body Model (HBM) ≤ 250 V and Machine Model (MM) ≤ 25 V.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage ($T_A = 25^\circ\text{C}$)	V_{CC} V_{EE}	2.7 0	– 0	6.5 0	Vdc
Input Frequency (LNA In, Mxr ₁ In)	f_{in}	100	–	1800	MHz
Ambient Temperature Range	T_A	-20	–	70	°C
Input Signal Level (with minor performance degradation)	P_{in}	–	-10	–	dBm

RECEIVER DC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_{CC} = 3.6$ Vdc; No Input Signal, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Total Supply Current (Enable = V_{CC})	I_{total}	24	27	34	mA
Power Down Current (Enable = V_{EE})	I_{total}	–	10	50	μA

RECEIVER AC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_{CC} = 3.6$ Vdc; RF In = 1.0 GHz; 1st LO Freq = 1070.7 MHz; 2nd LO Freq = 60 MHz; $f_{mod} = 1.0$ kHz; $f_{dev} = \pm 40$ kHz; IF filter bandwidth = 280 kHz, unless otherwise noted. See Figure 1 Test Circuit)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
SINAD @ -110 dBm LNA Input	LNA In	Det Out	SINAD	12	20	–	dB
12 dB SINAD Sensitivity (Apps Circuit with C-message filter at DetOut)	LNA In	Det Out	SINAD _{12dB}	–	-115	–	dBm
30 dB SINAD Sensitivity (No IF filter distortion within ± 40 kHz)	LNA In	Det Out	SINAD _{30dB}	–	-100	–	dBm
SINAD Variation with IF Offset of ± 40 kHz (No IF filter distortion within ± 40 kHz)	LNA In	Det Out	–	–	5.0	–	dB
Noise Figure: LNA, 1st Mixer & 2nd Mixer	LNA In	IF Out	NF	–	3.5	5.0	dB
Power Gain: LNA, 1st Mixer & 2nd Mixer	LNA In	IF Out	G	15	19	25	dB
RSSI Dynamic Range	IF In	RSSI	–	–	80	–	dB
RSSI Current	IF In	RSSI	–				μA
–10 dBm @ IF Input				35	40	55	
–20 dBm @ IF Input				–	35	–	
–30 dBm @ IF Input				–	30	–	
–40 dBm @ IF Input				–	25	–	
–50 dBm @ IF Input				15	20	37	
–60 dBm @ IF Input				–	15	–	
–70 dBm @ IF Input				–	10	–	
–80 dBm @ IF Input				–	5.0	–	
–90 dBm @ IF Input				–	1.0	7.0	
Input 1.0 dB Compression Point (Measured at IF output)			P_{in1dB}	–	-18	–	dBm
Input 3rd Order Intercept Point (Measured at IF output)			IIP3	–	-8.0	–	dBm
Demodulator Output Swing (50 k Ω 56 pF Load)	IF In	Det Out	V_{out}	0.8	1.0	1.2	V_{pp}

RECEIVER AC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_{CC} = 3.6\text{ Vdc}$; RF In = 1.0 GHz; 1st LO Freq = 1070.7 MHz; 2nd LO Freq = 60 MHz; $f_{\text{mod}} = 1.0\text{ kHz}$; $f_{\text{dev}} = \pm 40\text{ kHz}$; IF filter bandwidth = 280 kHz, unless otherwise noted. See Figure 1 Test Circuit)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Demodulator Bandwidth ($\pm 1.0\text{ dB}$ bandwidth)		Det Out	BW	–	100	–	kHz
Prescaler Output Level (10 k Ω /8.0 pF load) Prescaler 64 Frequency = 16.72968 MHz Prescaler 65 Frequency = 16.4723 MHz		PRSC _{out}	V _{out}	0.4 0.4	0.51 0.51	0.6 0.6	V _{pp}
MC Current Input (High)		MC	I _{ih}	70	100	130	μA
MC Current Input (Low)		MC	I _{il}	–130	–100	–70	μA
Input high voltage		Enable	V _{ih}	V _{CC} – 0.4	–	V _{CC}	V
Input low voltage		Enable	V _{il}	0	–	0.4	V
Input Current		Enable	I _{in}	–50	–	50	μA
PLL Setup Time [Note 1]	MC	PRSC _{out}	T _{PLL}	–	10	–	nS
SNR @ –30 dBm Signal Input (<40 kHz deviation;with C–Message Filter)				–	50	–	dB
Total Harmonic Distortion (<40 kHz deviation;with C–Message Filter)				–	1.0	–	%
Spurious Response SINAD (RF In: –50 dBm)				–	12	–	dB

*CF1 & CF2 = 280 kHz, 6.0 dB BW, 10.7 MHz Ceramic Filter
 **T1 = Toko Part # 600ENAS-A998EK

General

The ML13145 is a low power dual conversion wideband FM receiver incorporating a split IF. This device is designated for use as the receiver in analog and digital FM systems such as 900 Mhz ISM Band Cordless phones and wideband data links with data rates up to 150kbps. It contains a 1st and 2nd mixer, 1st and 2nd local oscillator, Received Signal Strength Indicator (RSSI), IF amplifier, limiting IF, a unique coilless quadrature detector, and a device enable function.

Current Regulation/Enable

The ML13145 is designed for battery powered portable applications. Supply current is typically 27 mA at 3.6 Vdc. Temperature compensating, voltage independent current regulators are controlled by the Enable Pin where "high" powers up and "low" powers down the entire circuit.

Low Noise Amplifier (LNA)

The LNA is a cascoded common emitter amplifier configuration. Under very large RF input signals, the DC base current of the common emitter and cascode transistors can become very significant. To maintain linear operation of the LNA, adequate dc current source is needed to establish the $2V_{be}$ reference at the base of the RF cascoded transistor and to provide the base voltage on the common emitter transistor. A sensing circuit, together with a current mirror guarantees that there is always sufficient DC base current available for the cascode transistor under all power levels.

1st and 2nd Mixer

Each mixer is a double-balanced class AB four quadrant multiplier which may be externally biased for high mixer dynamic range. Mixer input third order intercept point of up to 17 dBm is achieved with only 7.0 mA of additional supply current. The 1st mixer has a single-ended input at 50 Ω and operates at 1.0 GHz with -3.0 dB of power gain at approximately 100 mVrms LO drive level. The mixers have open collector differential outputs to provide excellent mixer dynamic range and linearity.

1st Local Oscillator

The 1st LO has an on-chip transistor which operates with coaxial transmission line and LC resonant elements up to 1.8 GHz. A VCO output is available for multi-frequency operation under PLL synthesizer control.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output (Pin 7) is derived by summing the currents from the IF and limiting amplifier stages. An increase in RSSI dynamic range, particularly at higher input signal levels is achieved. The RSSI circuit is designed to provide typical-

ly 80 dB of dynamic range with temperature compensation. Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB and 330 Ω source and load impedance.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB up to 40MHz.

The fixed internal input impedance is 330 Ω . When using ceramic filters requiring source and load impedances of 330 Ω , no external matching is necessary. Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 330 Ω .

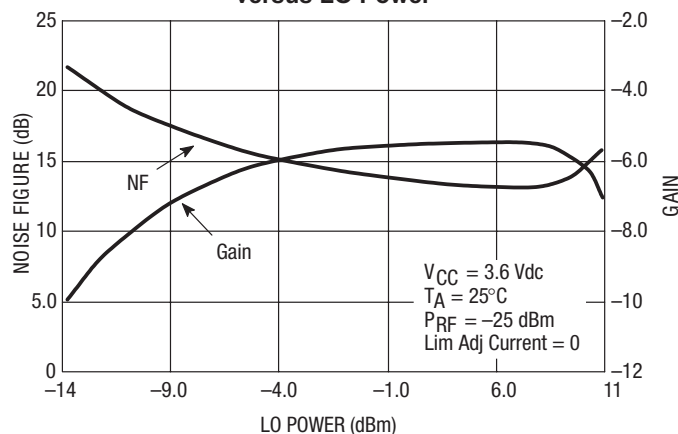
Limiter

The limiter section is similar to the IF amplifier section except that five stages are used with the middle three contributing to the RSSI. The fixed internal input impedance is 330 Ω . The total gain of the limiting amplifier section is approximately 84 dB. This IF limiting amplifier section internally drives the coilless quadrature detector section.

Coilless Quadrature Detector

The coilless detector is a unique design which eliminates the conventional tunable quadrature coil in FM receiver systems. The frequency detector implements a phase locked loop with a fully integrated on chip relaxation oscillator which is current controlled and externally adjusted, a bandwidth adjust, and an automatic frequency tuning circuit. The loop filter is external to the chip allowing the user to set the loop dynamics. Two outputs are used: one to deliver the audio signal (detector output) and the other to filter and tune the detector (AFT).

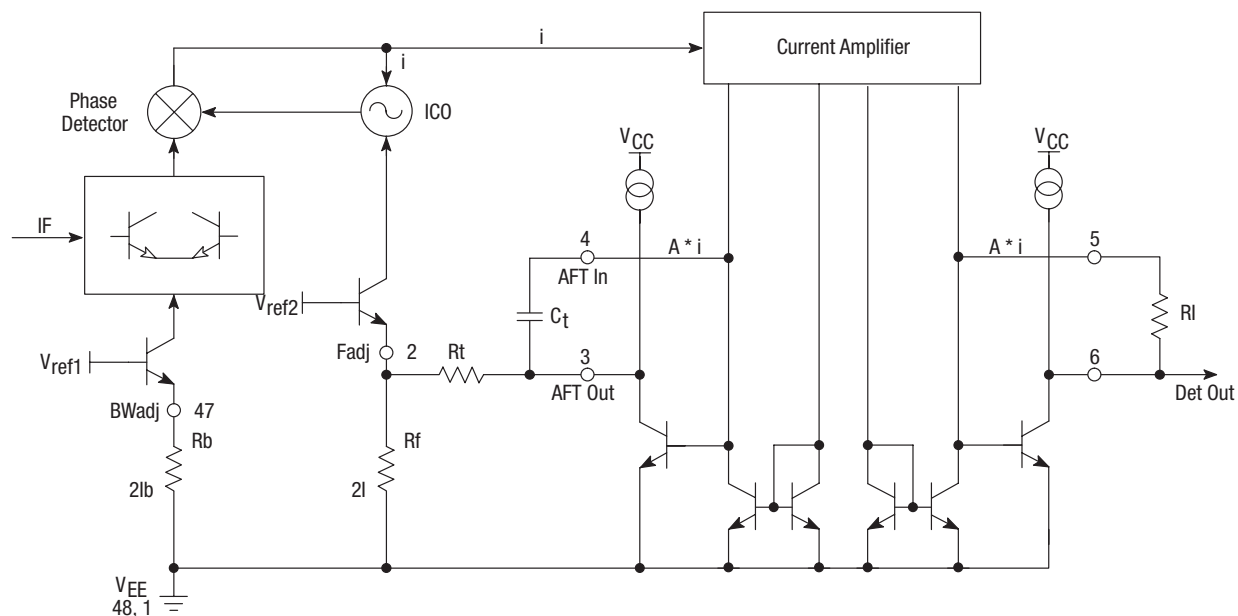
Figure 2. 2nd Mixer NF & Gain versus LO Power

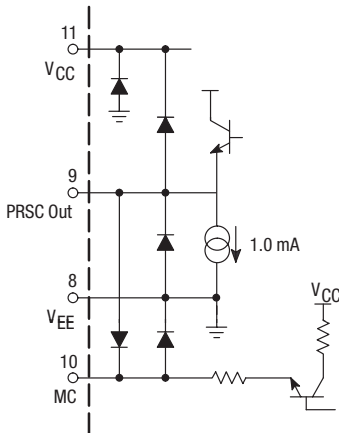
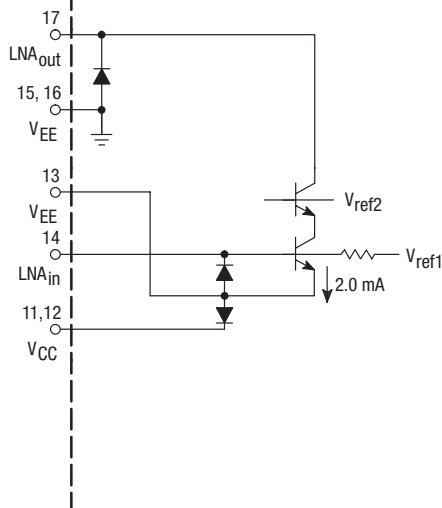
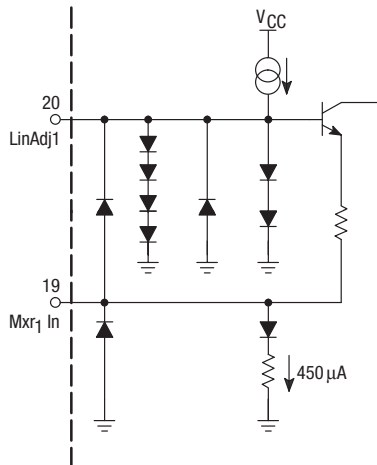


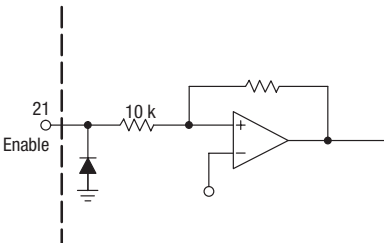
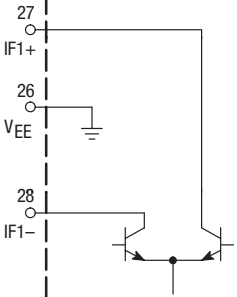
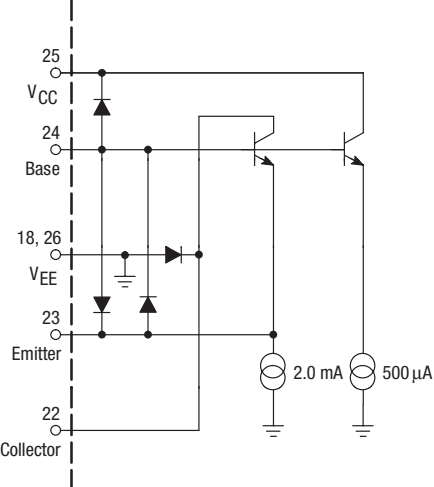
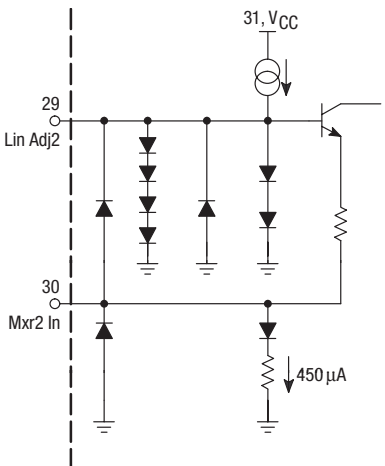
PIN FUNCTION DESCRIPTION

Pin	Symbol/Type	Description	Description
47	BWadj	See Figure 3.	COILLESS DETECTOR Bandwidth Adjust The deviation bandwidth of the detector response is determined by the combination of an on-chip capacitor and an external resistor to ground.
2	Fadj		Frequency Adjust The free running frequency of the detector oscillator is defined by the combination of an on-chip capacitor and an external resistor, Radj from frequency adjust pin to ground.
1, 48	VEE		VEE, Negative Supply These pins are VEE supply for the coilless detector circuit.
3	AFT Out		AFT Out The AFT is low pass filtered with a corner frequency below the audio bandwidth allowing the error to be added to the center frequency adjust signal at Fadj, Pin 2. The low frequency high pass corner is set by the external capacitor, Ct from AFT out (Pin 3) to AFT in (Pin 4) and external resistor, Rt from AFT out to Fadj (Pin 2).
4	AFT In		AFT In The AFT in is used to set the buffer transfer function.
5	Det Gain		Detector Gain The AFT buffer is used to set the buffer transfer function.
6	Det Out		Detector Output Set gain and output level of detector with resistor to Det Out Pin.

Figure 3. Coilless Detector Internal Circuit

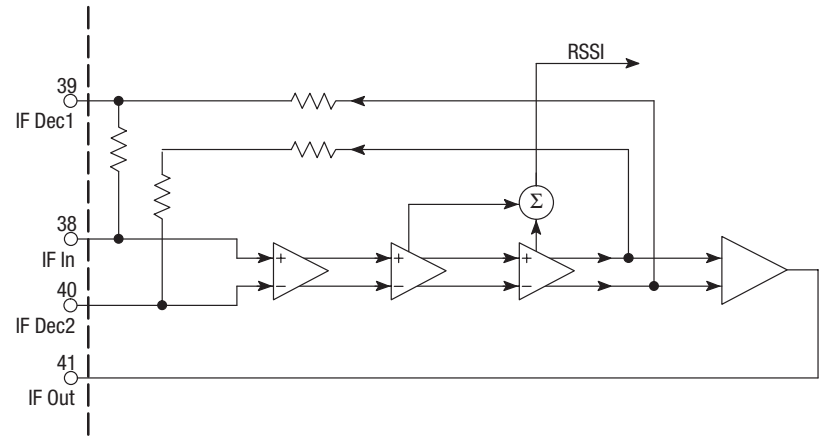


Pin	Symbol/Type	Description	Description
8	V _{EE}		V_{EE}, Negative Supply Voltage
9	PRSCout		Prescaler Output The prescaler output provides typically 500 mVpp drive to the fin pin of a PLL synthesizer. Conjugately matching the interface will increase the drive delivered to the PLL input.
10	MC		Dual Modulus Control Current Input This requires a current input of typically 200 μA _{pp} .
11, 12	V _{CC}		V_{CC}, Positive Supply V _{CC} pin is taken to the incoming positive battery or regulated dc voltage through a low impedance trace on the PCB. It decoupled to V _{EE} ground at the pin of the IC.
14	LNA In		LNA In The input is the base of the common emitter transistor. Minimum external matching is required to optimize the input return loss and gain.
13, 15, & 16	V _{EE}		V_{EE}, Negative Supply V _{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A minimum two sided PCB is recommended so that ground returns can be easily made through via holes.
17	LNAout		LNA Out The output is from the collector of the cascode transistor amplifier. The output may be conjugately matched with a shunt L (needed to dc bias the open collector), and series L and C network.
19	Mxr ₁ In		1st Mixer Input The mixer input impedance is broadband 50 Ω for applications up to 2.4 GHz. It easily interfaces with a RF ceramic filter.
20	Lin Adj1		1st Mixer Linearity Control The mixer linearity control circuit accepts approximately 0 to 300 μA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 17 dBm may be achieved at 300 μA of control current.

Pin	Symbol/Type	Description	Description
21	Enable		Enable Enable the receiver by pulling the pin up to V_{CC} .
26	V_{EE}		V_{EE}, Negative Supply V_{EE} supply for the mixer IF output.
27	IF1+		1st Mixer Outputs The Mixer is a differential open collector output configuration which is designed to use over a wide frequency range. The differential output of the mixer has back to back diodes across them to limit the output voltage swing and to prevent pulling of the VCO. Differential to single-ended circuit configuration and matching options are shown in the Test Circuit. Additional mixer gain can be achieved by matching the outputs for the desired passband Q.
28	IF1-		
22	Collector		On-board VCO Transistor The transistor has the emitter, base, collector, V_{CC} , and V_{EE} pins available. Internal biasing which is compensated for stability over temperature is provided. It is recommended that the base pin is pulled up to V_{CC} through an RFC chosen for the particular oscillator center frequency.
23	Emitter		V_{CC}, Positive Supply Voltage A V_{CC} pin is provided for the VCO. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc.
24	Base		V_{EE}, Negative Supply Voltage
25	V_{CC}		
18, 26	V_{EE}		
29	Lin Adj2		2nd Mixer Linearity Control The mixer linearity control circuit accepts approximately 0 to 400 μA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 17 dBm may be achieved at 400 μA of control current. IIP3 default with no external bias is 10 dBm.
30	Mxr2 In		2nd Mixer Input The mixer input impedance is broadband 50 Ω .
31	V_{CC}		V_{CC}, Positive Supply

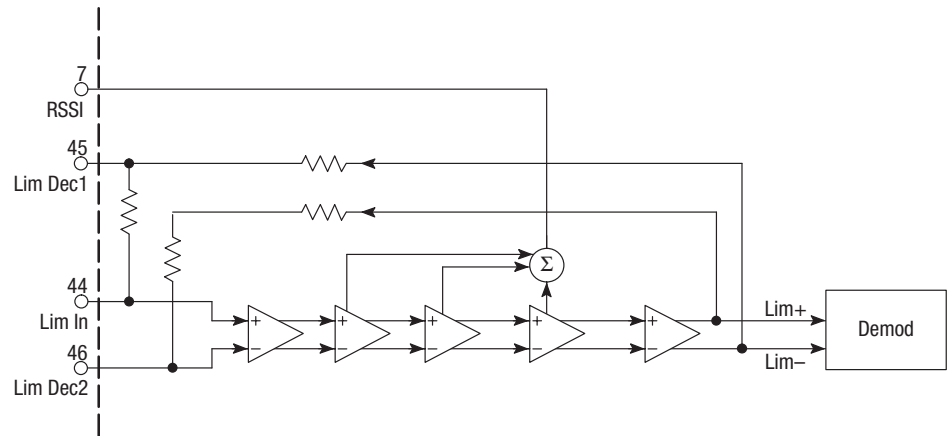
Pin	Symbol/Type	Description	Description
32, 34	V _{EE}		V_{EE}, Negative Supply Voltage
33	LO2		2nd Local Oscillator The 2nd LO input impedance is broadband 50 Ω; it is driven from an external 50 Ω source. Typical level is -15 to -10 dBm.
35	IF2+		2nd Mixer Outputs The Mixer is a differential open collector configuration.
36	IF2-		
37	V _{EE}	See Figure 4.	V_{EE}, Negative Supply Voltage
38	IF In		IF Amplifier Input IF amplifier input source impedance is 330 Ω. The three stage amplifier has 40 dB of gain with 3.0 dB bandwidth of 40 MHz.
39, 40	IF Dec1, IF Dec2		IF Decoupling These pins are decoupled to V _{CC} to provide stable operation of the limiting IF amplifier.
41	IF Out		IF Amplifier Output IF amplifier output load impedance is 330 Ω.
42	V _{CC}		V_{CC}, Positive Supply Voltage
7	RSSI		RSSI The RSSI circuitry in the 2nd & 3rd amplifier stages outputs a current when the output of the previous stage enters limiting. The net result is a RSSI current which represents the logarithm of the IF input voltage. An external resistor to ground is used to provide a voltage output.

Figure 4. IF Amplifier Functional Diagram

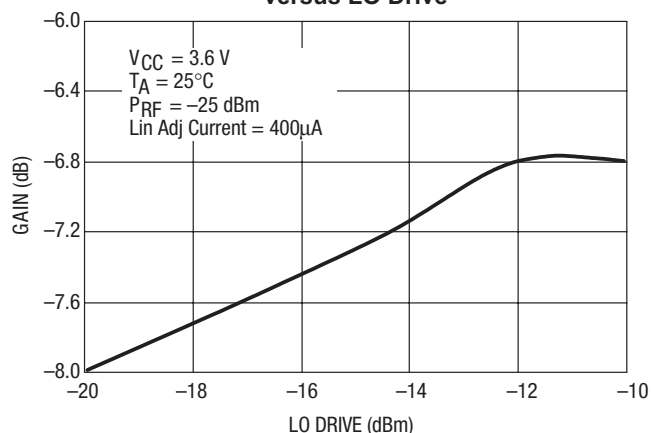


Pin	Symbol/Type	Description	Description
43	V _{CC}	See Figure 5.	V_{CC}, Positive Supply Voltage
44	Lim In		Limiting Amplifier Input Limiting amplifier input source impedance is 330 Ω. This amplifier has 84 dB of gain with 3.0 dB bandwidth of 40 MHz; this enables the IF and limiting amplifiers chain to hard limit on noise.
45, 46	Lim Dec1, Lim Dec2		If Decoupling These pins are decoupled to V _{CC} to provide stable operation of the 2nd IF limiting amplifier.
7	RSSI		RSSI The RSSI circuitry in the 2nd, 3rd, & 4th amplifier stages outputs a current when the output of the previous stage enters limiting. The net result is a RSSI current which represents the logarithm of the IF input voltage. An external resistor to ground is used to provide a voltage output.

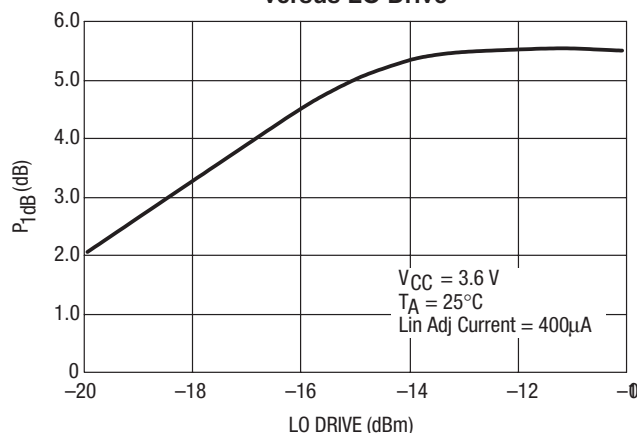
Figure 5. Limiter Amplifier Functional Diagram



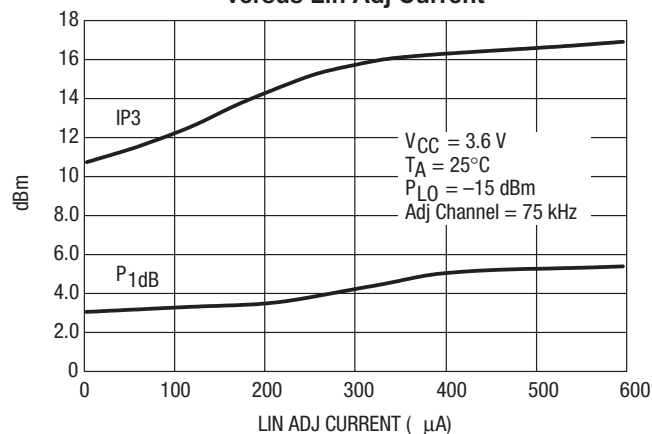
**Figure 6. 2nd Mixer Gain
versus LO Drive**



**Figure 7. 2nd Mixer P1dB
versus LO Drive**



**Figure 8. 2nd Mixer IP3/P1dB
versus Lin Adj Current**



**Figure 9. 2nd Mixer Gain
versus Lin Adj Current**

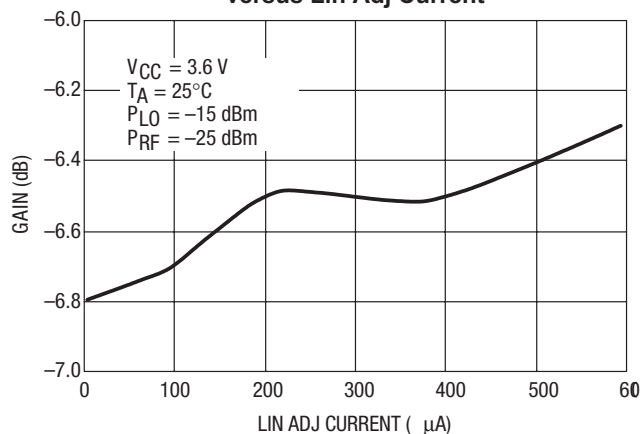


Figure 10. Test Circuit for Figures 6 thru 9.

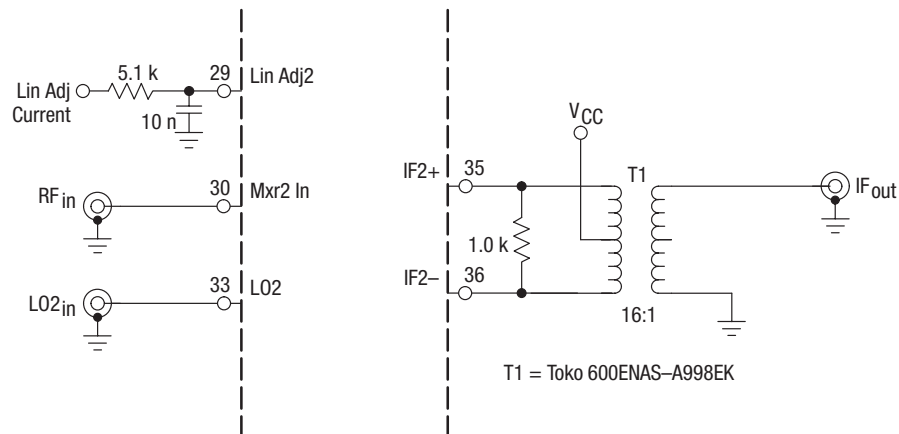


Figure 11. Fadj Current
versus IF Frequency

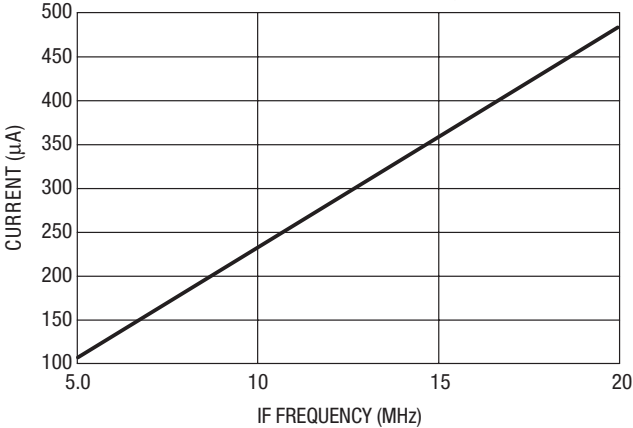


Figure 12. Fadj Resistor
versus IF Frequency

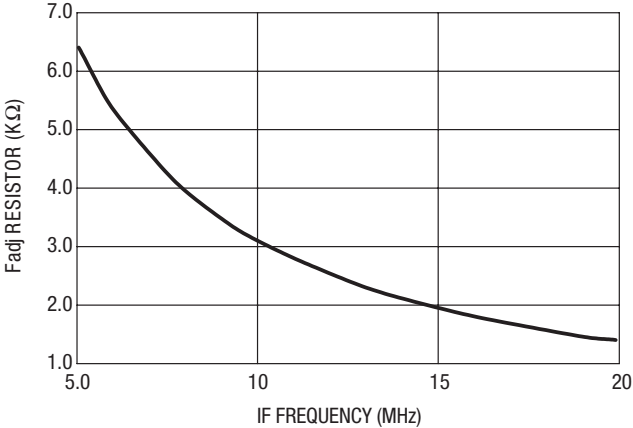


Figure 13. BWadj Resistor
versus BWadj Current

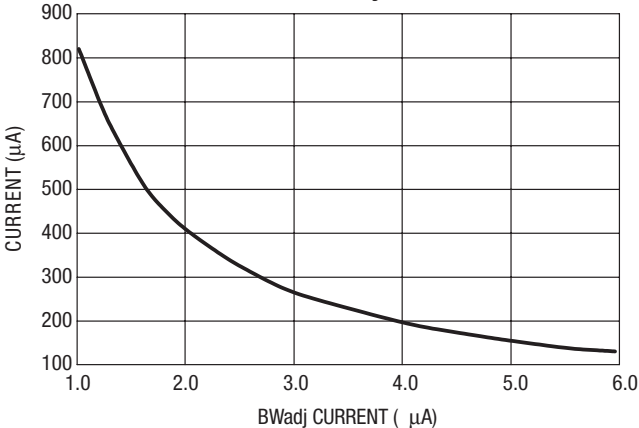


Figure 14. IF Frequency
versus BWadj Current

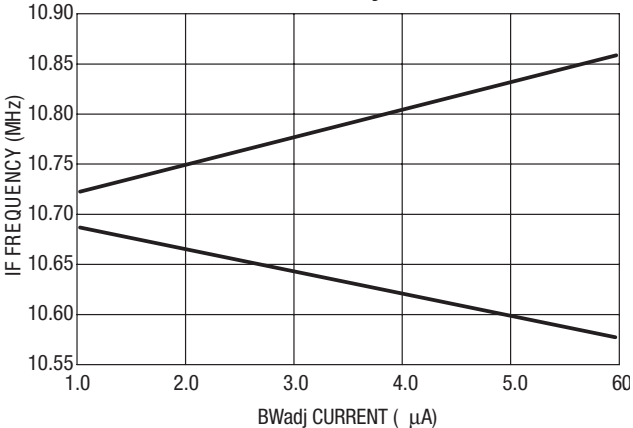


Table 1. LNA S-Parameters: 3.6 Vdc

Freq (MHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 mag	S22 Ang
25	0.84	-3.0	10.8	176	0.00005	-27	1.0	-1.2
50	0.84	-71	10.7	171	0.0004	76	1.0	-3.7
100	0.83	-15	10.3	162	0.0006	61	0.99	-4.9
150	0.81	-22	10.	154	0.0011	91	0.99	-7.3
200	0.78	-28	9.6	147	0.001	60	0.99	-9.7
300	0.73	-41	9.0	132	0.002	42	0.99	-15
400	0.66	-50	7.8	116	0.00070	22	0.95	-19
450	0.64	-54	7.4	111	0.0014	39	0.96	-21
500	0.62	-59	7.0	106	0.0009	69	0.96	-23
750	0.51	-77	5.5	80	0.0013	-51	0.94	-33
800	0.49	-80	5.2	75	0.002	-80	0.93	-36
850	0.47	-81	4.9	71	0.004	-120	0.92	-37
900	0.46	-82	4.6	67	0.0057	-130	0.92	-38
950	0.44	-82	4.3	62	0.008	-142	0.91	-40
1000	0.45	-81	3.9	58	0.014	-162	0.95	-41
1250	0.55	-94	3.5	47	0.029	140	0.099	-50
1500	0.48	-120	3.1	24	0.02	63	0.94	-65
1750	0.43	-126	2.5	6.9	0.0066	79	0.93	-74
2000	0.43	-135	2.1	-9.9	0.0099	129	0.92	-85
2250	0.45	-145	1.8	-27	0.017	133	0.91	-96
2500	0.47	-155	1.5	-43	0.021	132	0.89	-106
2750	0.51	-167	1.2	-60	0.03	130	0.88	-118
3000	0.55	-180	1.0	-78	0.039	120	0.85	-129

Figure 15. ML13145 Evaluation PCB Schematic

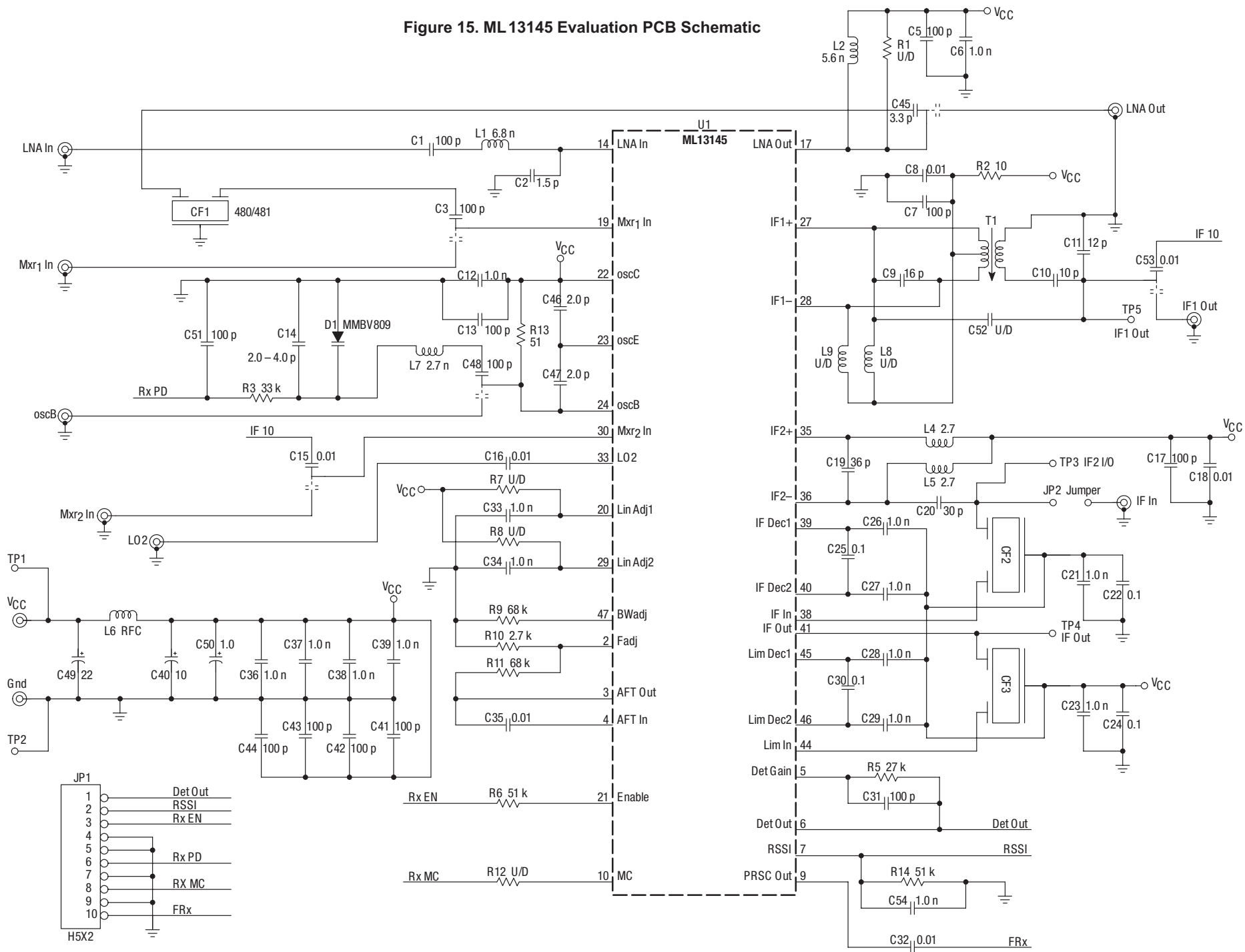
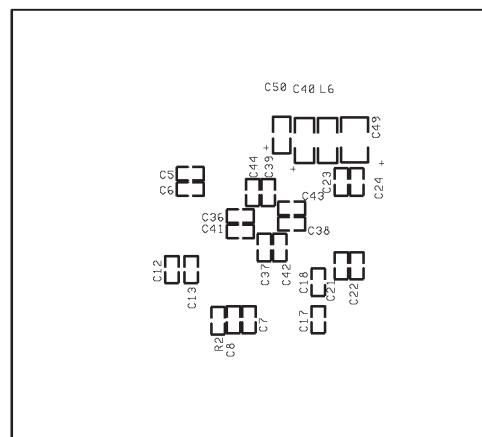
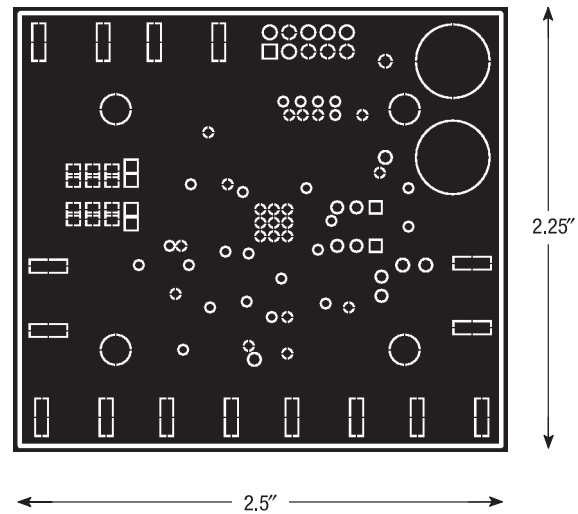
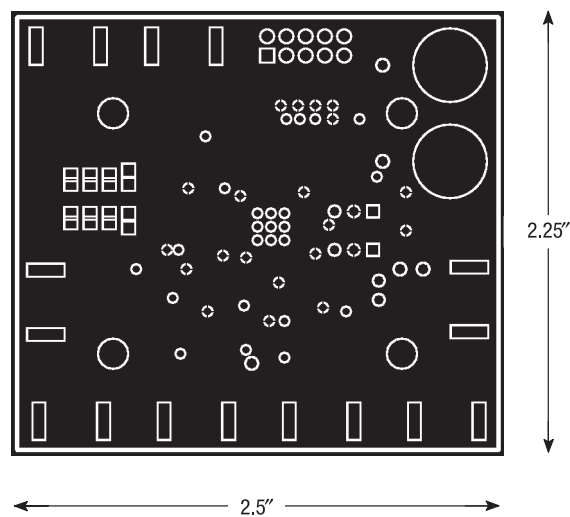


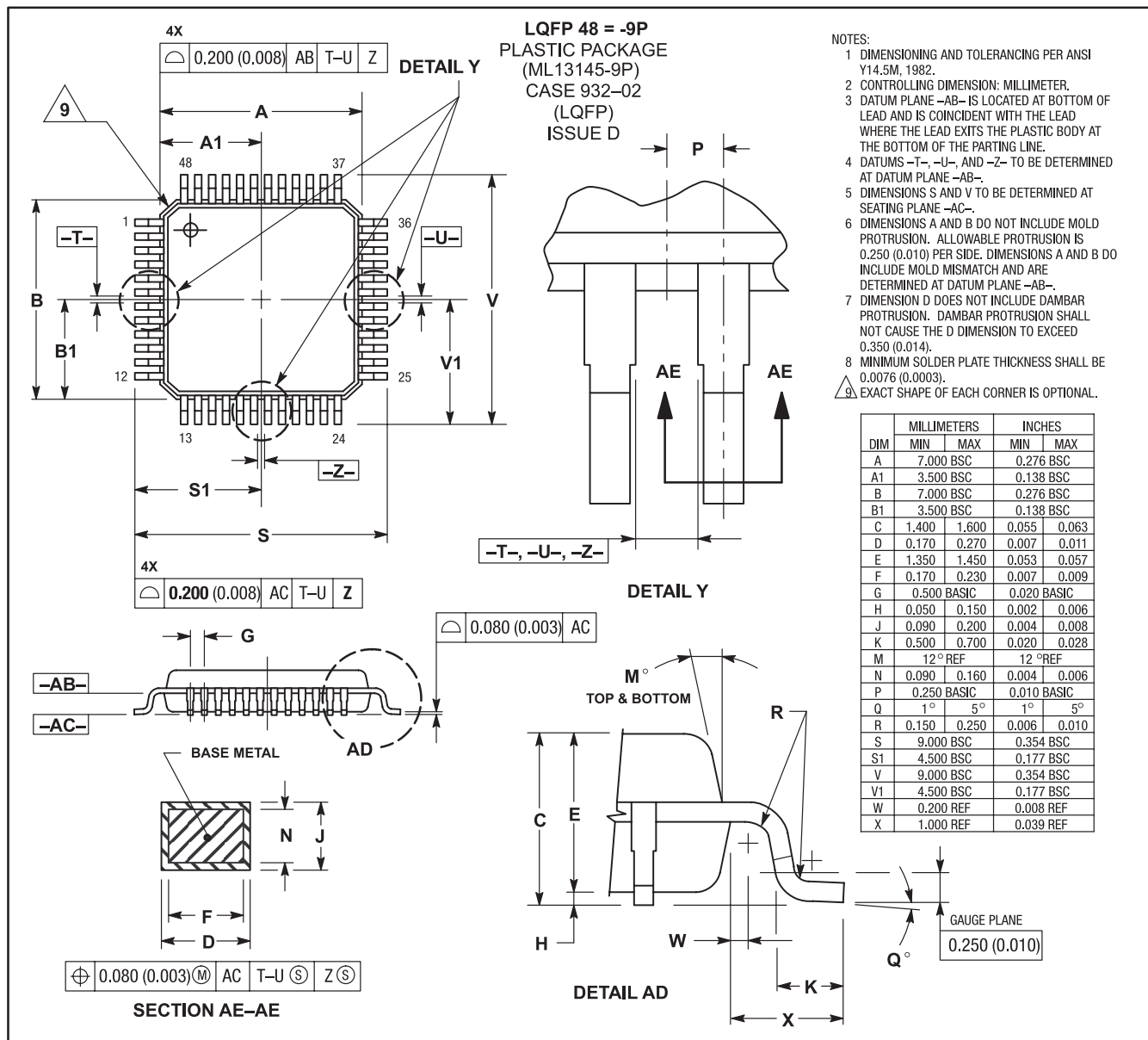
Figure 16. Evaluation PCB Component Side



CF1	480/481	C45	3.3 p
CF2,CF3	10.7M	C46, C47	2.0 p
C1, C3, C5, C7, C13, C17, C31, C41, C42, C43, C44, C48, C51	100 p	C49	22
C2	1.5 p	C50	1.0
C6, C12, C21, C23, C26, C27, C28, C29, C33, C34, C36, C37, C38, C39, C54	1.0 n	R1, R7, R8, L8, L9, R12, C52	U/D
C8, C15, C16, C18, C32, C53	0.01	L1	6.8 n
C9	16 p	L2	5.6 n
C10	10 p	L4, L5	2.7
C11	12 p	L6	RFC
C14	2.0–4.0 p	L7	2.7 n
C19	36 p	R3	33 k
C20	39 p	R5	27 k
C22, C24, C25, C30, C35	0.1	R6,R14	51 k
R2, C40	10	R11,R9	68 k
		R10	2.7 k
		R13	51
		T1	A099
		U1	ML13145

*Legacy Applications Information***Figure 18. Evaluation PCB Ground Plane****Figure 19. Evaluation PCB Power Plane**

OUTLINE DIMENSIONS



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