

#### MECL PLL COMPONENTS $\div 32/33$ , $\div 64/65$ DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

#### Legacy Device: Motorola MC12034A

The ML12034 can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series or Lansdale's ML145xxx series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- ML12034 for Positive Edge Triggered Synthesizers
- 12mA Maximum,  $-40$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 5.5$  Vdc
- Modulus Control Input is Compatible with Standard CMOS and TTL
- Low-Supply Current 8.5 mA Typical
- Operating Temperature Range  $T_A = -40$  to  $85^{\circ}\text{C}$

#### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

NOTES: 1. SW: H =  $V_{CC}$ , L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.  
2. MC: H = 2.0 V to  $V_{CC}$ , L = Gnd to 0.8 V.

Design Criteria	Value	Unit
Internal Gate Count *	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

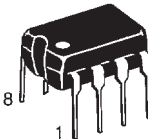
NOTE: \*Equivalent to a two-input NAND gate.

#### MAXIMUM RATINGS


Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	$V_{CC}$	$-0.5$ to $7.0$	Vdc
Operating Temperature Range	$T_A$	$-40$ to $85$	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	$-65$ to $150$	$^{\circ}\text{C}$
Modulus Control Input, Pin 6	MC	$-0.5$ to $6.5$	Vdc

NOTES: 1. ESD data available upon request.  
2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $\text{Gnd} \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

**P DIP 8 = PP**  
PLASTIC PACKAGE  
CASE 626-04



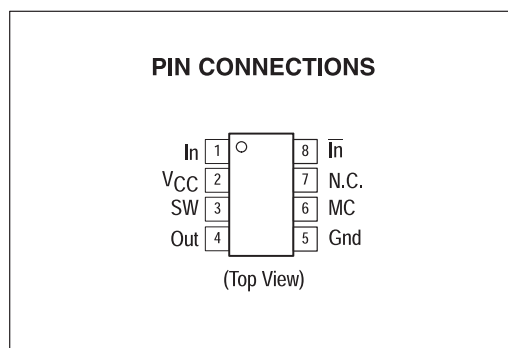
**SO 8 = -5P**  
PLASTIC PACKAGE  
CASE 751  
(SO-8)



PACKAGE	MOTOROLA	LANSDALE
P-DIP 8	MC12034AP	ML12034PP
SO 8	MC12034AD	ML12034-5P

**CROSS REFERENCE/ORDERING INFORMATION**

**Note:** Lansdale lead free (Pb) product, as it becomes available, will be identified by a part number prefix change from ML to MLE.



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5$  Vdc,  $T_A = -40$  to  $85^{\circ}\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	$f_t$	0.5	2.4	2.0	GHz
Supply Current Output Unloaded (Pin 2)	$I_{CC}$	–	8.5	12	mA
Modulus Control Input High (MC)	$V_{IH1}$	2.0	–	$V_{CC}$	V
Modulus Control Input Low (MC)	$V_{IL1}$	–	–	0.8	V
Divide Ratio Control Input High (SW)	$V_{IH2}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	Vdc
Divide Ratio Control Input Low (SW)	$V_{IL2}$	Open	Open	Open	–
Output Voltage Swing ( $C_L = 12$ pF, $R_L = 1.1$ k $\Omega$ )	$V_{out}$	1.0	1.6	–	V <sub>pp</sub>
Modulus Setup Time MC to Out	$t_{SET}$	–	8.0	10.0	ns
Input Voltage Sensitivity 500 to 2000 MHz	$V_{in}$	100	–	1500	mV <sub>pp</sub>
Output Current ( $C_L = 12$ pF, $R_L = 1.1$ k $\Omega$ )	$I_O$	–	–	3.5	mA

Figure 1. Logic Diagram

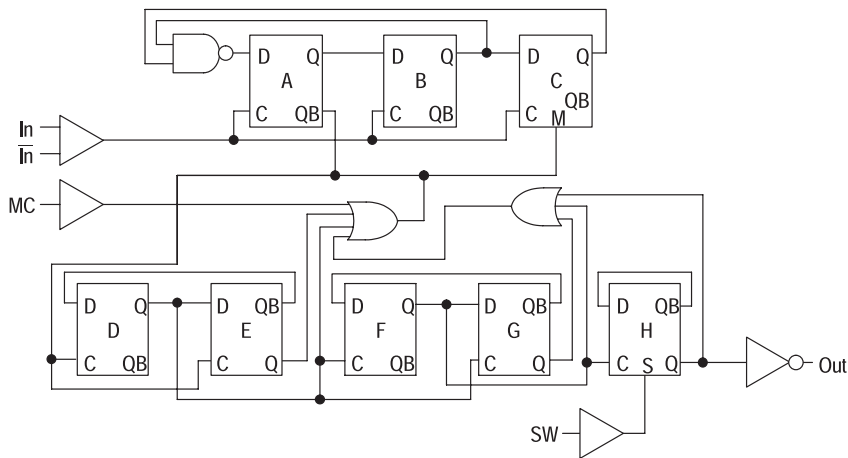


Figure 2. Modulus Setup Time

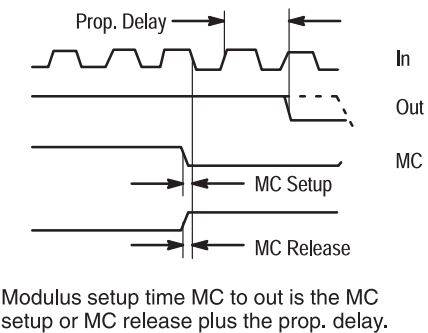


Figure 3. Typical Output Waveform

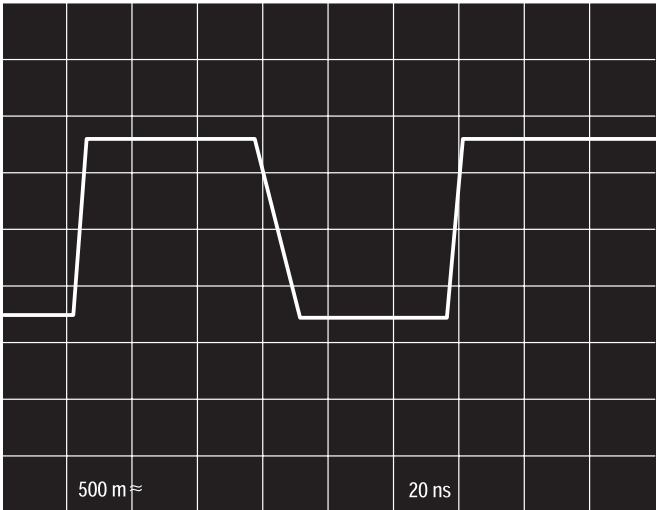


Figure 4. AC Test Circuit

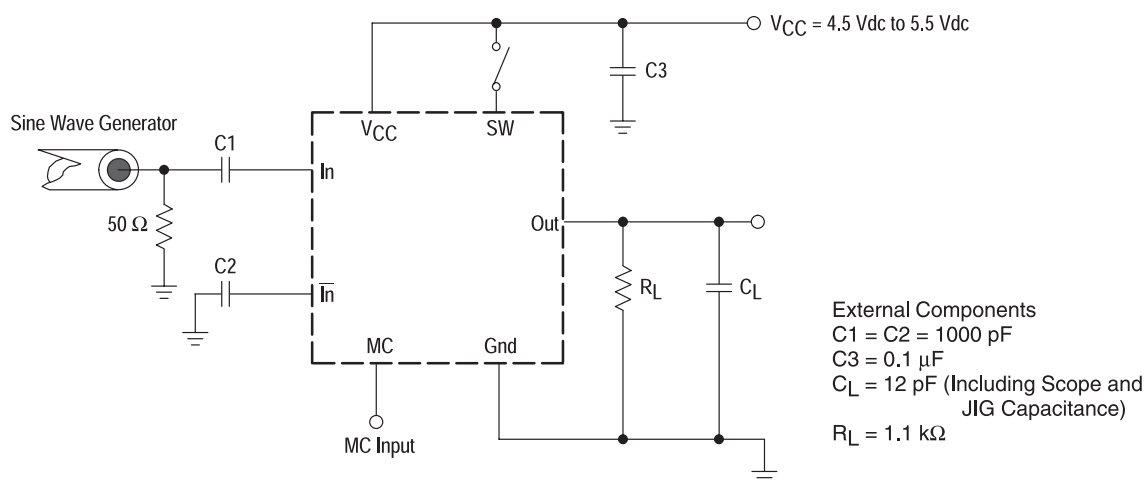


Figure 5. Input Signal Amplitude versus Input Frequency

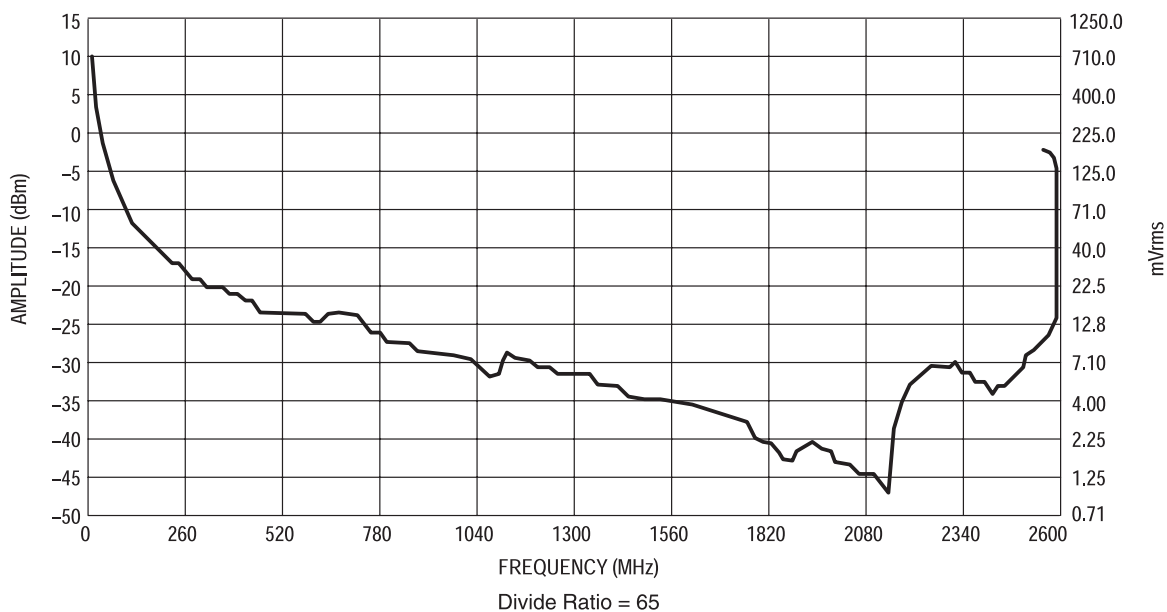


Figure 6. Output Amplitude versus Input Frequency

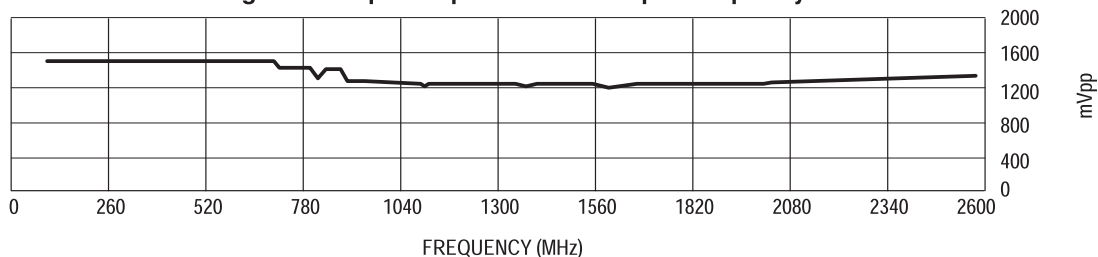


Figure 7. Generic block diagram showing prescaler connection to PLL device

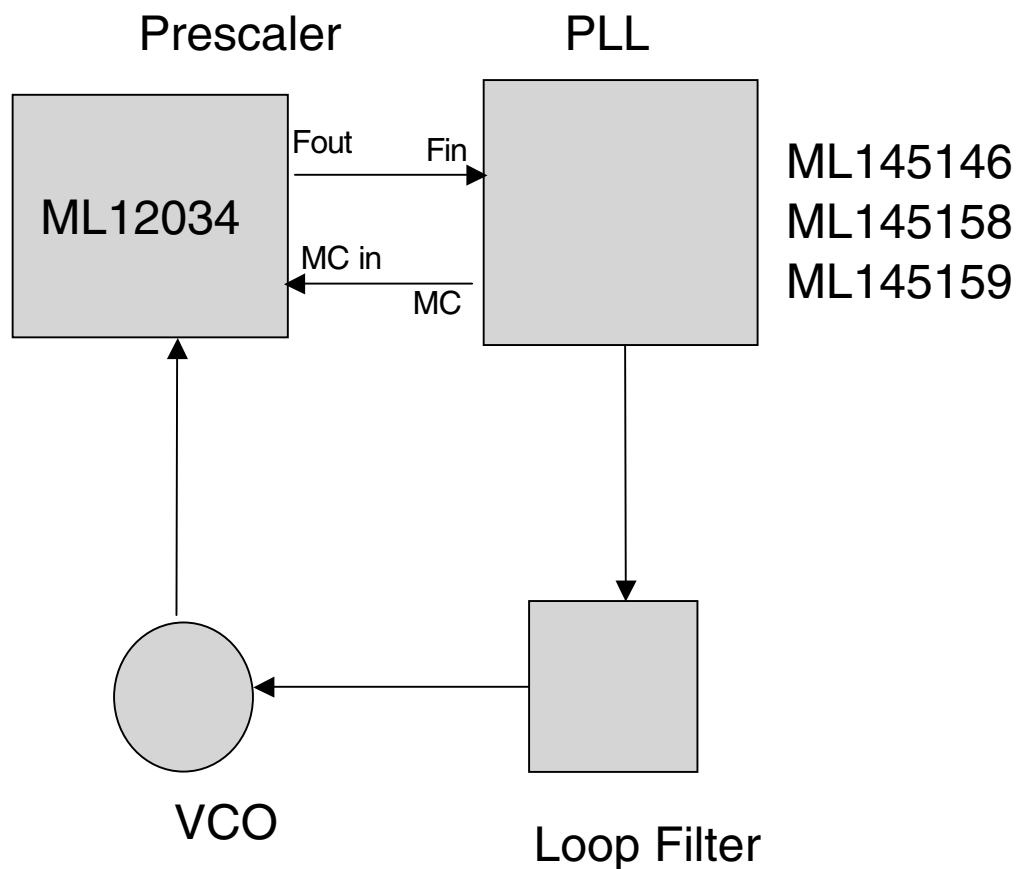
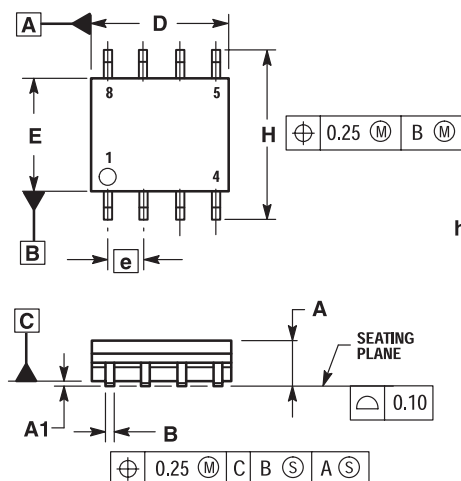


Figure 7 shows a generic block diagram of connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 describes using a two-modulus prescaler technique. By using a prescaler, higher frequencies can be achieved than by a single CMOS PLL device.

## OUTLINE DIMENSIONS

SO-8 = -5P  
 PLASTIC PACKAGE  
 (ML12034-5P)  
 CASE 751-06  
 (SO-8)  
 ISSUE T

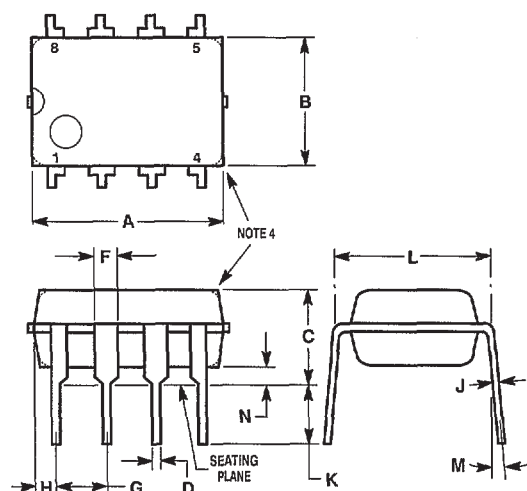


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

P DIP 8 = PP  
 PLASTIC PACKAGE  
 (ML12034PP)  
 CASE 626-04



## NOTES:

1. LEAD POSITIONAL TOLERANCE:

$$\phi 0.13 (0.005) \text{ (M) T A (M) B (M)}$$

2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

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