

### MECL PLL COMPONENTS

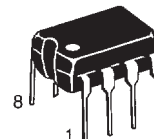
SEMICONDUCTOR TECHNICAL DATA

**Legacy Device:** Motorola MC12015, MC12016, MC12017

The ML12015, ML12016 and ML12017 are dual modulus prescalers which will drive divide by 32 and 33, 40 and 41, and 64 and 65, respectively. An internal regulator is provided to allow these devices to be used over a wide range of power-supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc  $\pm 10\%$  at Pin 7, or by applying an unregulated voltage source from 5.5 Vdc to 9.5 Vdc to Pin 8.

- 225 MHz Toggle Frequency
- Low-Power 7.5 mA Maximum at 6.8 V
- Control Input and Output Are Compatible With Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V
- Operating Temperature Range  $T_A = -40$  to  $85^\circ\text{C}$

**P DIP 8 = PP**  
PLASTIC PACKAGE  
CASE 626-04



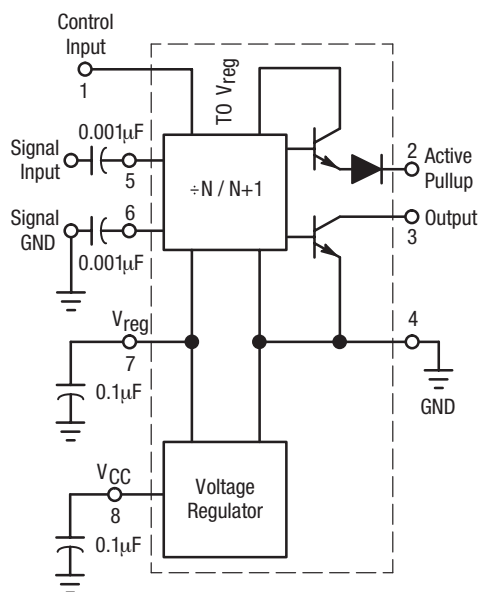
**SO 8 = -5P**  
PLASTIC PACKAGE  
CASE 751  
(SO-8)

#### CROSS REFERENCE/ORDERING INFORMATION

| PACKAGE | MOTOROLA | LANSDALE   |
|---------|----------|------------|
| P-DIP 8 | MC12015P | ML12015PP  |
| SO 8    | MC12015D | ML12015-5P |
| P-DIP 8 | MC12016P | ML12016PP  |
| SO 8    | MC12016D | ML12016-5P |
| P-DIP 8 | MC12017P | ML12017PP  |
| SO 8    | MC12017D | ML12017-5P |

**Note:** Lansdale lead free (Pb) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

#### SIMPLIFIED BLOCK DIAGRAM



1.  $V_{reg}$  at Pin 7 is not guaranteed to be between 4.5 and 5.5V when  $V_{CC}$  is being applied to Pin 8
2. Pin 7 is not to be used as a source of regulated output voltage

**MAXIMUM RATINGS**

| Rating                      | Symbol    | Value       | Unit |
|-----------------------------|-----------|-------------|------|
| Regulated Voltage, Pin 7    | $V_{reg}$ | 8.0         | Vdc  |
| Power Supply Voltage, Pin 8 | $V_{CC}$  | 10          | Vdc  |
| Operating Temperature Range | $T_A$     | -40 to +85  | °C   |
| Storage Temperature Range   | $T_{stg}$ | -65 to +175 | °C   |

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.5$  to  $9.5$  V;  $V_{reg} = 4.5$  to  $5.5$  V;  $T_A = -40$  to  $85^\circ\text{C}$ , unless otherwise noted.)

| Characteristic  | Symbol    | Min | Typ | Max             | Unit |
|---|-----------|-----|-----|-----------------|------|
| Toggle Frequency (Sine Wave Input)                            | $f_{max}$ | 225 | –   | –               | MHz  |
|   | $f_{min}$ | –   | –   | 35              |      |
| Supply Current  | $I_{CC}$  | –   | 6.0 | 7.8             | mA   |
| Control Input HIGH (+32, 40 or 64)                            | $V_{IH}$  | 2.0 | –   | –               | V    |
| Control Input LOW (+33, 41 or 65)                             | $V_{IL}$  | –   | –   | 0.8             | V    |
| Output Voltage HIGH ( $I_{source} = 50\mu\text{A}$ ) [Note 1] | $V_{OH}$  | 2.5 | –   | –               | V    |
| Output Voltage LOW ( $I_{sink} = 2\text{mA}$ ) [Note 1]       | $V_{OL}$  | –   | –   | 0.5             | V    |
|   |           |     |     |                 |      |
| Input Voltage Sensitivity                                     | $V_{in}$  |     |     |                 | mVpp |
|   |           | 400 | –   | 800             |      |
|   |           | 200 | –   | 800             |      |
| PLL Response Time [Notes 2 and 3]                             | $t_{PLL}$ | –   | –   | $t_{out}$ to 70 | ns   |

**NOTES:** 1. Pin 2 connected to Pin 3.

2.  $t_{PLL}$  = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.

3.  $t_{out}$  = period of output waveform.

Figure 1. Generic block diagram showing prescaler connection to PLL device

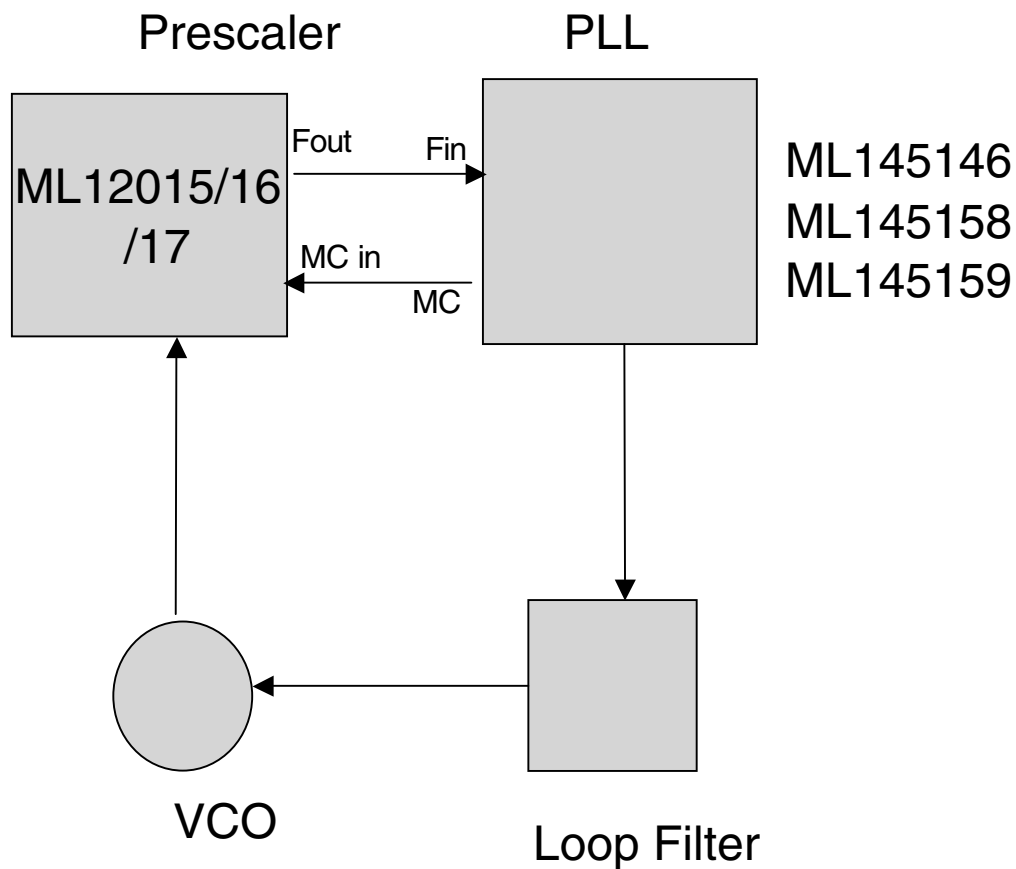
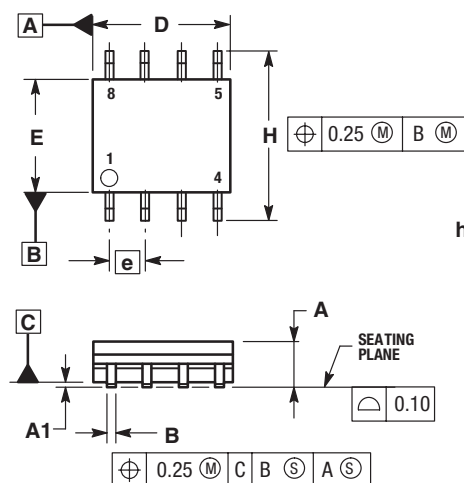


Figure 1. shows a generic block diagram for connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 describes using a two-modulus prescaler technique. By using prescaler higher frequencies can be achieved than by a single CMOS PLL device.

## OUTLINE DIMENSIONS

**SO 8 = -5P**  
**PLASTIC PACKAGE**  
 (ML12015-5P, ML12016-5P, ML12017-5P)  
 CASE 751-06  
 (SO-8)  
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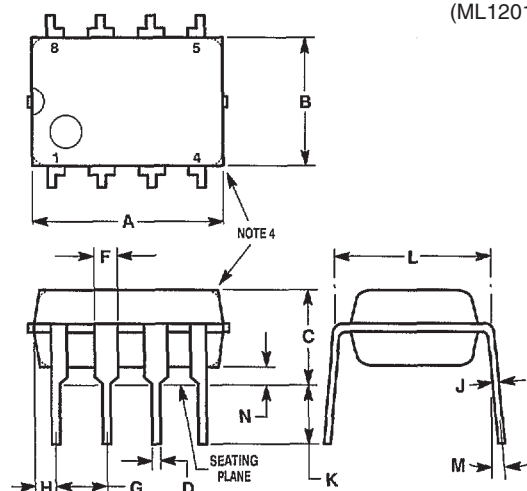


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 1.35        | 1.75 |
| A1  | 0.10        | 0.25 |
| B   | 0.35        | 0.49 |
| C   | 0.19        | 0.25 |
| D   | 4.80        | 5.00 |
| E   | 3.80        | 4.00 |
| e   | 1.27 BSC    |      |
| H   | 5.80        | 6.20 |
| h   | 0.25        | 0.50 |
| L   | 0.40        | 1.25 |
| θ   | 0°          | 7°   |

**P DIP 8 = PP**  
**PLASTIC PACKAGE**  
 (ML12015PP, ML12016PP, ML12017PP)  
 CASE 626-04



## NOTES:

1. LEAD POSITIONAL TOLERANCE:  
 $\phi 0.13 (0.005) (M) T A (M) B (M)$
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.40        | 10.16 | 0.370     | 0.400 |
| B   | 6.10        | 6.60  | 0.240     | 0.260 |
| C   | 3.94        | 4.45  | 0.155     | 0.175 |
| D   | 0.38        | 0.51  | 0.015     | 0.020 |
| F   | 1.02        | 1.52  | 0.040     | 0.060 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| H   | 0.76        | 1.27  | 0.030     | 0.050 |
| J   | 0.20        | 0.30  | 0.008     | 0.012 |
| K   | 2.92        | 3.43  | 0.115     | 0.135 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | — 10°       |       | — 10°     |       |
| N   | 0.51        | 0.76  | 0.020     | 0.030 |

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