LANSDALE Semiconductor, Inc.

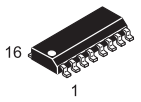
ML12013
MECL PLL Components
Dual Modulus Prescaler

Legacy Device: *Motorola MC12013*

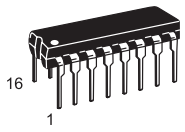
This device is a two–modulus prescaler which will divide by 10 and 11. A MECL–to–MTTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- 550 MHz (÷10/11)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- 5.0 or –5.2 V Operation*
- Buffered Clock Input — Series Input RC Typ, 20 Ω and 4.0 pF
- V_{BB} Reference Voltage
- 310 Milliwatts (Typ)

* When using a 5.0 V supply, apply 5.0 V to Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using –5.2 V supply, ground Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply –5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve DC power drain.



SO 16 = -5P
PLASTIC PACKAGE
CASE 751B
(SO–16)



P DIP 16 = EP
PLASTIC PACKAGE
CASE 648

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 16	MC12013P	ML12013EP
SOIC 16	MC12013D	ML12013-5P

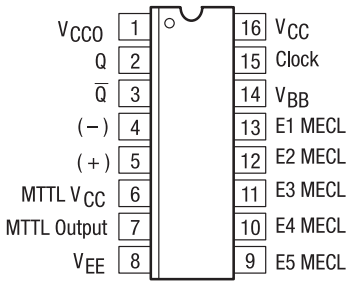
Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
(Ratings above which device life may be impaired)			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	–8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current Continuous Surge	I_O	 < 50 < 100	mAdc
Storage Temperature Range	T_{stg}	–65 to 175	°C
(Recommended Maximum Ratings above which performance may be degraded)			
Operating Temperature Range	T_A	–40 to +85	°C
DC Fan–Out (Note 1) (Gates and Flip–Flops)	n	70	–

NOTES: 1. AC fan–out is limited by desired system performance.

PIN CONNECTIONS



(Top View)

Figure 1. Logic Diagrams

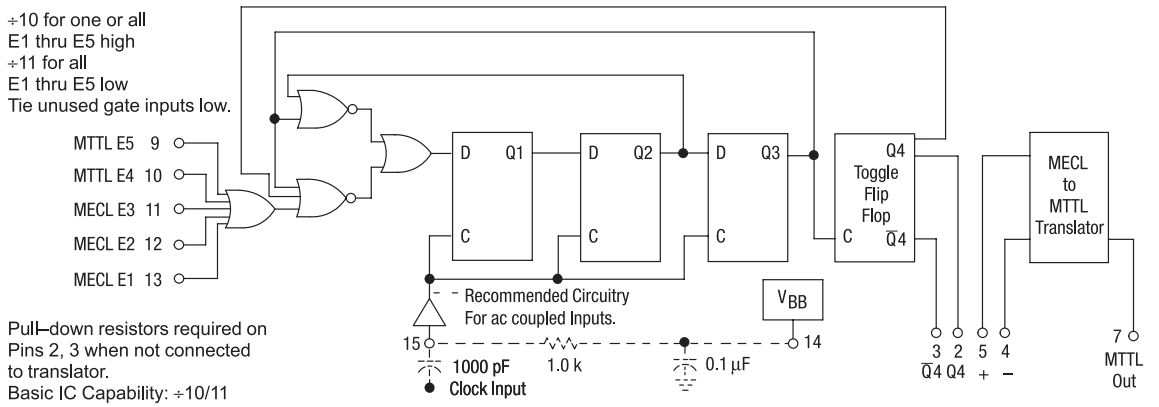


Figure 2a. Typical Frequency Synthesizer Application

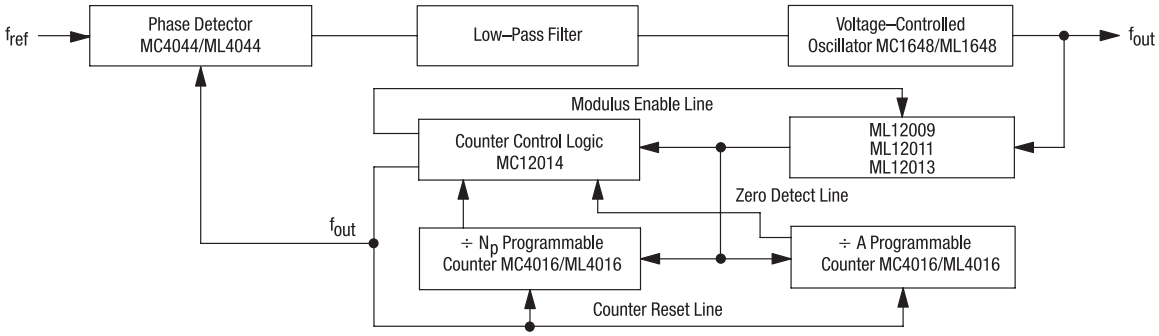


Figure 2b Generic block diagram showing prescaler connection to PLL Device

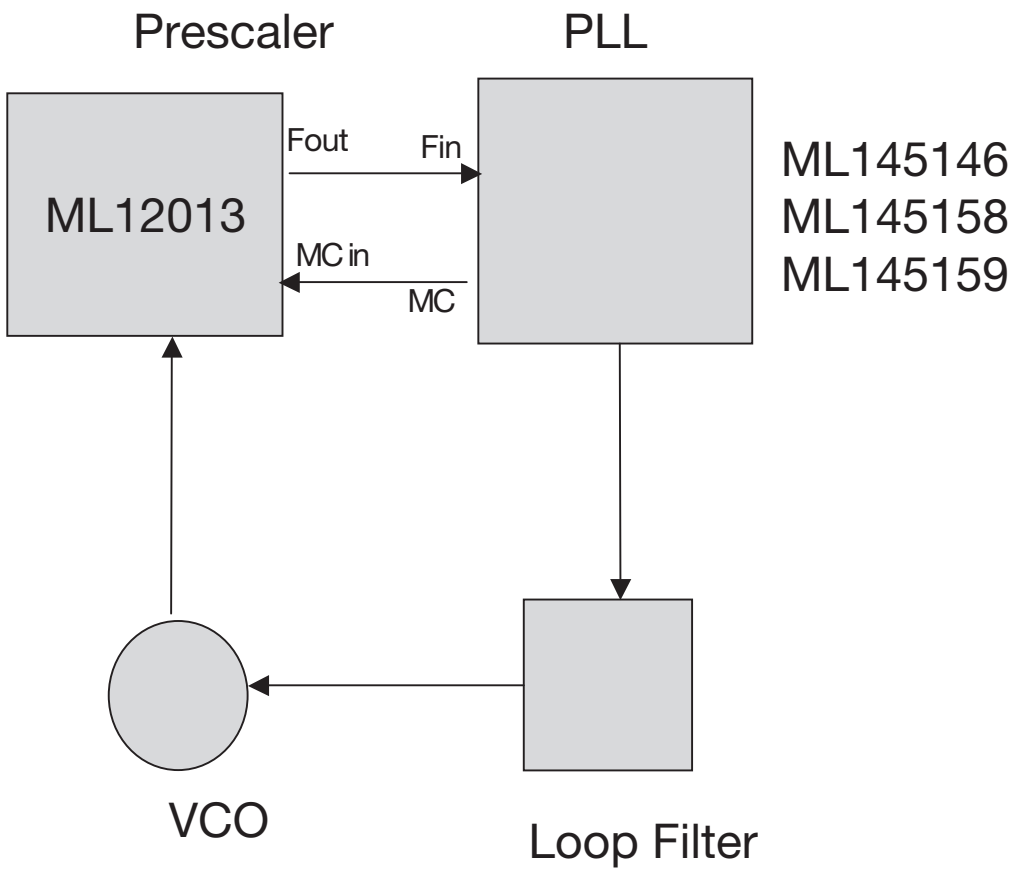
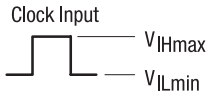


Figure 2b shhows a generic block diagram of connecting a prescaler to a PLL device that supports dual modulus control. Application note An535 describes using a two–modulus prescaler technique by using prescaler higher frequencies can be achieved than by a single CMOS PLL device

ELECTRICAL CHARACTERISTICS (Supply Voltage = –5.2 V, unless otherwise noted.)

Characteristic	Symbol	Pin Under Test	Test Limits						Unit
			–40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{CC1}	8	–88		–80		–80		mAdc
	I_{CC2}	6		5.2		5.2		5.2	mAdc
Input Current	I_{inH1}	15 11 12 13		375 375 375 375		250 250 250 250		250 250 250 250	μAdc
	I_{inH2}	4 5	1.7 1.7	6.0 6.0	2.0 2.0	6.0 6.0	2.0 2.0	6.4 6.4	mAdc
	I_{inH3}	5	0.7	3.0	1.0	3.0	1.0	3.6	
	I_{inH4}	9 10		100 100		100 100		100 100	μAdc
Leakage Current	I_{inL1}	15 11 12 13	–10 –10 –10 –10		–10 –10 –10 –10		–10 –10 –10 –10		μAdc
	I_{inL2}	9 10	–1.6 –1.6		–1.6 –1.6		–1.6 –1.6		mAdc
Reference Voltage	V_{BB}	14			–1.360	–1.160			Vdc
Logic '1' Output Voltage	V_{OH1} (Note 1)	2 3	–1.100 –1.100	–0.890 –0.890	–1.000 –1.000	–0.810 –0.810	–0.930 –0.930	–0.700 –0.700	Vdc
	V_{OH2}	7	–2.8		–2.6		–2.4		
Logic '0' Output Voltage	V_{OL1} (Note 1)	2 3	–1.990 –1.990	–1.675 –1.675	–1.950 –1.950	–1.650 –1.650	–1.925 –1.925	–1.615 –1.615	Vdc
	V_{OL2}	7		–4.26		–4.40		–4.48	
Logic '1' Threshold Voltage	V_{OHA} (Note 2)	2 3	–1.120 –1.120		–1.020 –1.020		–0.950 –0.950		Vdc
Logic '0' Threshold Voltage	V_{OLA} (Note 3)	2 3		–1.655 –1.655		–1.630 –1.630		–1.595 –1.595	Vdc
Short Circuit Current	I_{OS}	7	–65	–20	–65	–20	–65	–20	mAdc

NOTES: 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



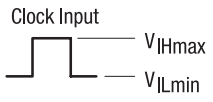
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to –2.0 V. Test procedures are shown for only one gate. The other gates are tested in the same manner.

ELECTRICAL CHARACTERISTICS (Supply Voltage = –5.2 V, unless otherwise noted.) (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{ILH}
	TEST VOLTAGE/CURRENT VALUES (Volts)					
–40°C	–0.890	–1.990	–1.205	–1.500	–2.8	–4.7
25°C	–0.810	–1.950	–1.105	–1.475	–2.8	–4.7
85°C	–0.700	–1.925	–1.035	–1.440	–2.8	–4.7

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	Gnd
Power Supply Drain Current	I_{CC1}	8							1,16
	I_{CC2}	6	4	5					6
Input Current	I_{inH1}	15 11 12 13	15 11 12 13						1,16 1,16 1,16 1,16
	I_{inH2}	4 5	5 5	4 4					6 6
	I_{inH3}	5	4	5					6
	I_{inH4}	9 10					9 10		1,16 1,16
Leakage Current	I_{inL1}	15 11 12 13							1,16 1,16 1,16 1,16
	I_{inL2}	9 10						9 10	1,16 1,16
Reference Voltage	V_{BB}	14							1,16
Logic ‘1’ Output Voltage	V_{OH1} (Note 1)	2 3		11,12,13 11,12,13				9,10 9,10	1,16 1,16
	V_{OH2}	7	5	4					6
Logic ‘0’ Output Voltage	V_{OL1} (Note 1)	2 3		11,12,13 11,12,13				9,10 9,10	1,16 1,16
	V_{OL2}	7	4	5					6
Logic ‘1’ Threshold Voltage	V_{OHA} (Note 2)	2 3			11,12,13 11,12,13				1,16 1,16
Logic ‘0’ Threshold Voltage	V_{OLA} (Note 3)	2 3				11,12,13 11,12,13			1,16 1,16
Short Circuit Current	I_{OS}	7	5	4				7	6

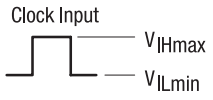
NOTES: 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS (Supply Voltage = –5.2 V, unless otherwise noted.) (continued)

			TEST VOLTAGE/CURRENT VALUES						
			Volts			mA			
@ Test Temperature			V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	
–40°C			–3.2	–4.4	–5.2	–0.25	16	–0.40	
25°C			–3.2	–4.4	–5.2	–0.25	16	–0.40	
85°C			–3.2	–4.4	–5.2	–0.25	16	–0.40	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd
			V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	
Power Supply Drain Current	I_{CC1}	8			8				1,16
	I_{CC2}	6			8				6
Input Current	I_{inH1}	15 11 12 13	 9,10 9,10 9,10		8 8 8 8				1,16 1,16 1,16 1,16
	I_{inH2}	4 5			8 8				6 6
	I_{inH3}	5			8				6
	I_{inH4}	9 10			8 8				1,16 1,16
Leakage Current	I_{inL1}	15 11 12 13			8,15 8,11 8,12 8,13				1,16 1,16 1,16 1,16
	I_{inL2}	9 10			8 8				1,16 1,16
Reference Voltage	V_{BB}	14			8	14			1,16
Logic ‘1’ Output Voltage	V_{OH1} (Note 1)	2 3			8 8				1,16 1,16
	V_{OH2}	7			8			7	6
Logic ‘0’ Output Voltage	V_{OL1} (Note 1)	2 3			8 8				1,16 1,16
	V_{OL2}	7			8		7		6
Logic ‘1’ Threshold Voltage	V_{OHA} (Note 2)	2 3	9,10 9,10		8 8				1,16 1,16
Logic ‘0’ Threshold Voltage	V_{OLA} (Note 3)	2 3		9,10 9,10	8 8				1,16 1,16
Short Circuit Current	I_{OS}	7			8				6

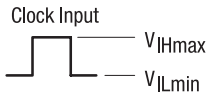
NOTES: 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS (Supply Voltage = 5.0 V, unless otherwise noted.)

Characteristic	Symbol	Pin Under Test	Test Limits						Unit
			–40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{CC1}	8	–88		–80		–80		mAdc
	I_{CC2}	6		5.2		5.2		5.2	mAdc
Input Current	I_{inH1}	15 11 12 13		375 375 375 375		250 250 250 250		250 250 250 250	µAdc
	I_{inH2}	4 5	1.7 1.7	6.0 6.0	2.0 2.0	6.0 6.0	2.0 2.0	6.4 6.4	mAdc
	I_{inH3}	5	0.7	3.0	1.0	3.0	1.0	3.6	
	I_{inH4}	9 10			100 100	100 100		100 100	µAdc
Leakage Current	I_{inL1}	15 11 12 13	–10 –10 –10 –10		–10 –10 –10 –10		–10 –10 –10 –10		µAdc
	I_{inL2}	9 10	–1.6 –1.6		–1.6 –1.6		–1.6 –1.6		mAdc
Reference Voltage	V_{BB}	14			3.67	3.87			Vdc
Logic ‘1’ Output Voltage	V_{OH1} (Note 1)	2 3	3.900 3.900	4.110 4.110	4.000 4.000	4.190 4.190	4.070 4.070	4.300 4.300	Vdc
	V_{OH2}	7	2.4		2.6		2.8		
Logic ‘0’ Output Voltage	V_{OL1} (Note 1)	2 3	3.070 3.070	3.385 3.385	3.110 3.110	3.410 3.410	3.135 3.135	3.445 3.445	Vdc
	V_{OL2}	7		0.94		0.80		0.72	
Logic ‘1’ Threshold Voltage	V_{OHA} (Note 2)	2 3	3.880 3.880		3.980 3.980		4.050 4.050		Vdc
Logic ‘0’ Threshold Voltage	V_{OLA} (Note 3)	2 3		3.405 3.405		3.430 3.430		3.465 3.465	Vdc
Short Circuit Current	I_{OS}	7	–65	–20	–65	–20	–65	–20	mAdc

NOTES: 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



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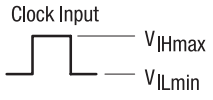
ELECTRICAL CHARACTERISTICS (Supply Voltage = 5.0 V, unless otherwise noted.) (continued)

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{ILH}
–40°C	4.110	3.070	3.795	3.500	2.4	0.5
25°C	4.190	3.110	3.895	3.525	2.4	0.5
85°C	4.300	3.135	3.965	3.560	2.4	0.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	(V_{EE}) Gnd
Power Supply Drain Current	I_{CC1}	8							8
	I_{CC2}	6	4	5					8
Input Current	I_{inH1}	15 11 12 13	15 11 12 13						8 8 8 8
	I_{inH2}	4 5	5 5	4 4					8 8
	I_{inH3}	5	4	5					8
	I_{inH4}	9 10					9 10		8 8
Leakage Current	I_{inL1}	15 11 12 13							8,15 8,11 8,12 8,13
	I_{inL2}	9 10						9 10	8 8
Reference Voltage	V_{BB}	14							8
Logic '1' Output Voltage	V_{OH1} (Note 1)	2 3		11,12,13 11,12,13				9,10 9,10	8 8
	V_{OH2}	7	5	4					8
Logic '0' Output Voltage	V_{OL1} (Note 1)	2 3		11,12,13 11,12,13				9,10 9,10	8 8
	V_{OL2}	7	4	5					8
Logic '1' Threshold Voltage	V_{OHA} (Note 2)	2 3			11,12,13 11,12,13				8 8
Logic '0' Threshold Voltage	V_{OLA} (Note 3)	2 3				11,12,13 11,12,13			8 8
Short Circuit Current	I_{OS}	7	5	4				7	8

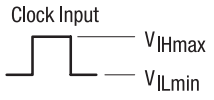
NOTES: 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS (Supply Voltage = 5.0 V, unless otherwise noted.) (continued)

			TEST VOLTAGE/CURRENT VALUES						
			Volts			mA			
@ Test Temperature			V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	
–40°C			2.0	0.8	5.0	–0.25	16	–0.40	
25°C			2.0	0.8	5.0	–0.25	16	–0.40	
85°C			2.0	0.8	5.0	–0.25	16	–0.40	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						(V_{EE}) Gnd
			V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	
Power Supply Drain Current	I_{CC1}	8			1,16				8
	I_{CC2}	6			6				8
Input Current	I_{inH1}	15 11 12 13	 9,10 9,10 9,10		1,16 1,16 1,16 1,16				8 8 8 8
	I_{inH2}	4 5			6 6				8 8
	I_{inH3}	5			6				8
	I_{inH4}	9 10			1,16 1,16				8 8
Leakage Current	I_{inL1}	15 11 12 13			1,16 1,16 1,16 1,16				8,15 8,11 8,12 8,13
	I_{inL2}	9 10			1,16 1,16				8 8
Reference Voltage	V_{BB}	14			1,16	14			8
Logic '1' Output Voltage	V_{OH1} (Note 1)	2 3			1,16 1,16				8 8
	V_{OH2}	7			6			7	8
Logic '0' Output Voltage	V_{OL1} (Note 1)	2 3			1,16 1,16				8 8
	V_{OL2}	7			6		7		8
Logic '1' Threshold Voltage	V_{OHA} (Note 2)	2 3	9,10 9,10		1,16 1,16				8 8
Logic '0' Threshold Voltage	V_{OLA} (Note 3)	2 3		9,10 9,10	1,16 1,16				8 8
Short Circuit Current	I_{OS}	7			6				8

NOTES: 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	ML12013 –40°C Min	–40°C Typ	–40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Typ	85°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen.1	Pulse Gen.2	Pulse Gen.3	V_{IHmin} †	V_{ILmin} †	V_F –3.0 V	V_{EE} –3.0 V	V_{CC} 2.0
Propagation Delay (See Figures 3 and 5)	$t_{15+\,2+}$	2	—	—	8.1	—	—	8.1	—	—	8.9	ns	15	—	—	—	11,12,13	9,10	8	1,6,16
	$t_{15+\,2-}$	2	—	—	7.5	—	—	7.5	—	—	8.2	↓	15	—	—	—	11,12,13	9,10	8	1,6,16
	$t_{5+\,7+}$	7	—	—	8.4	—	—	8.1	—	—	8.9		A	—	—	—	—	—	8	1,6,16
	$t_{5-\,7-}$	7	—	—	6.5	—	—	6.5	—	—	7.1		A	—	—	—	—	—	8	1,6,16
Setup Time (See Figures 4 and 5)	t_{setup1}	11	5.0	—	—	5.0	—	—	5.0	—	—	ns	15	*	—	—	*	9,10	8	1,6,16
	t_{setup2}	9	5.0	—	—	5.0	—	—	5.0	—	—	ns	15	—	*	—	11,12,13	*	8	1,6,16
Release Time (See Figures 4 and 5)	t_{rel1}	11	5.0	—	—	5.0	—	—	5.0	—	—	ns	15	*	—	—	*	9,10	8	1,6,16
	t_{rel2}	9	5.0	—	—	5.0	—	—	5.0	—	—	ns	15	—	*	—	11,12,13	*	8	1,6,16
Toggle Frequency (See Figure 6) ÷10/11	f_{max}	2	500	—	—	550	—	—	500	—	—	MHz	—	—	—	11	—	—	8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

	–40°C	25°C	85°C	
†V_{IHmin}	1.03	1.115	1.20	Vdc
†V_{ILmin}	0.175	0.200	0.235	Vdc

Figure 3. AC Voltage Waveforms

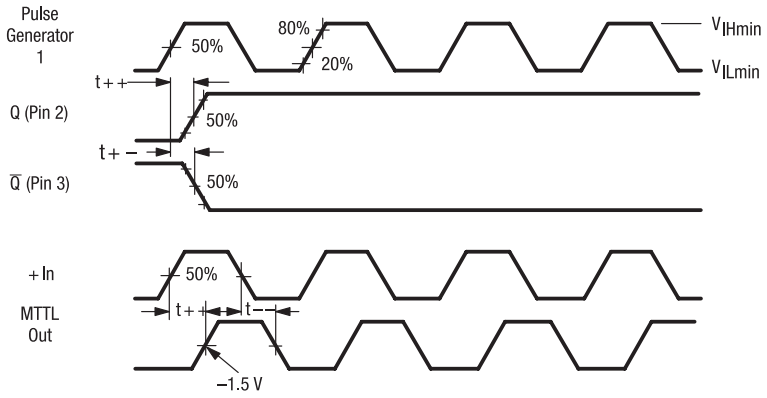


Figure 4. Setup and Release Time Waveforms

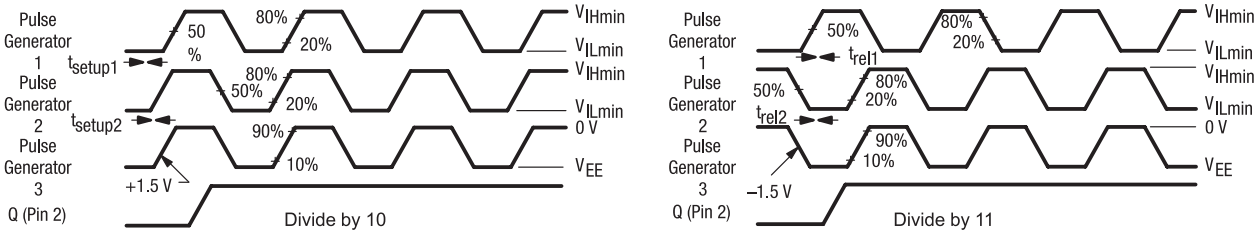
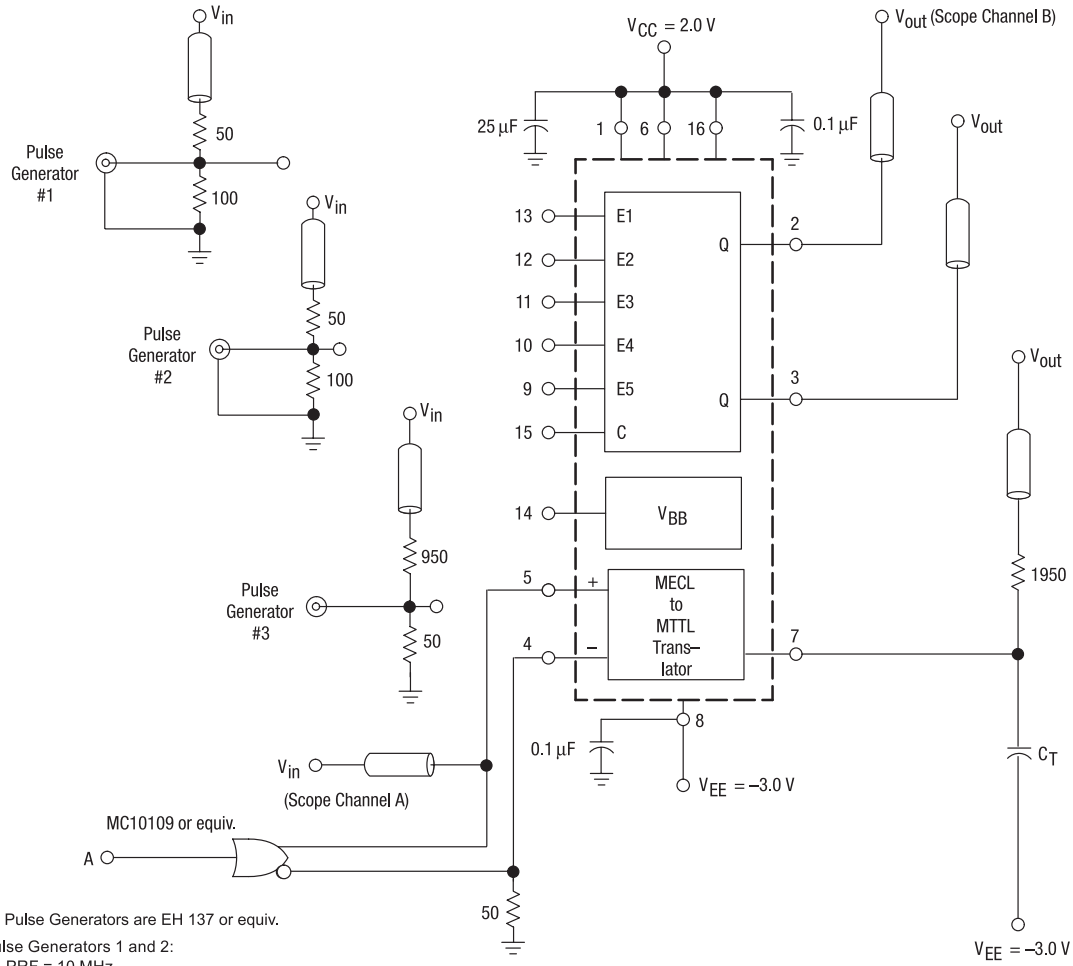


Figure 5. AC Test Circuit



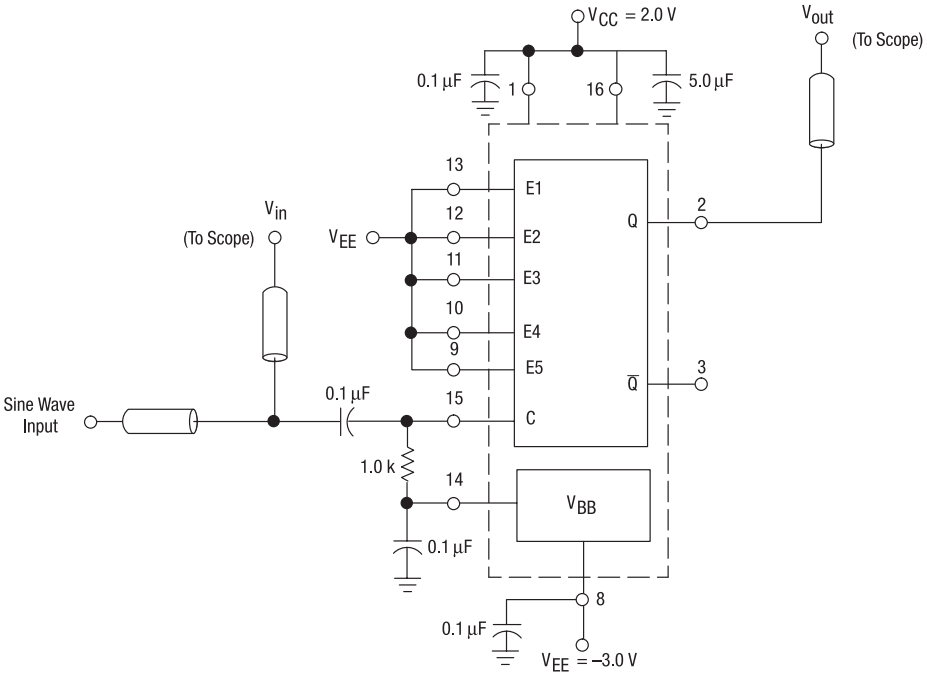
All Pulse Generators are EH 137 or equiv.

Pulse Generators 1 and 2:
PRF = 10 MHz
PW = 50% Duty Cycle
$t_+ = t_- = 2.0 \pm 0.2$ ns

Pulse Generator 3:
PRF = 2.0 MHz
PW = 50% Duty Cycle
$t_+ = t_- = 5.0 \pm 0.5$ ns

All resistors are +1%.
All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
The 1950 Ω resistor at Pin 7 and the scope termination impedance constitute a 40 :1 attenuator probe.
C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.
Unused output connected to a 50 Ω resistor to ground.

Figure 6. Maximum Frequency Test Circuit



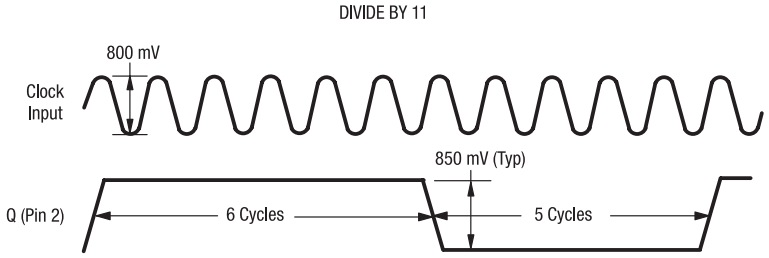
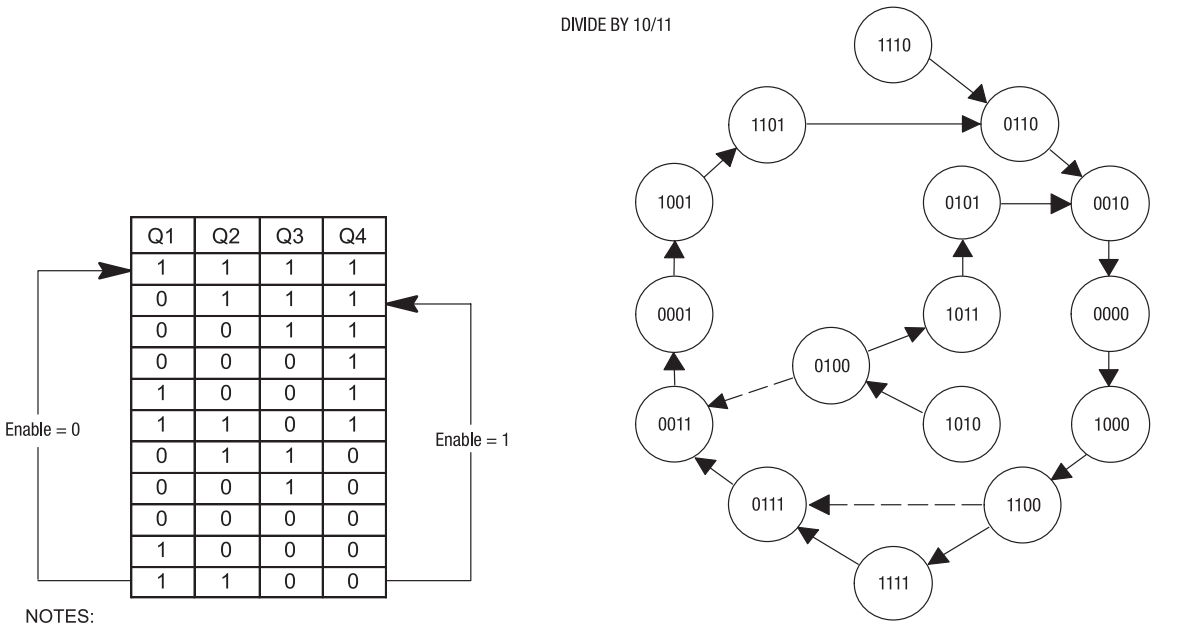


Figure 7. State Diagram



NOTES:

— — — Enable = 1.

The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.

APPLICATIONS INFORMATION

The primary application of this device is as a high–speed variable modulus prescaler in the divide by N section of a phase–locked loop synthesizer used as the local oscillator of two–way radios.

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In it's basic form, this device will divide by 10/11. Division by 10 occurs when any one or all of the five gate inputs E1 through E5 are high. Division by 11 occurs when all inputs E1 through E5 are low. (Unconnected MTTL inputs are normally high, unconnected MECL inputs are normally low). With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.) A few of the many configurations are shown below.

Figure 8. Divide By 10/11

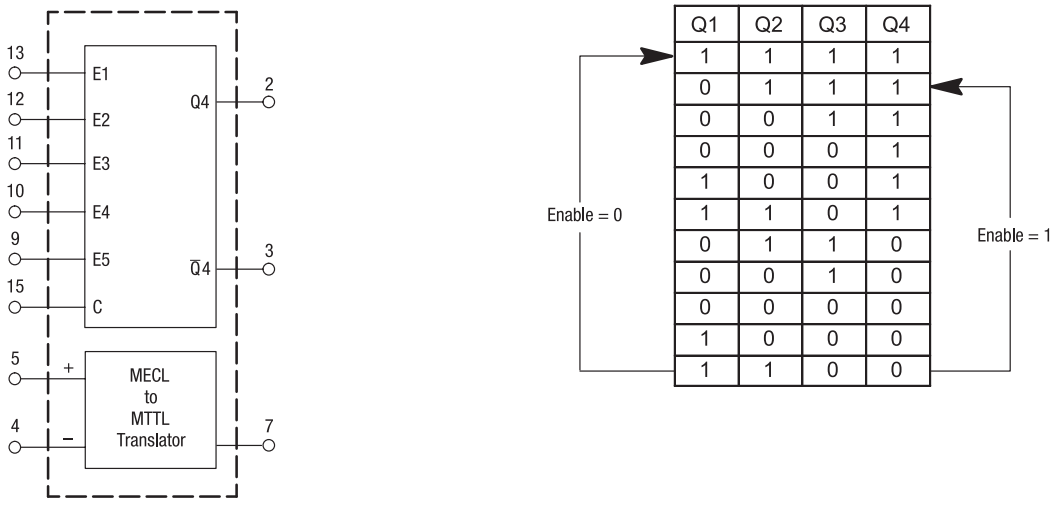
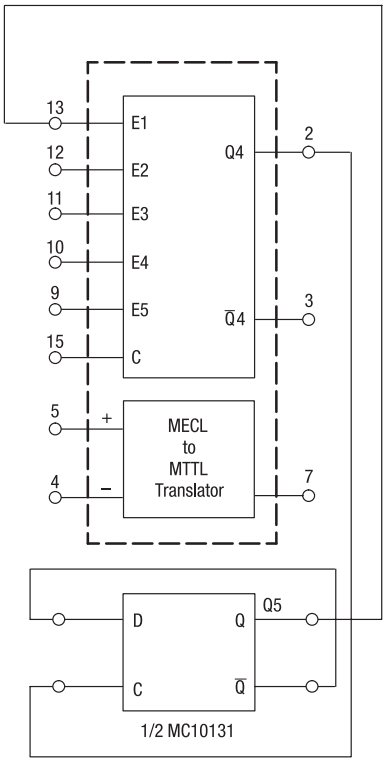


Figure 9. Divide By 20/21



COUNT	Q1	Q2	Q3	Q4	Q4
31	1	1	1	1	1
30	0	1	1	1	1
28	0	0	1	1	1
24	0	0	0	1	1
25	1	0	0	1	1
27	1	1	0	1	1
22	0	1	1	0	1
20	0	0	1	0	1
16	0	0	0	0	1
17	1	0	0	0	1
19	1	1	0	0	1
14	0	1	1	1	0
12	0	0	1	1	0
8	0	0	0	1	0
9	1	0	0	1	0
11	1	1	0	1	0
6	0	1	1	0	0
4	0	0	1	0	0
0	0	0	0	0	0
1	1	0	0	0	0
3	1	1	0	0	0

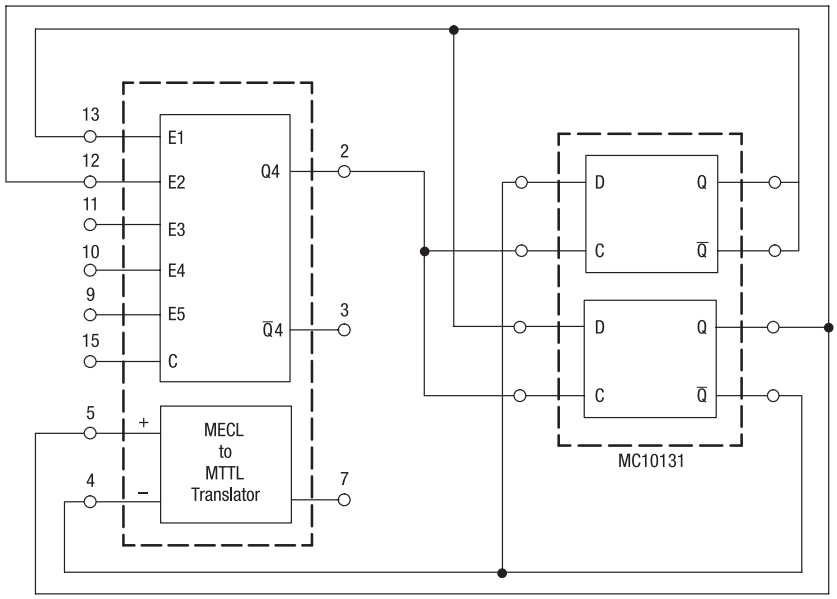
E2 + E3 + E4 + E5 = 0

E2 + E3 + E4 + E5 = 1

To obtain an MTTL output, connect Pins 5 and 4 to Pins 2 and 3, respectively. Termination resistors for the MECL outputs are not shown, but are required except for the flip–flop driving the translator section.

The ÷20/21 counter may also be built using an MTTL flip–flop by connecting Pins 5 and 4 to Pins 2 and 3 respectively, and driving the MTTL flip–flop with Pin 7. ML12013 inputs E4 and E5 are used rather than E1. With E1 + E2 + E3 = 0, operation remains as shown.

Figure 10. Divide By 40/41

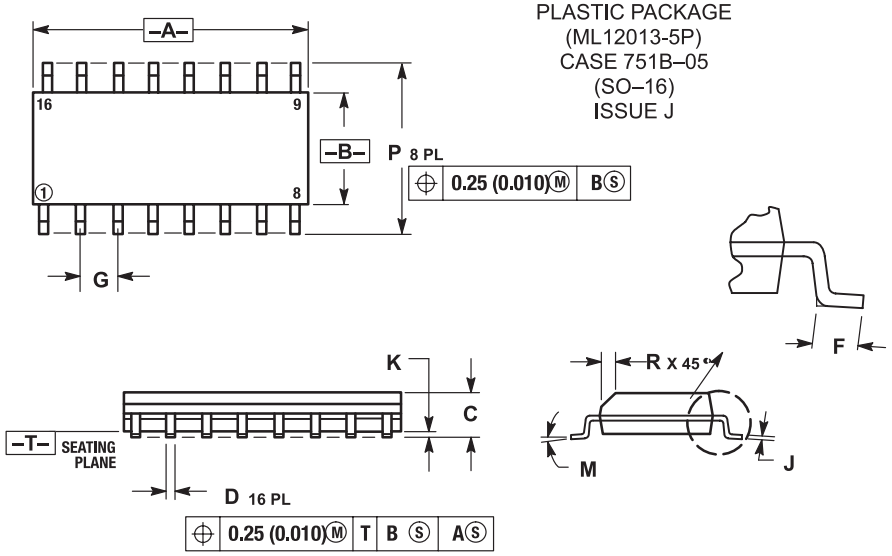


For ÷40 : E4 + E5 = 1
For ÷41 : E4 + E5 = 0

Termination resistors for MECL outputs are not shown, but are required except for the flip–flop driving the translator section.

OUTLINE DIMENSIONS

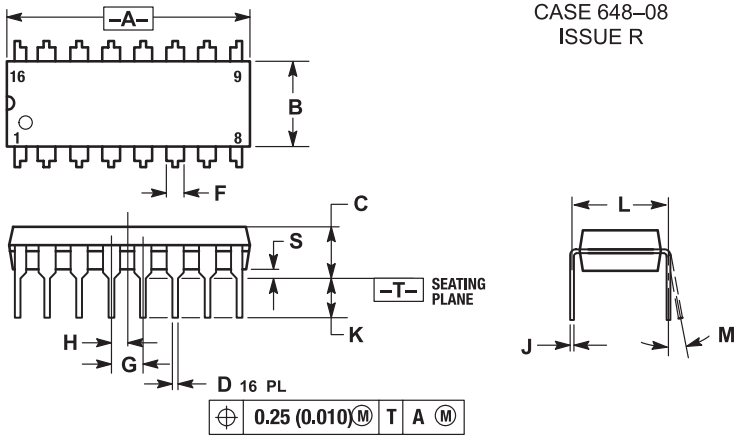
SO 16 = -5P
PLASTIC PACKAGE
(ML12013-5P)
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

P DIP 16 = EP
PLASTIC PACKAGE
(ML12013EP)
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01