PYRAMID SEMICONDUCTOR CORPORATION

PYX28HC64

8K X 8 EEPROM

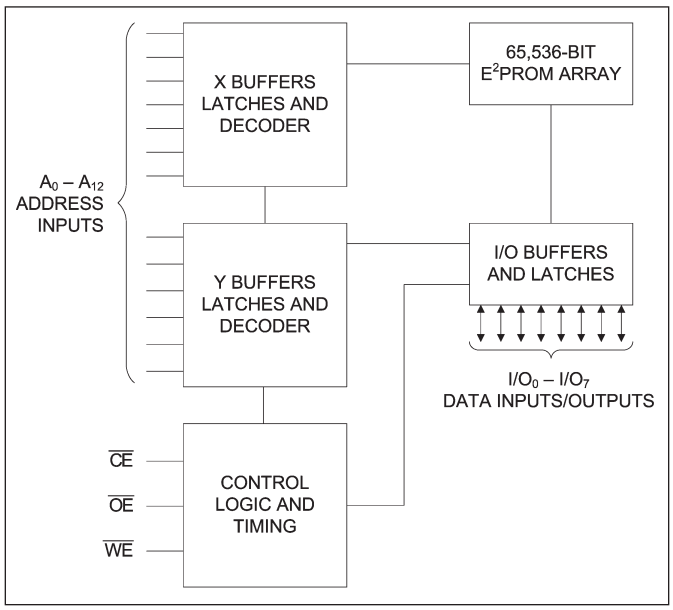
FEATURES

- **Access Times of 70, 90, and 120ns**
- **Single 5V±10% Power Supply**
- **Simple Byte and Page Write**
- **Low Power CMOS:**
  - **40 mA Active Current**
  - **200 µA Standby Current**
- **Fast Write Cycle Times**
- **Software Data Protection**
- **Fully TTL Compatible Inputs and Outputs**
- **Endurance: 100,000 Cycles**
- **Data Retention: 100 Years**
- **Available in the following packages:**
  - **– 32-Pin Ceramic LCC (450 x 550 mils)**
  - **– 28-Pin 600 mil Ceramic DIP**

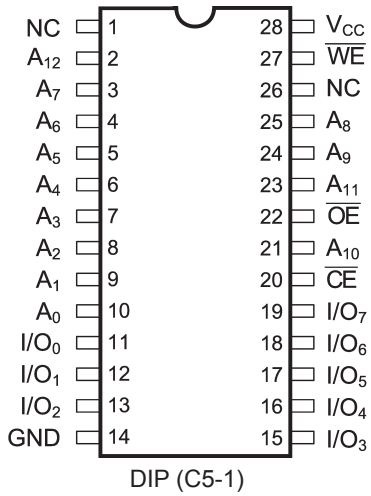
DESCRIPTION

The PYX28HC64 is a 5 Volt 8Kx8 EEPROM using floating gate CMOS Technology. The device supports 64-byte page write operation. The PYX28HC64 features $\overline{\text{DATA}}$ and Toggle Bit Polling as well as a system software scheme used to indicate early completion of a Write Cycle. The device also includes user-optional software data protection. Endurance is 100,000 Cycles and Data Retention is 100 Years. The device is available in a 32-Pin LCC package as well as a 28-Pin 600 mil wide Ceramic DIP.

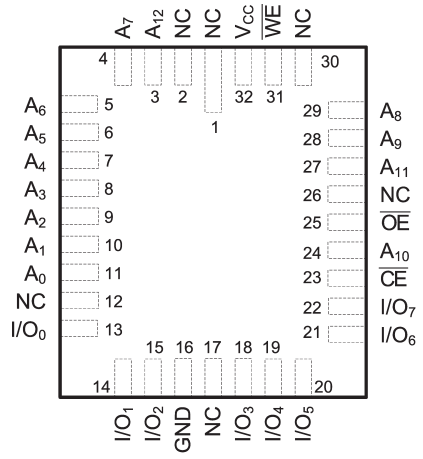
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (C5-1)



LCC (L6)

MAXIMUM RATINGS(1)

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.3 to +6.25	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to +6.25	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade(2)	Ambient Temp	GND	V_{cc}
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES(4)

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)(2)

Sym	Parameter	Test Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5(3)	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC} - 0.2	V_{CC} + 0.5	V
V_{LC}	CMOS Input Low Voltage		-0.5(3)	0.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +5 mA, V_{CC} = Min		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -5 mA, V_{CC} = Min	2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max V_{IN} = GND to V_{CC}	-10	+10	µA
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-10	+10	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}$ ≥ V_{IH}, $\overline{OE}$ = V_{IL}, V_{CC} = Max, f = Max, Outputs Open	—	3	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max, f = Max, Outputs Open, V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	—	250	µA
I_{CC}	Supply Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Inputs = V_{CC} = 5.5V	—	40	µA

Notes:

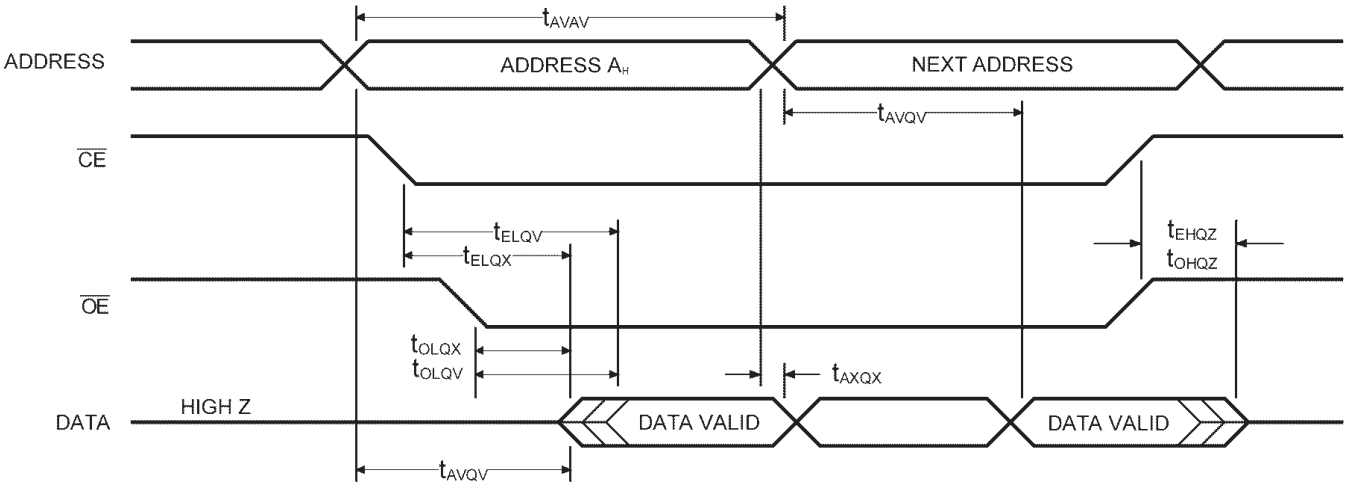
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-70		-90		-120		Unit
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	70		90		120		ns
t_{AVQV}	Address Access Time		70		90		120	ns
t_{ELQV}	Chip Enable Access Time		70		90		120	ns
t_{OLQV}	Output Enable Access Time		40		50		60	ns
t_{ELQX}	Chip Enable to Output in Low Z	10		10		10		ns
t_{EHQZ}	Chip Disable to to Output in High Z		50		50		50	ns
t_{OLQX}	Output Enable to Output in Low Z	10		10		10		ns
t_{OHQZ}	Output Disable to Output in High Z		50		50		50	ns
t_{AVQX}	Output Hold from Address Change	0		0		0		ns
t_{PU}	Chip Enable to Power Up Time		90		90		90	ns
t_{PD}	Chip Disable to Power Down Time		10		10		10	ns

TIMING WAVEFORM OF READ CYCLE

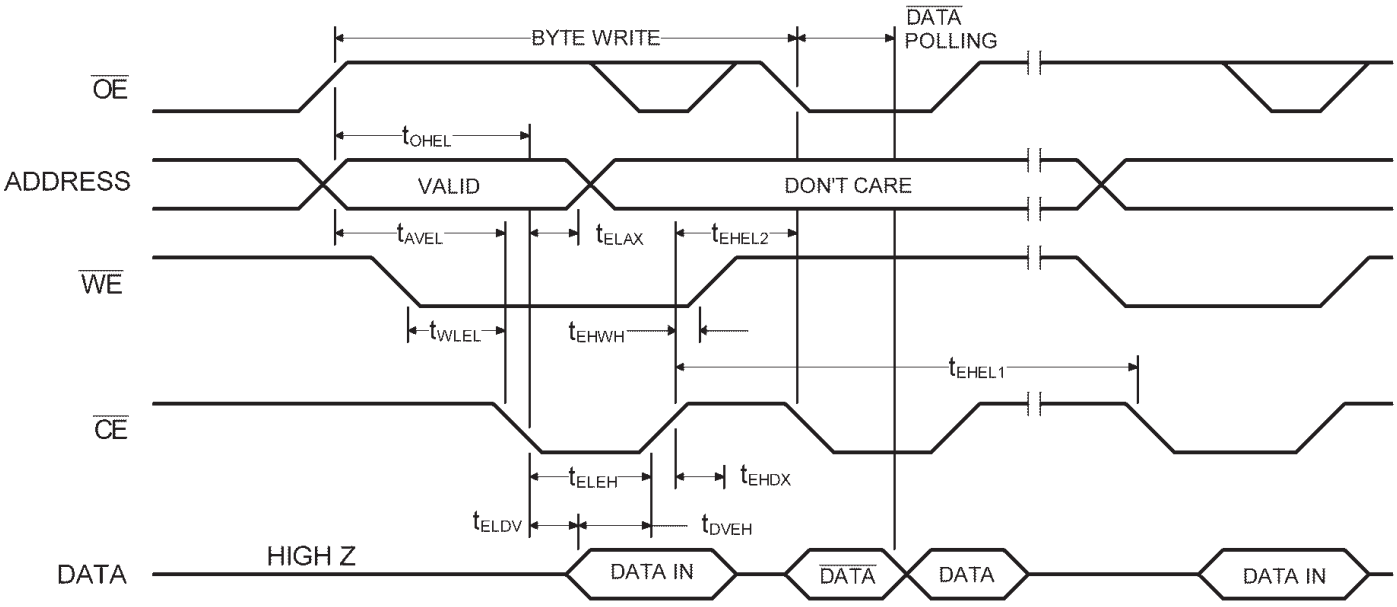


AC CHARACTERISTICS—WRITE CYCLE

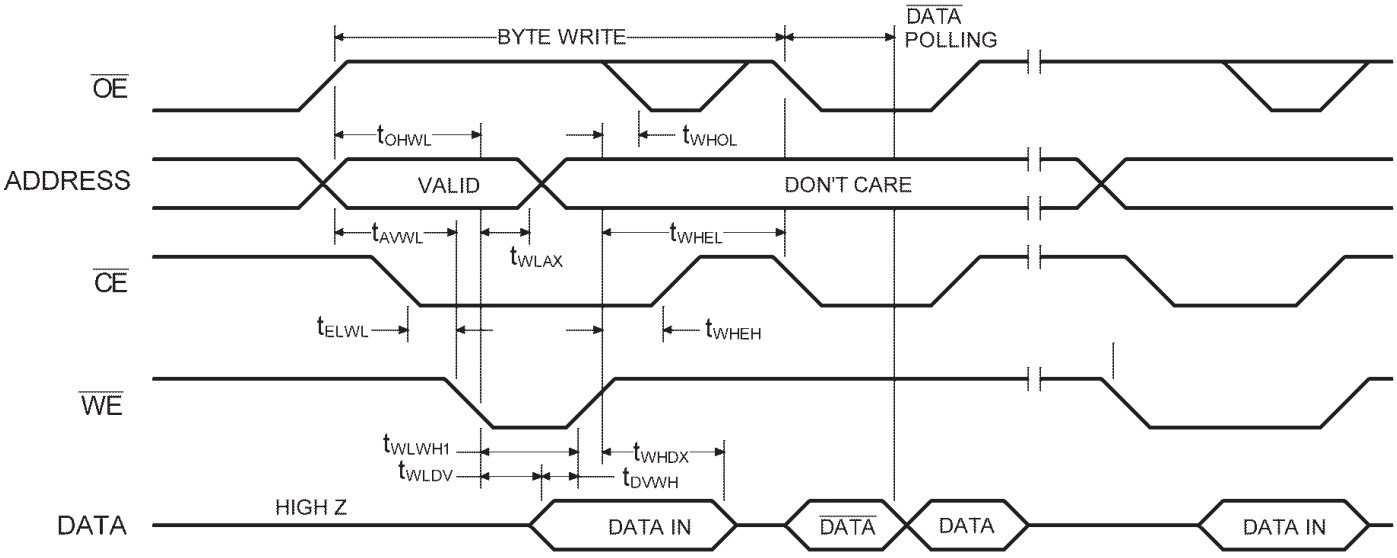
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-70		-90		-120		Unit
		Min	Max	Min	Max	Min	Max	
t_{WHWL1} t_{EHEL1}	Write Cycle Time		5		5		5	ms
t_{AVEL} t_{AVWL}	Address Setup Time	10		10		10		ns
t_{ELAX} t_{WLAX}	Address Hold Time	60		60		60		ns
t_{WLEL} t_{ELWL}	Write Setup Time	0		0		0		ns
t_{WHEH}	Write Hold Time	0		0		0		ns
t_{OHEL} t_{OHWL}	OE Setup Time	10		10		10		ns
t_{WHOL}	OE Hold Time	10		10		10		ns
t_{ELEH} t_{WLWH}	WE Pulse Width	60		60		60		ns
t_{DVEH} t_{DVWH}	Data Setup Time	50		50		50		ns
t_{EHDX} t_{WHDX}	Data Hold Time	10		10		10		ns
t_{EHEL2} t_{WHWL2}	Byte Load Cycle Time	0.2	2	0.2	2	0.2	2	µs
t_{ELWL}	CE Setup Time	1		1		1		µs
t_{OVHWL}	Output Setup Time	1		1		1		µs
t_{EHWH}	CE Hold Time	1		1		1		µs
t_{WHOH}	OE Hold Time	1		1		1		µs
t_{OHAV}	Erase Time	200		200		200		ms
t_{WLWH2}	Chip Erase Time	150		150		150		ns
V_H	High Voltage for Chip Clear	12	13	12	13	12	13	V

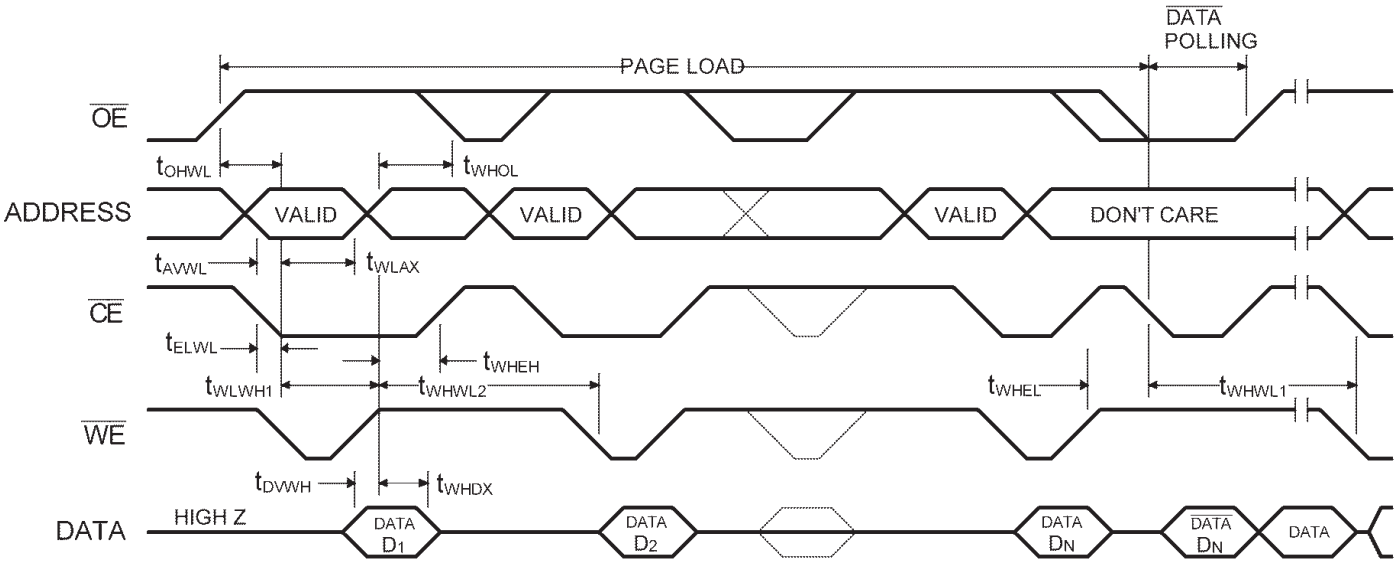
TIMING WAVEFORM OF BYTE WRITE CYCLE ($\overline{CE}$ CONTROLLED)



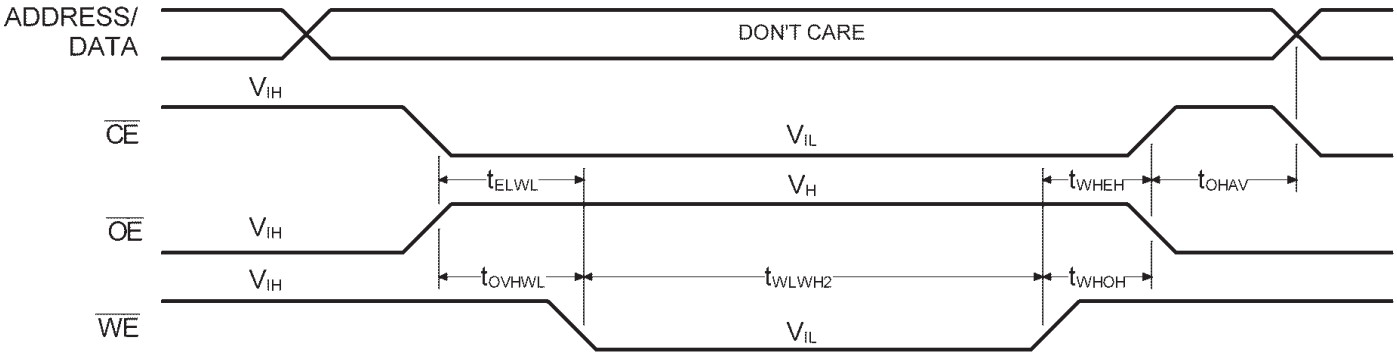
TIMING WAVEFORM OF BYTE WRITE CYCLE ($\overline{WE}$ CONTROLLED)



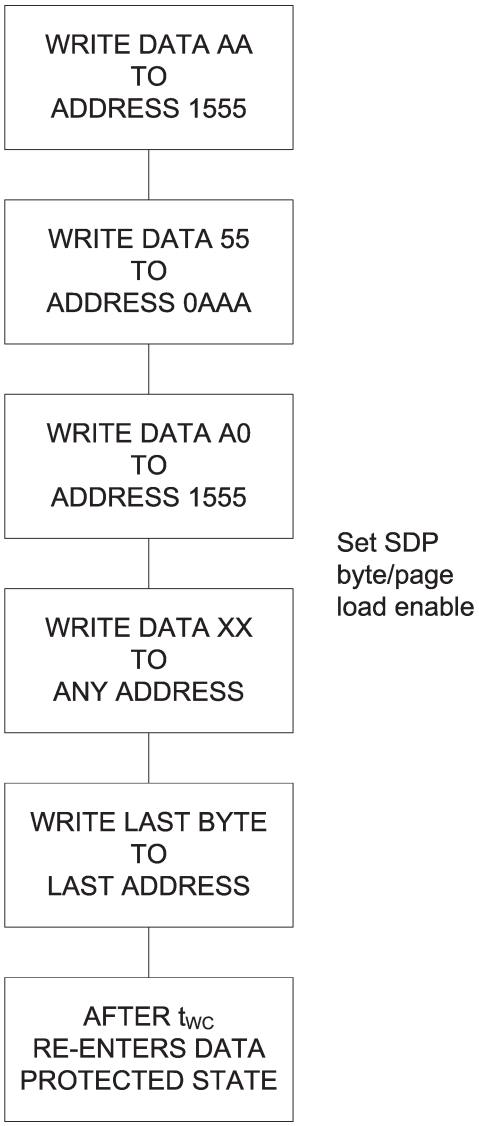
TIMING WAVEFORM OF PAGE WRITE CYCLE



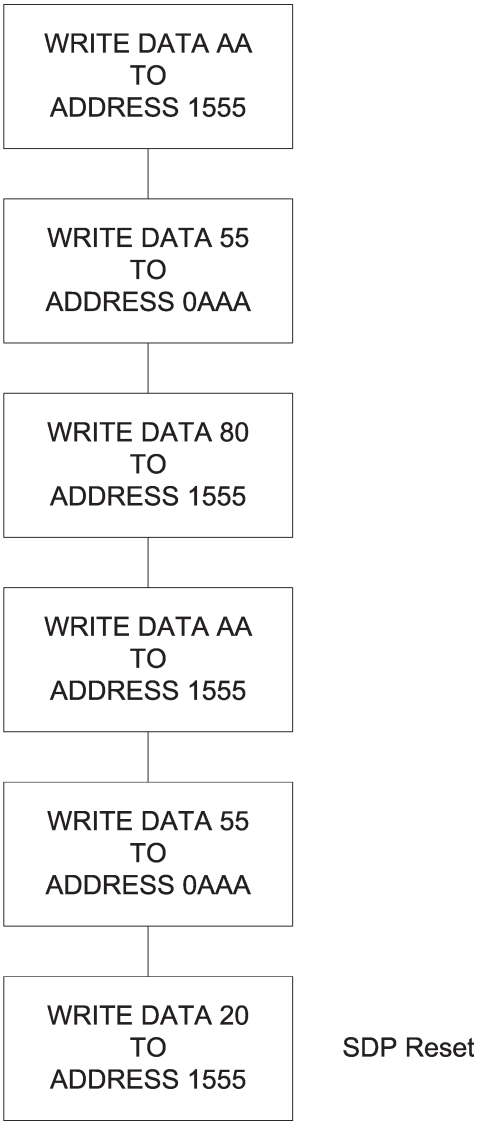
TIMING WAVEFORM OF CHIP CLEAR CYCLE



WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION



SOFTWARE SEQUENCE TO DE-ACTIVATE SOFTWARE DATA PROTECTION



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figure 1

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Chip Clear	V_{IL}	V_{IH}	V_{IL}	X
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X	V_{IL}	X	High Z / D_{OUT}
Write Inhibit	X	X	V_{IH}	High Z / D_{OUT}
Standby	V_{IH}	X	X	High Z

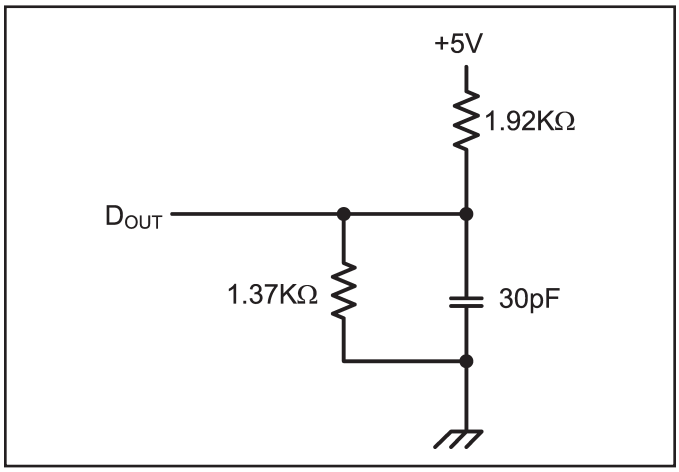
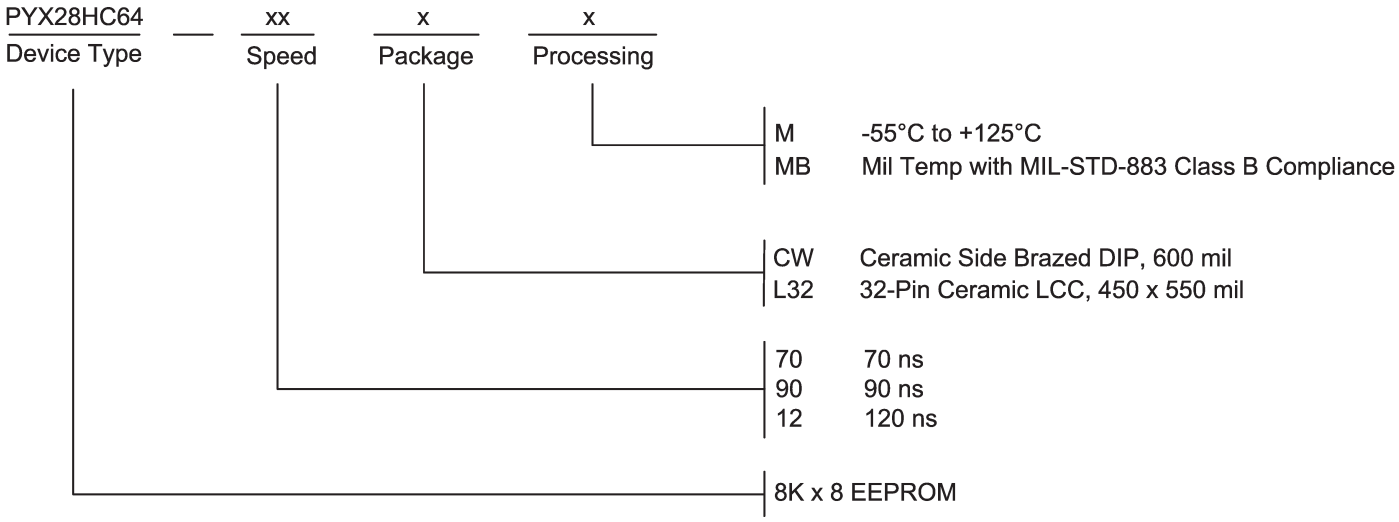


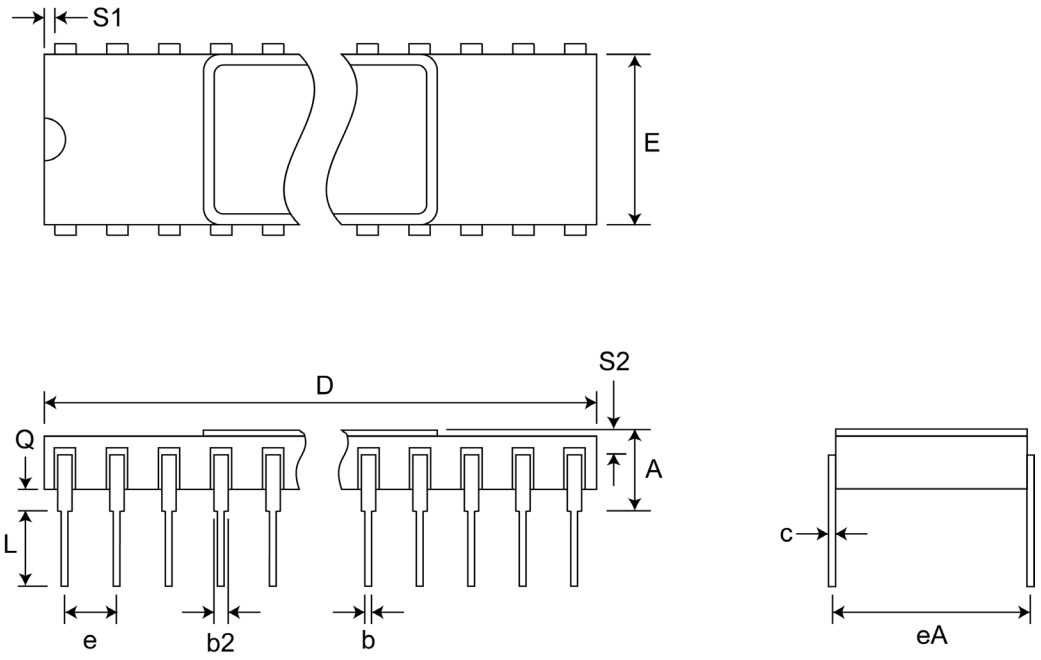
Figure 1. Output Load

ORDERING INFORMATION



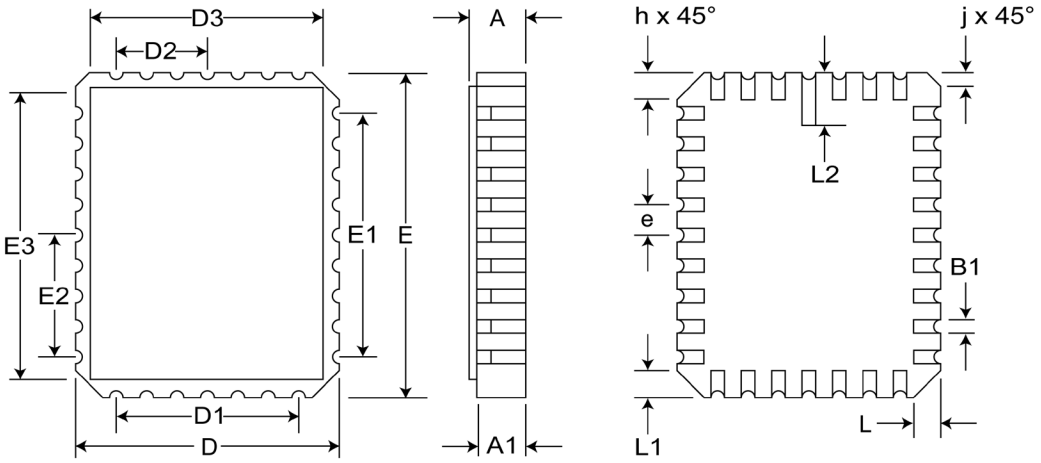
Pkg #	C5-1	
# Pins	28 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.232
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDE BRAZED DUAL IN-LINE PACKAGE (600 mils)



Pkg #	L6	
# Pins	32	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	

RECTANGULAR LEADLESS CHIP CARRIER



REVISIONS

DOCUMENT NUMBER	EEPROM107
DOCUMENT TITLE	PYX28HC64 - 8K x 8 EEPROM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Aug 2011	JDB	New Data Sheet