

### FEATURES

- Access Times of 150, 200, 250 and 350ns
- Single 5V±10% Power Supply
- Fast Byte Write (200µs or 1 ms)
- Low Power CMOS:
  - 60 mA Active Current
  - 150 µA Standby Current
- Fast Write Cycle Time -  $\overline{\text{DATA}}$  Polling
- CMOS & TTL Compatible Inputs and Outputs
- Endurance:
  - 10,000 Write Cycles
  - 100,000 Write Cycles (optional)
- Data Retention: 10 Years
- Available in the following package:
  - 24-Pin 600 mil Ceramic DIP
  - 32-Pin Ceramic LCC (450x550 mils)

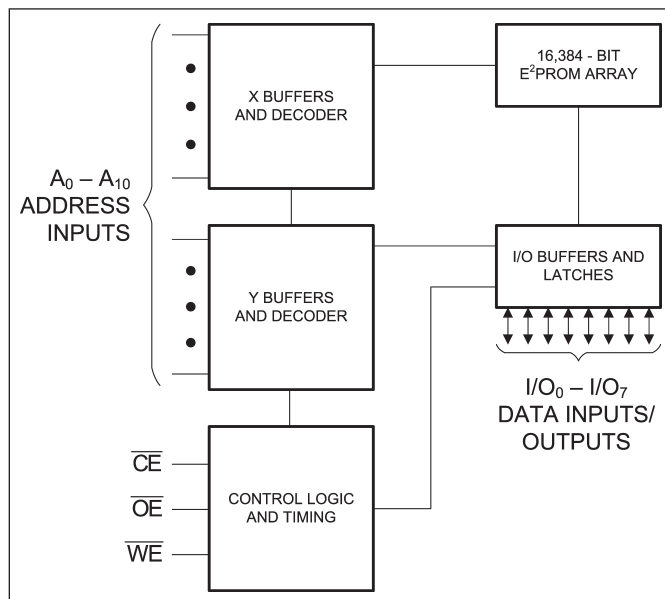


### DESCRIPTION

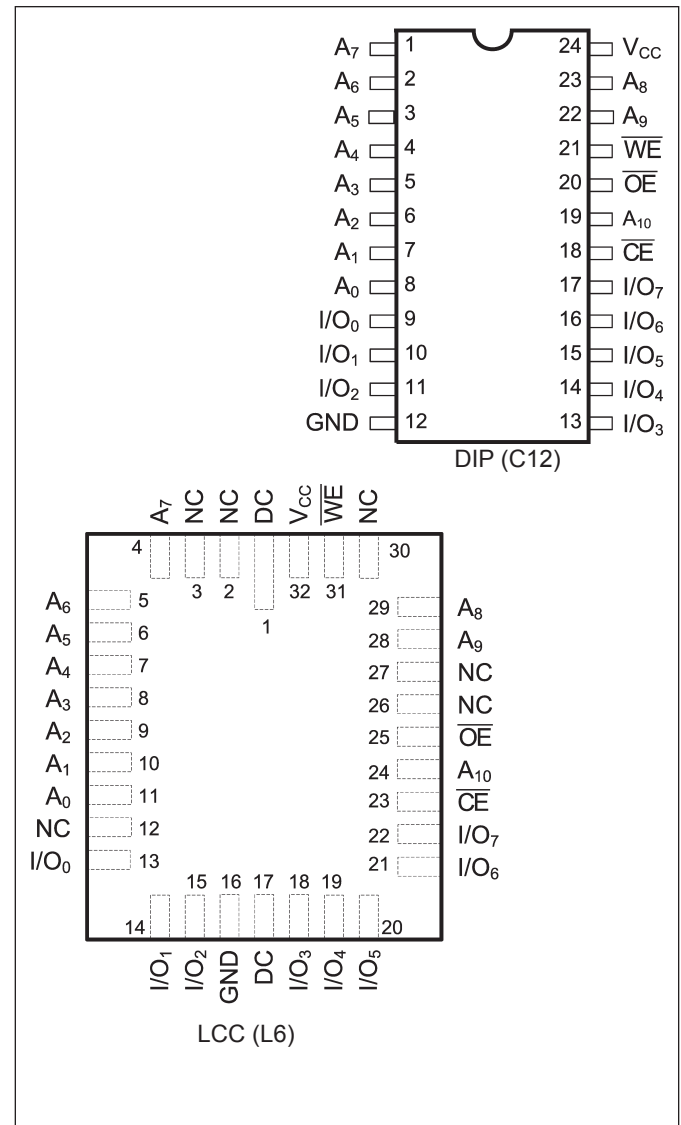
The PYA28C16 is a 5 Volt 2Kx8 EEPROM. The PYA28C16 is a 16K memory organized as 2,048 words by 8 bits. Data Retention is 10 Years. The device is available in a 24-Pin 600 mil wide Ceramic DIP and 32-Pin LCC.



### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATIONS





## OPERATION

### READ

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### BYTE WRITE

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The PYA28C16 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion.

### CHIP CLEAR

The contents of the entire memory of the PYA28C16 may be set to the high state by the CHIP CLEAR operation. By setting  $\overline{CE}$  low and  $\overline{OE}$  to 12 volts, the chip is cleared when a 10 msec low pulse is applied to  $\overline{WE}$ .

### DEVICE IDENTIFICATION

An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising  $A_9$  to  $12 \pm 0.5V$  and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

### $\overline{DATA}$ POLLING

The PYA28C16 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the PYA28C16, eliminating additional interrupts or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on  $I/O_7$  (i.e., write data=0xxx xxxx, read data=1xxx xxxx). Once the programming cycle is complete,  $I/O_7$  will reflect true data.

## MAXIMUM RATINGS<sup>(1)</sup>

Sym	Parameter	Value	Unit
$V_{CC}$	Power Supply Pin with Respect to GND	-0.3 to +6.25	V
$V_{TERM}$	Terminal Voltage with Respect to GND (up to 6.25V)	-0.5 to +6.25	V
$T_A$	Operating Temperature	-55 to +125	°C
$T_{BIAS}$	Temperature Under Bias	-55 to +125	°C
$T_{STG}$	Storage Temperature	-65 to +150	°C
$P_T$	Power Dissipation	1.0	W
$I_{OUT}$	DC Output Current	50	mA

## RECOMMENDED OPERATING CONDITIONS

Grade <sup>(2)</sup>	Ambient Temp	GND	$V_{CC}$
Military	-55°C to +125°C	0V	5.0V $\pm$ 10%

## CAPACITANCES<sup>(4)</sup>

( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ ,  $f = 1.0MHz$ )

Sym	Parameter	Conditions	Typ	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	10	pF



## DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)<sup>(2)</sup>

Sym	Parameter	Test Conditions	PYA28C16		Unit
			Min	Max	
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage		-0.5 <sup>(3)</sup>	0.8	V
V <sub>HC</sub>	CMOS Input High Voltage		V <sub>CC</sub> - 0.2	V <sub>CC</sub> + 0.5	V
V <sub>LC</sub>	CMOS Input Low Voltage		-0.5 <sup>(3)</sup>	0.2	V
V <sub>OL</sub>	Output Low Voltage (TTL Load)	I <sub>OL</sub> = +2.1 mA, V <sub>CC</sub> = Min		0.45	V
V <sub>OH</sub>	Output High Voltage (TTL Load)	I <sub>OH</sub> = -0.4 mA, V <sub>CC</sub> = Min	2.4		V
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max V <sub>IN</sub> = GND to V <sub>CC</sub>	-10	+10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max, $\overline{CE} = V_{IH}$ , V <sub>OUT</sub> = GND to V <sub>CC</sub>	-10	+10	μA
I <sub>SB</sub>	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$ , $\overline{OE} = V_{IL}$ , V <sub>CC</sub> = Max, f = Max, Outputs Open	—	5	mA
I <sub>SB1</sub>	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$ , V <sub>CC</sub> = Max, f = 0, Outputs Open, V <sub>IN</sub> ≤ V <sub>LC</sub> or V <sub>IN</sub> ≥ V <sub>HC</sub>	—	150	μA
I <sub>CC</sub>	Supply Current	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = Open, Inputs = V <sub>CC</sub> = 5.5V	—	60	mA

### Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V<sub>IL</sub> and I<sub>IL</sub> not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

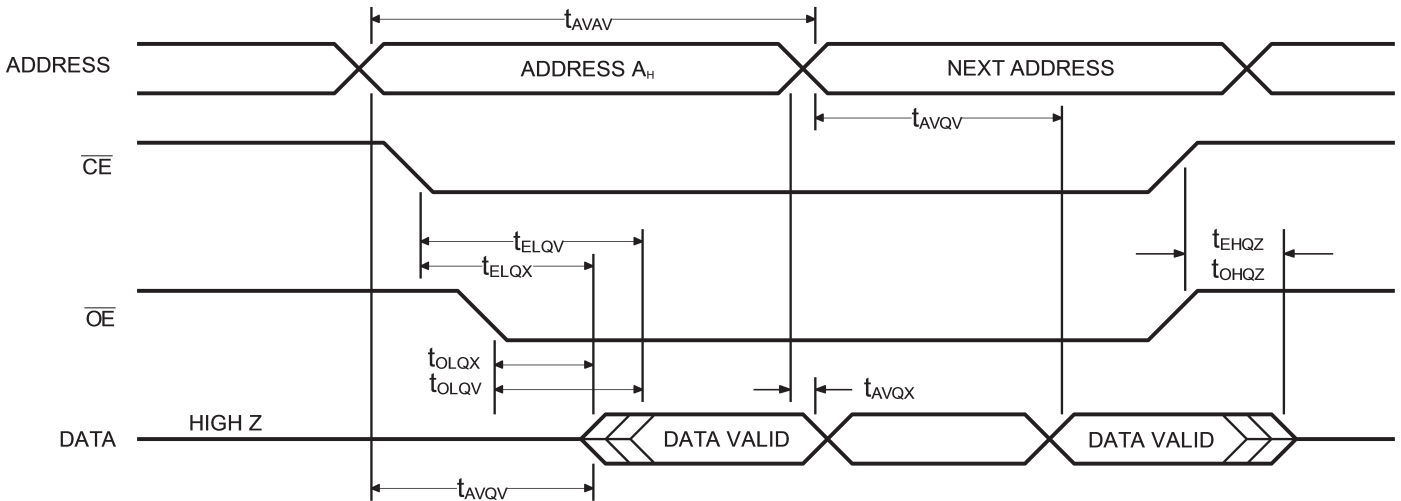


### AC ELECTRICAL CHARACTERISTICS—READ CYCLE

( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

Sym	Parameter	-150		-200		-250		-350		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{AVAV}$	Read Cycle Time	150		200		250		350		ns
$t_{AVQV}$	Address Access Time		150		200		250		350	ns
$t_{ELQV}$	Chip Enable Access Time		150		200		250		350	ns
$t_{OLQV}$	Output Enable Access Time		80		100		100		100	ns
$t_{ELQX}$	Chip Enable to Output in Low Z	0		0		0		0		ns
$t_{EHQZ}$	Chip Disable to Output in High Z		55		60		65		70	ns
$t_{OLQX}$	Output Enable to Output in Low Z	0		0		0		0		ns
$t_{OHQZ}$	Output Disable to Output in High Z		55		60		65		70	ns
$t_{AVQX}$	Output Hold from Address Change	0		0		0		0		ns

### TIMING WAVEFORM OF READ CYCLE



**AC CHARACTERISTICS—WRITE CYCLE** $(V_{CC} = 5V \pm 10\%, \text{ All Temperature Ranges})^{(2)}$ 

Symbol	Parameter	150 / 200 / 250 / 350		Unit
		Min	Max	
$t_{ELRH}$ $t_{WLRH}$	Write Cycle Time		1	ms
$t_{AVEL}$ $t_{AVWL}$	Address Setup Time	10		ns
$t_{ELAX}$ $t_{WLAX}$	Address Hold Time	50		ns
$t_{WLEL}$	Write Setup Time	0		ns
$t_{WHEH}$	Write Hold Time	0		ns
$t_{OHEL}$ $t_{OHWL}$	$\overline{OE}$ Setup Time	10		ns
$t_{WHOL}$ $t_{EHOL2}$	$\overline{OE}$ Hold Time	10		ns
$t_{ELEH}$ $t_{WLWH}$	$\overline{WE}$ Pulse Width	100	1000	ns
$t_{DVEH}$ $t_{DVWH}$	Data Setup Time	50		ns
$t_{EHDX}$ $t_{WHDX}$	Data Hold Time	10		ns
$t_{ELWL}$	$\overline{CE}$ Setup Time	0		ns
$t_{EHWH}$	$\overline{CE}$ Hold Time	0		ns
$t_{EHRL}$ $t_{WHRL}$	Time to device busy		50	ns





### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figure 1

### TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	D <sub>OUT</sub>
Write	L	H	L	D <sub>IN</sub>
Write Inhibit	X	L	X	—
Write Inhibit	X	X	H	—
Standby	H	X	X	High Z
Output Disable	X	H	X	High Z

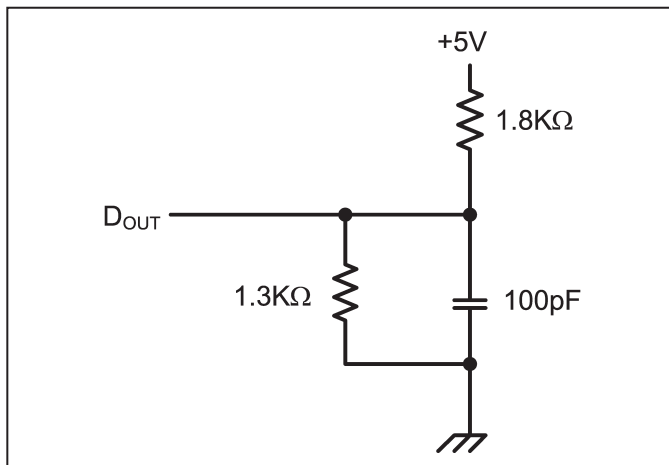
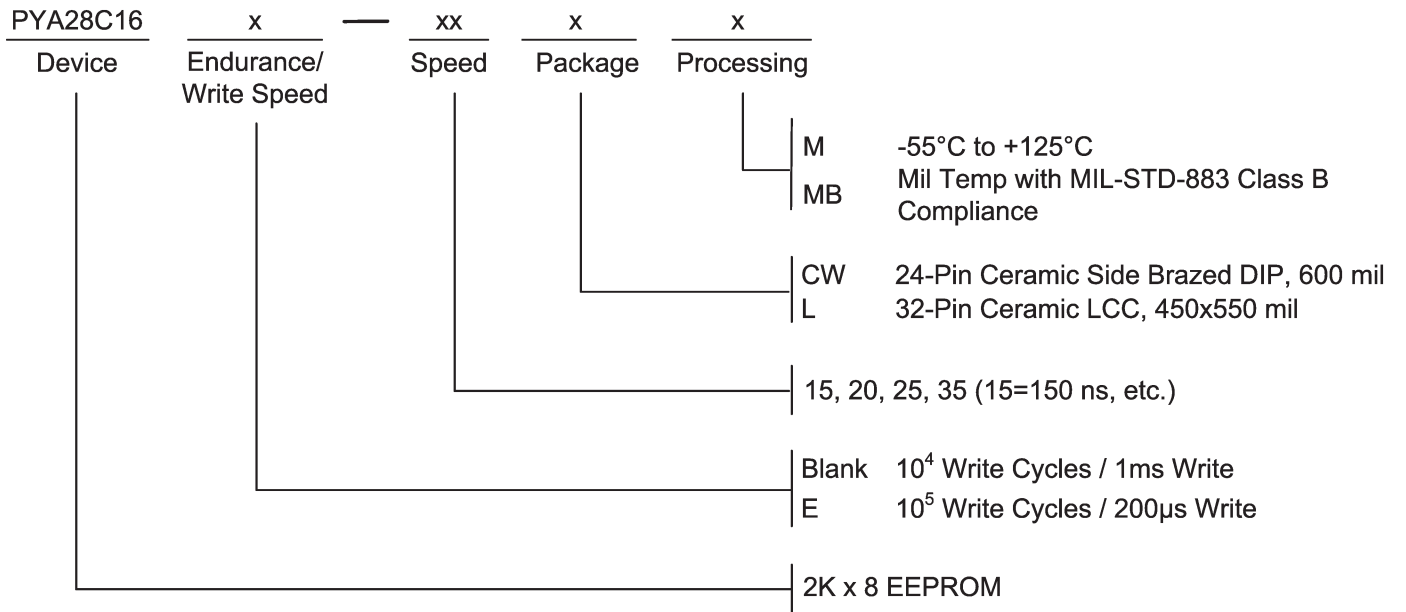


Figure 1. Output Load



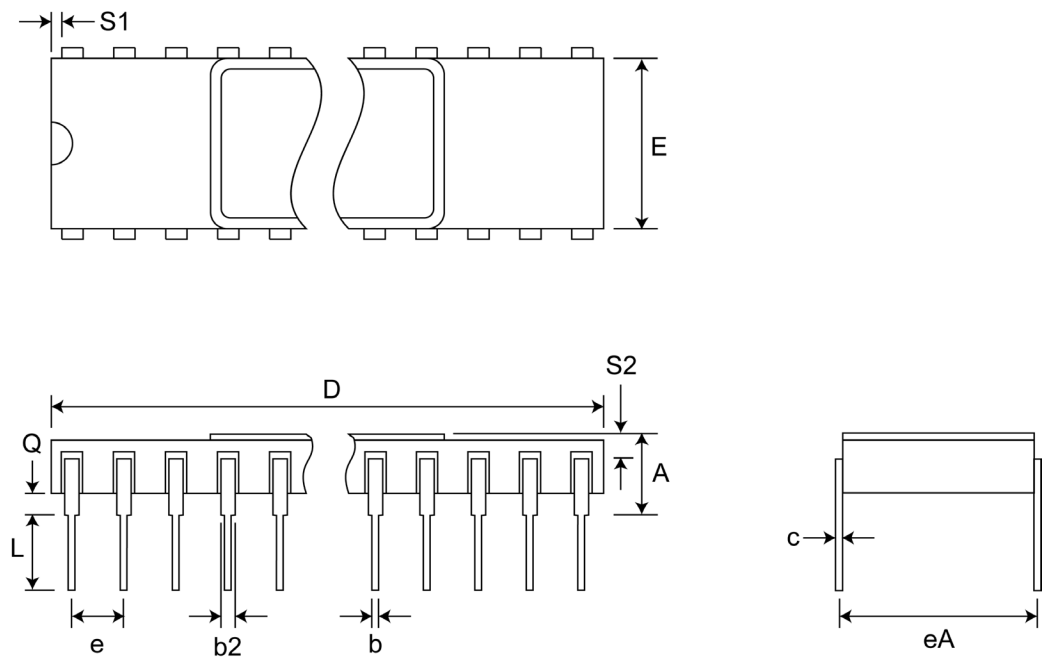
## ORDERING INFORMATION





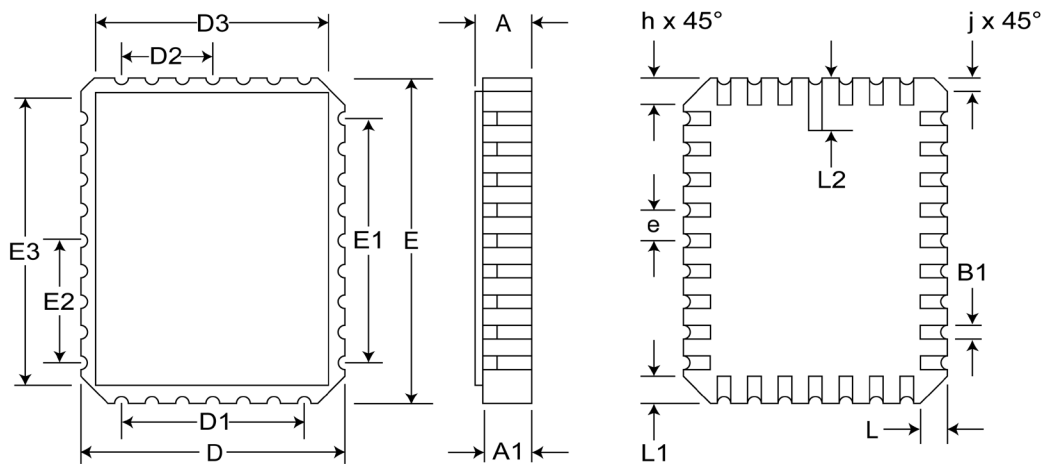
Pkg #	<b>C12-1</b>	
# Pins	24 (600 mil)	
Symbol	<b>Min</b>	<b>Max</b>
A	-	0.232
b	0.014	0.022
b2	0.045	0.065
C	0.008	0.014
D	-	1.290
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

**SIDE BRAZED DUAL IN-LINE PACKAGE (600 mils)**



Pkg #	<b>L6</b>	
# Pins	32	
Symbol	<b>Min</b>	<b>Max</b>
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	

**RECTANGULAR LEADLESS CHIP CARRIER**



**REVISIONS**

<b>DOCUMENT NUMBER</b>	EEPROM108
<b>DOCUMENT TITLE</b>	PYA28C16 - 2K x 8 EEPROM

<b>REV</b>	<b>ISSUE DATE</b>	<b>ORIGINATOR</b>	<b>DESCRIPTION OF CHANGE</b>
OR	Jun 2012	JDB	New Data Sheet
A	Jul 2012	JDB	Tightened package definition for 600-Mil Sidebrazed DIP