P4C1023/P4C1023L LOW POWER 128K x 8 SINGLE CHIP ENABLE CMOS STATIC RAM

FEATURES

- **V_{CC} Current**
  — Operating: 35mA
  — CMOS Standby: 100µA
- **Access Times**
  —55/70 ns
- **Single 5 Volts ±10% Power Supply**
- **Easy Memory Expansion Using $\overline{CE}$ and $\overline{OE}$ Inputs**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Automatic Power Down**
- **Packages**
  —32-Pin 400 or 600 mil Ceramic DIP
  —32-Pin Ceramic SOJ

DESCRIPTION

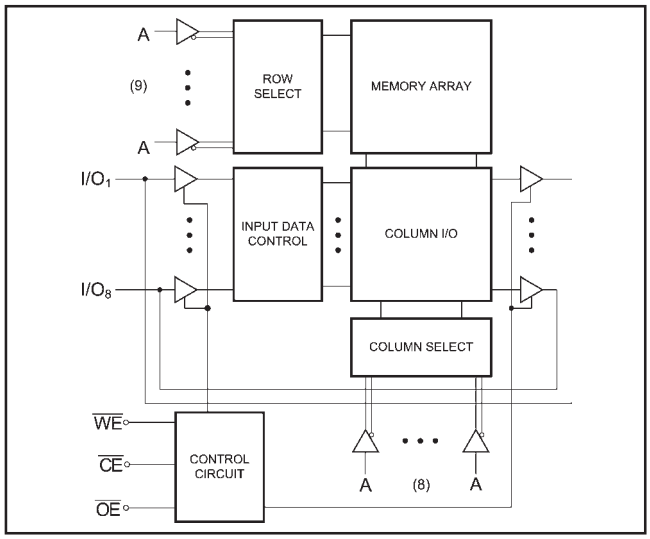
The P4C1023L is a 1 Megabit low power CMOS static RAM organized as 128K x 8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

Access times of 55 ns and 70 ns are availale. CMOS is utilized to reduce power consumption to a low level.

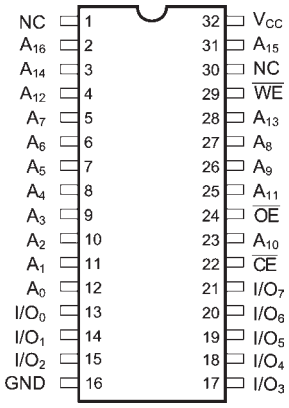
The P4C1023L device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{16}. Reading is accomplished by device selection ($\overline{CE}$ low) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}$ is HIGH or $\overline{WE}$ is LOW.

The P4C1023L is packaged in a 32-pin 400 or 600 mil ceramic DIP and in a 32-pin ceramic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP (C10, C11), CERAMIC SOJ (CJ1)
TOP VIEW

RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

Temperature Range (Ambient)	Supply Voltage
Commercial (0°C to 70°C)	$4.5V \le V_{CC} \le 5.5V$
Industrial (-40°C to 85°C)	$4.5V \le V_{CC} \le 5.5V$
Military (-55°C to 125°C)	$4.5V \le V_{CC} \le 5.5V$

MAXIMUM RATINGS

Stresses greater than those listed can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Maximum Ratings for extended periods can adversely affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage with Respect to GND	-0.5	7.0	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5	V_{CC} + 0.5	V
T_A	Operating Ambient Temperature	-55	125	°C
S_{TG}	Storage Temperature	-65	150	°C
I_{OUT}	Output Current into Low Outputs		25	mA
I_{LAT}	Latch-up Current	>200		mA

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	Output High Voltage (I/O_0 - I/O_7)	I_{OH} = –1mA, V_{CC} = 4.5V	2.4		V
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 2.1mA		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{LI}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$ Comm. Industrial Military	-2 -5 -10	+2 +5 +10	µA
I_{LO}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$ Comm. $\overline{CE}_1 \ge V_{IH}$ or $CE_2 \le V_{IL}$ Industrial Military	-2 -5 -10	+2 +5 +10	µA
I_{SB}	V_{CC} Current TTL Standby Current (TTL Input Levels)	V_{CC} = 5.5V, I_{OUT} = 0 mA $\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$		3	mA
I_{SB1}	V_{CC} Current CMOS Standby Current (CMOS Input Levels)	V_{CC} = 5.5V, I_{OUT} = 0 mA $\overline{CE}_1 \ge V_{CC}$-0.2V, $CE_2 \le 0.2V$		100	µA

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	pF

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	Note 1		Unit
			-55	-70	
I_{CC}	Dynamic Operating Current	Commercial	20	20	mA
		Industrial	25	25	
		Military	35	35	

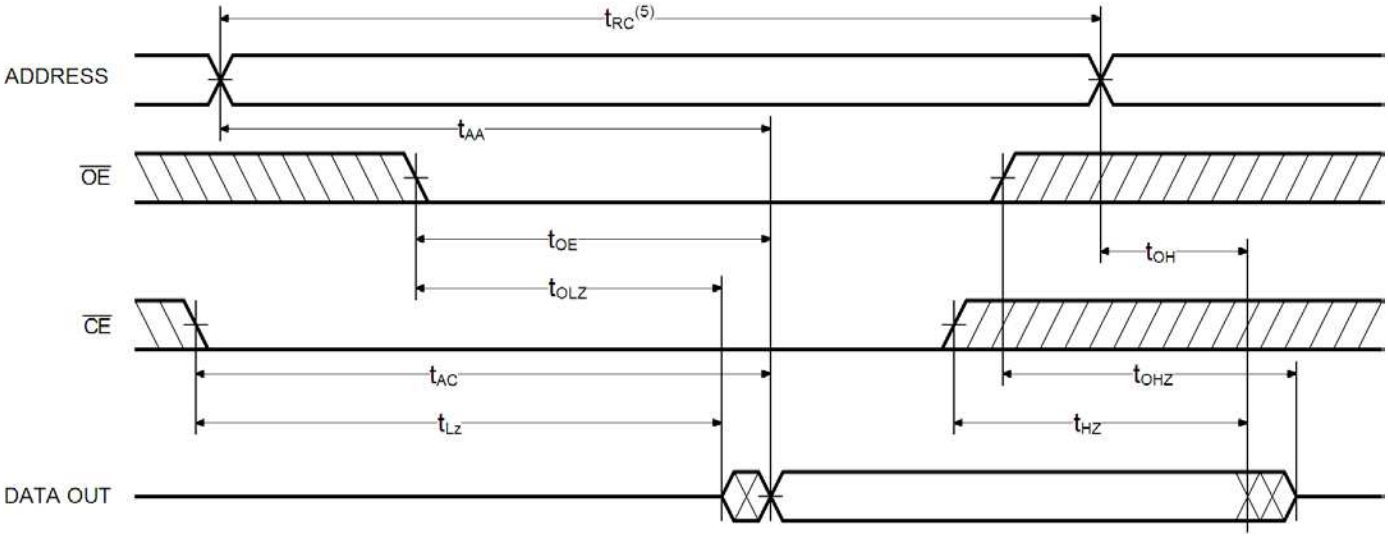
Note 1 - Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $CE_2 \geq V_{IH}$ (min), $\overline{CE_1}$ and $\overline{WE} \leq V_{IL}$ (max), $\overline{OE}$ is high. Switching inputs are 0V and 3V.

AC ELECTRICAL CHARACTERISTICS - READ CYCLE

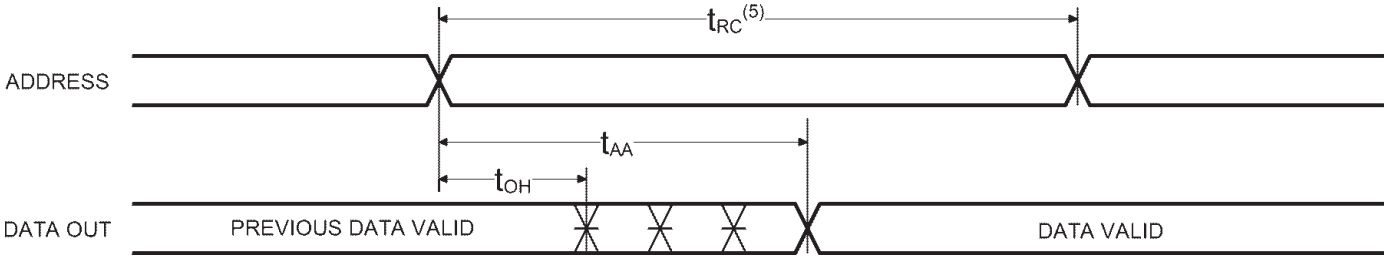
(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-55		-70		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address Access Time		55		70	ns
t_{AC}	Chip Enable Access Time		55		70	ns
t_{OH}	Output Hold from Address Change	5		5		ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		ns
t_{HZ}	Chip Disable to Output in High Z		20		25	ns
t_{OE}	Output Enable Low to Data Valid		30		35	ns
t_{OLZ}	Output Enable Low to Low Z	5		5		ns
t_{OHZ}	Output Enable High to High Z		20		25	ns
t_{PU}	Chip Enable to Power Up Time	0		0		ns
t_{PD}	Chip Disable to Power Down Time		55		70	ns

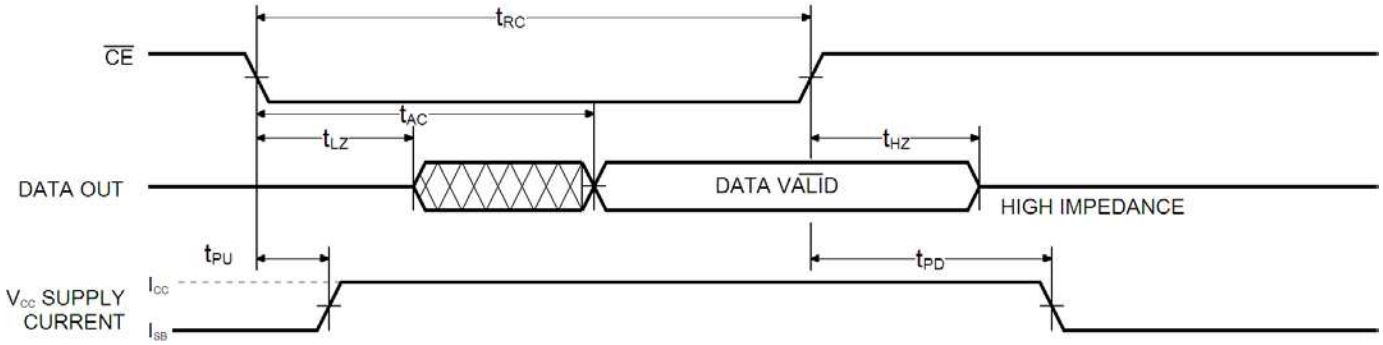
READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[1]



READ CYCLE NO. 2 (ADDRESS CONTROLLED)



READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)



Notes:

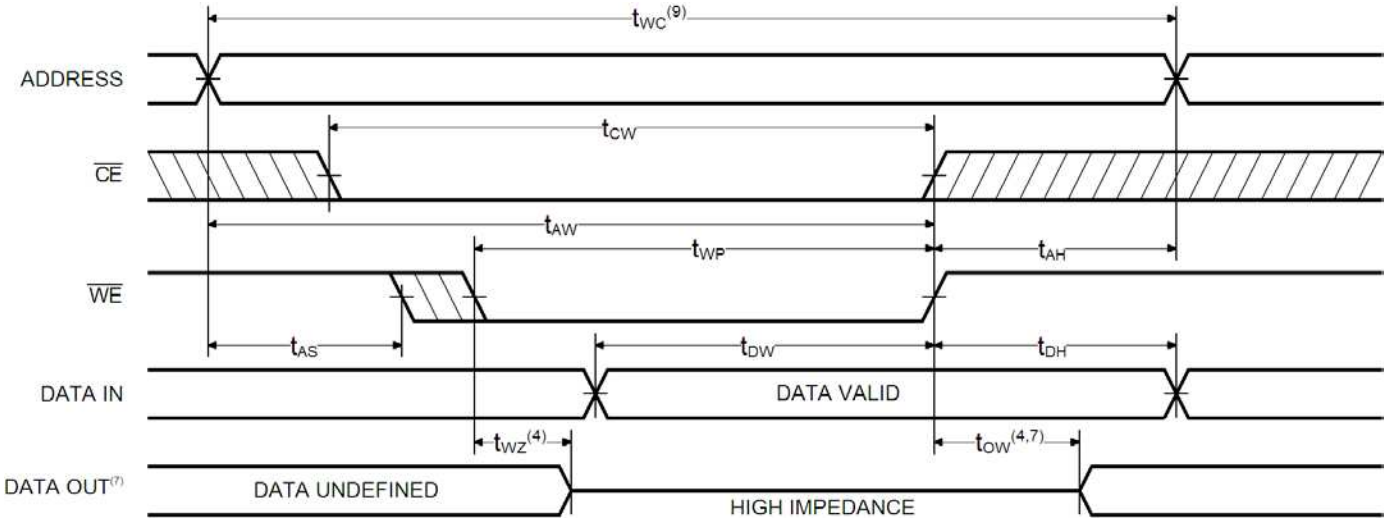
1. $\overline{WE}$ is HIGH for READ cycle.
2. $\overline{CE}$ and $\overline{OE}$ are LOW for READ cycle.
3. ADDRESS must be valid prior to, or coincident with later of $\overline{CE}$ transition LOW.
4. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
5. READ Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS - WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-55		-70		Unit
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	55		70		ns
t_{CW}	Chip Enable Time to End of Write	50		60		ns
t_{AW}	Address Valid to End of Write	50		60		ns
t_{AS}	Address Set-up Time	0		0		ns
t_{WP}	Write Pulse Width	40		50		ns
t_{AH}	Address Hold Time	0		0		ns
t_{DW}	Data Valid to End of Write	25		30		ns
t_{DH}	Data Hold Time	0		0		ns
t_{WZ}	Write Enable to Output in High Z		25		30	ns
t_{OW}	Output Active from End of Write	5		5		ns

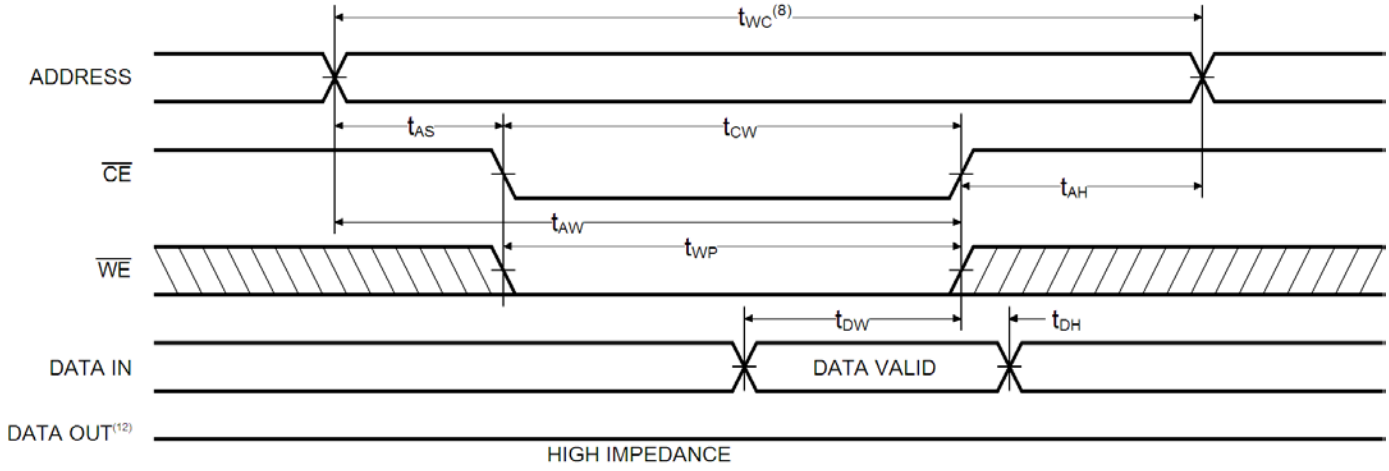
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[6]



Notes:

6. $\overline{CE}$ and $\overline{WE}$ are LOW for WRITE cycle.
7. $\overline{OE}$ is LOW for this WRITE cycle to show twz and tow.
8. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CE}$ CONTROLLED)[6]

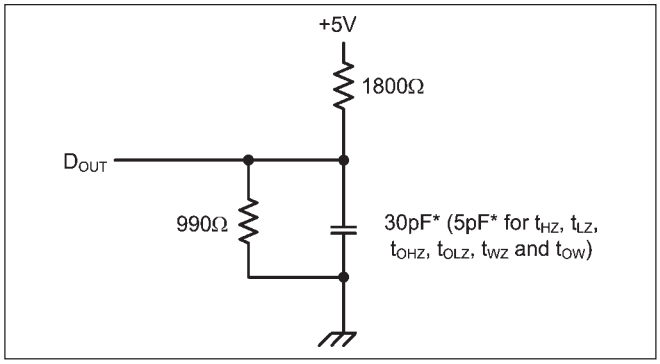


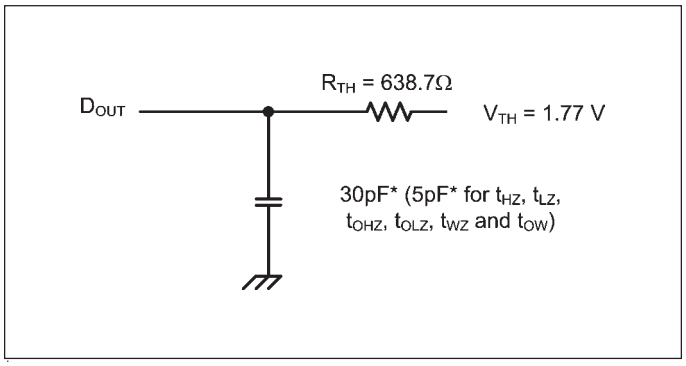
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	High Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active





* including scope and test fixture.

Note:
Because of the high speed of the P4C1023L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground.

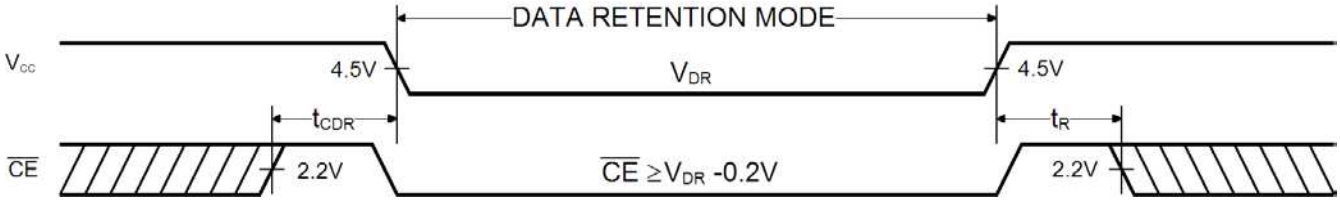
To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.77V (Thevenin Voltage) at the comparator input, and a 589Ω resistor must be used in series with D_{OUT} to match 639Ω (Thevenin Resistance).

DATA RETENTION

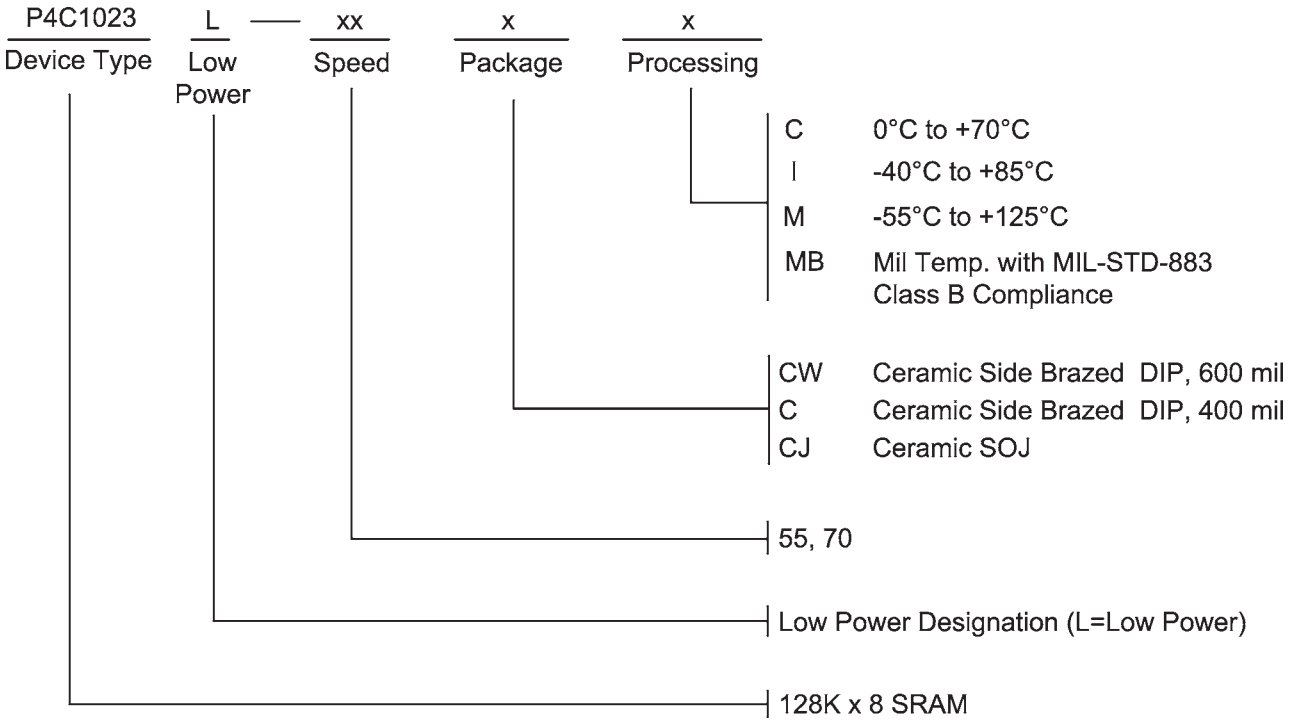
Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CE} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$	2.0	5.5	V
I_{CCDR}	Data Retention Current	V_{DR} = 2.0V		50	µA
		V_{DR} = 3.0V		100	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns
t_R	Operating Recovery Time		t_{RC}		ns

1. $\overline{CE_1} \geq V_{DR}$ -0.2V, $CE_2 \geq V_{DR}$ -0.2V or $CE_2 \leq 0.2V$; or $\overline{CE_1} \leq 0.2V$, CE_2 - 0.2V; $V_{IN} \geq V_{DR}$ -0.2V or $V_{IN} \leq 0.2V$

LOW V_{CC} DATA RETENTION WAVEFORM



ORDERING INFORMATION



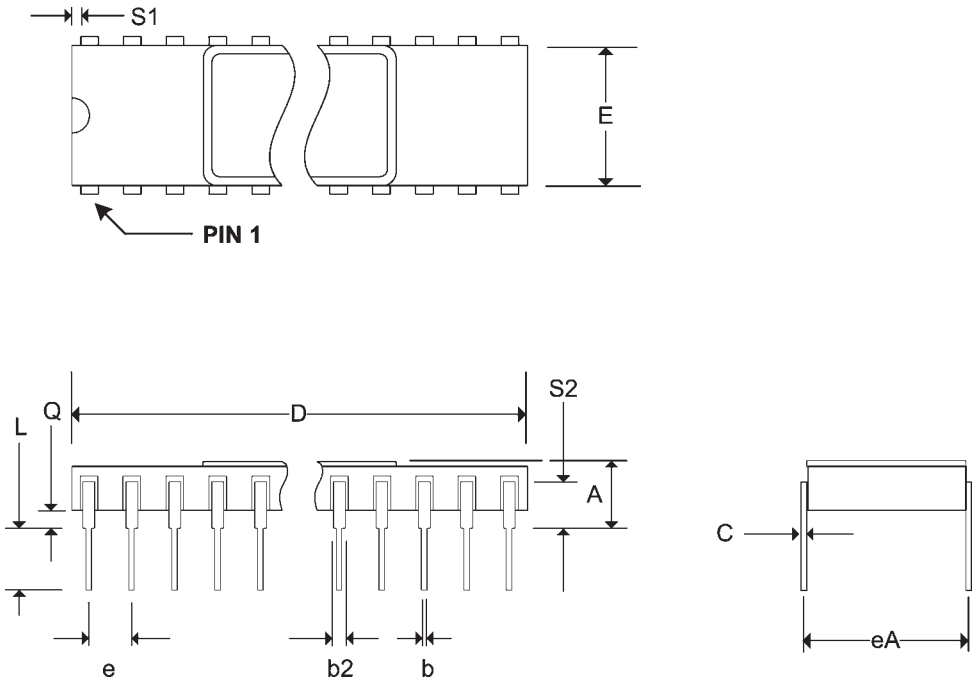
SELECTION GUIDE

The P4C1023L is available in the following temperature, speed and package options.

Temperature Range	Package	Speed (ns)	
		55	70
Commercial	Side Brazed DIP (400 mil)	-55CC	-70CC
	Side Brazed DIP (600 mil)	-55CWC	-70CWC
	Ceramic SOJ	-55CJC	-70CJC
Industrial	Side Brazed DIP (400 mil)	-55CI	-70CI
	Side Brazed DIP (600 mil)	-55CWI	-70CWI
	Ceramic SOJ	-55CJI	-70CJI
Military Temperature	Side Brazed DIP (400 mil)	-55CM	-70CM
	Side Brazed DIP (600 mil)	-55CWM	-70CWM
	Ceramic SOJ	-55CJM	-70CJM
Military Processed*	Side Brazed DIP (400 mil)	-55CMB	-70CMB
	Side Brazed DIP (600 mil)	-55CWMB	-70CWMB
	Ceramic SOJ	-55CJMB	-70CJMB

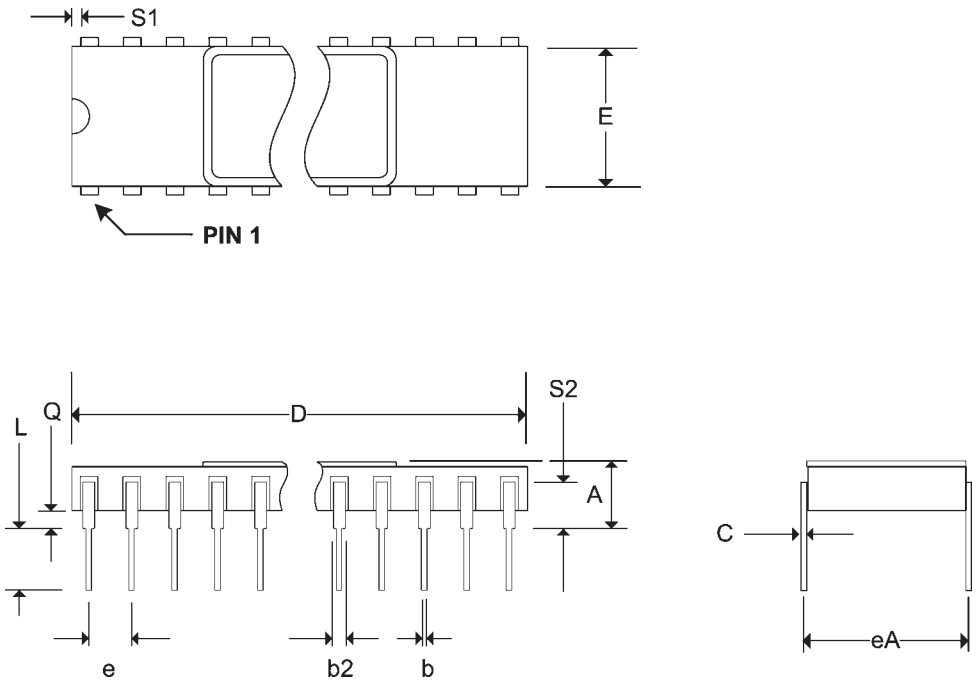
Pkg #	C11	
# Pins	32 (400 mil)	
Symbol	**Min**	**Max**
A	-	0.232
b	0.014	0.023
b2	0.038	0.065
C	0.008	0.018
D	-	1.700
E	0.350	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



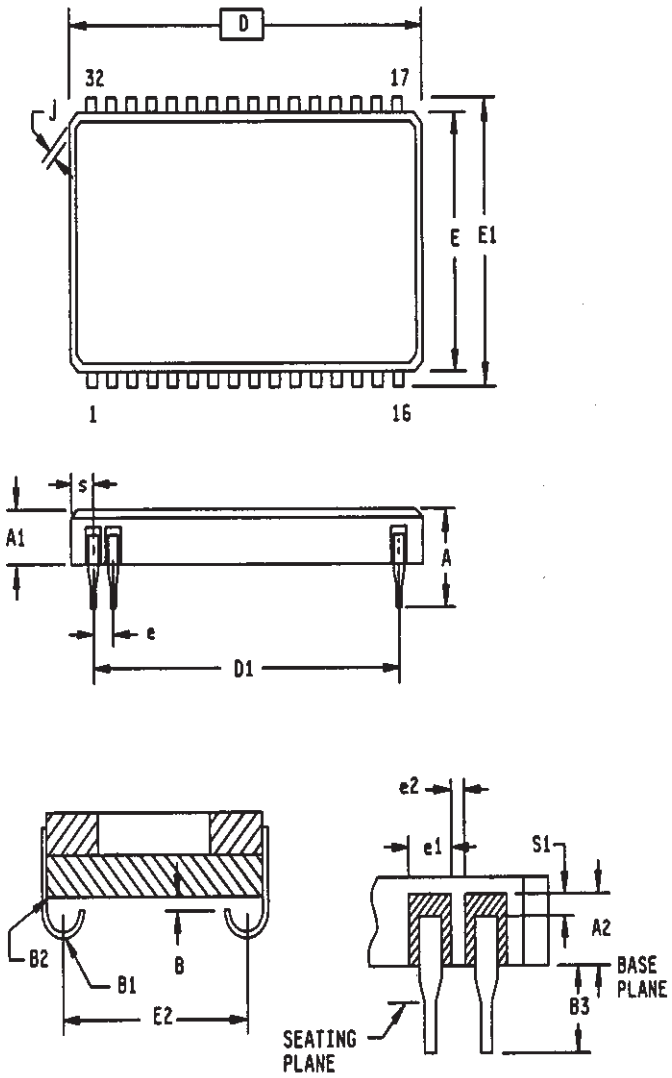
Pkg #	C10	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.680
E	0.510	0.620
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



Pkg #	CJ1	
# Pins	32	
Symbol	**Min**	**Max**
A	0.120	0.165
A1	0.088	0.120
A2	0.070	REF
B	0.010	REF
B1	0.030R	TYP
B2	0.020	REF
B3	0.025	0.045
D	0.816	0.838
D1	0.750	REF
E	0.419	0.431
E1	0.430	0.445
E2	0.360	0.380
e	0.050 BSC	
e1	0.038	TYP
e2	0.005	
j	0.005	TYP
S	0.030	0.040
S1	0.020	TYP

CERAMIC SOJ SMALL OUTLINE IC PACKAGE



REVISIONS

DOCUMENT NUMBER: SRAM126
DOCUMENT TITLE: P4C1023 / P4C1023L LOW POWER 128K x 8 SINGLE CHIP ENABLE CMOS STATIC RAM

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
OR	Oct-05	JDB	New Data Sheet