

FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
 - 12/15/20/25 ns (Commercial)
 - 15/20/25/35 ns (Industrial)
 - 20/25/35/45 ns (Military)
- Low Power Operation
- 5V ± 10% Power Supply
- Separate Inputs and Outputs
 - P4C1281 Input Data at Outputs during Write
 - P4C1282 Outputs in High Z during Write
- Fully TTL Compatible Inputs and Outputs
- Standard Pinout (JEDEC Approved)
 - 28-Pin 300 mil DIP, SOJ
 - 28-Pin 350 x 550 mil LCC

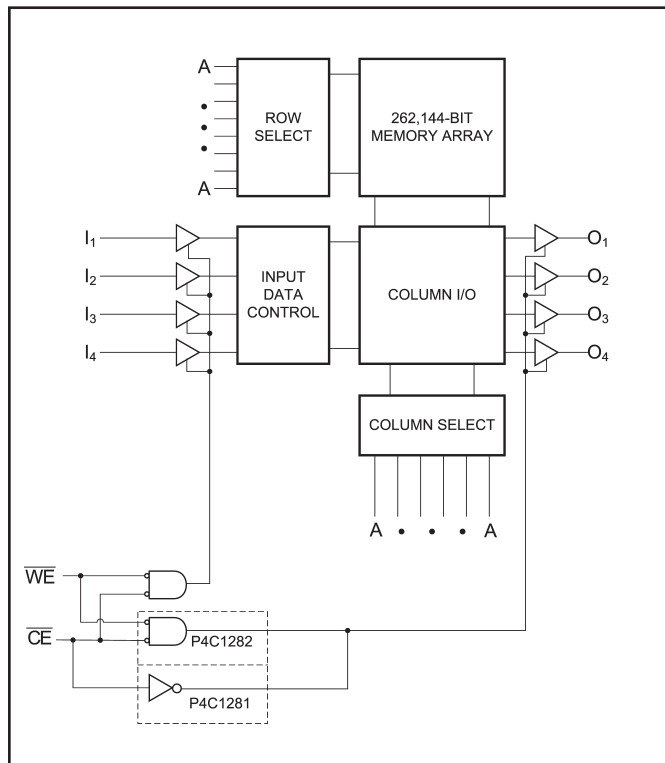
DESCRIPTION

The P4C1281 and P4C1282 are 262,144-bit (64Kx4) ultra high-speed static RAMs similar to the P4C1258, but with separate data I/O pins. The P4C1281 features a transparent write operation; the outputs of the P4C1282 are in high impedance during the write cycle. The RAMs operate from a single 5V ± 10% tolerance power supply.

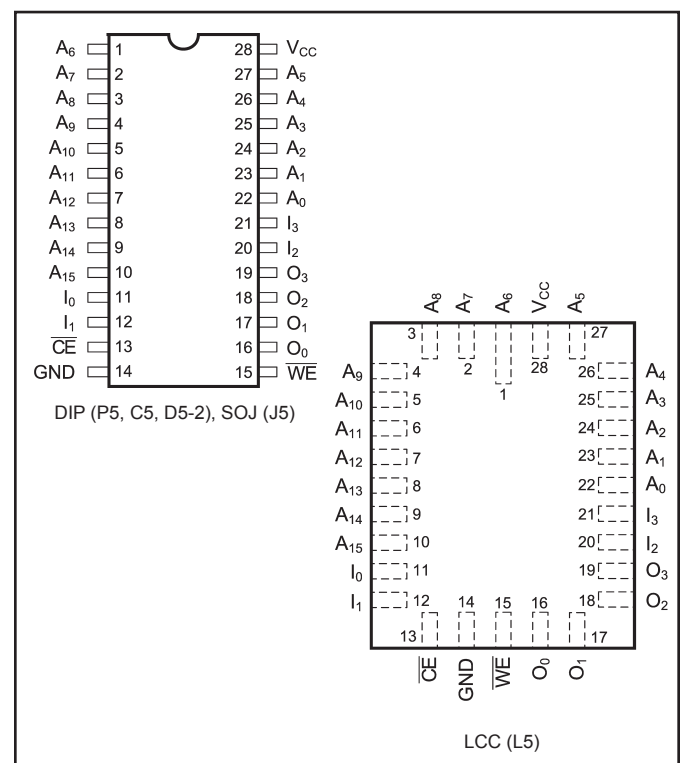
Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption.

The P4C1281 and P4C1282 are available in 28-pin 300 mil DIP and SOJ, and a 28-pin 350x550 mil LCC providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





MAXIMUM RATINGS⁽¹⁾

Sym	Parameter	Value	Unit
V _{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V _{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V _{CC} + 0.5	V
T _A	Operating Temperature	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade ⁽²⁾	Ambient Temp	GND	V _{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES⁽⁴⁾

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	10	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)⁽²⁾

Sym	Parameter	Test Conditions	P4C1281/1282		Unit	
			Min	Max		
V _{IH}	Input High Voltage		2.2	V _{CC} + 0.5	V	
V _{IL}	Input Low Voltage		-0.5 ⁽³⁾	0.8	V	
V _{HC}	CMOS Input High Voltage		V _{CC} - 0.2	V _{CC} + 0.5	V	
V _{LC}	CMOS Input Low Voltage		-0.5 ⁽³⁾	0.2	V	
V _{CD}	Input Clamp Diode Voltage	V _{CC} = Min, I _{IN} = -18 mA		-1.2	V	
V _{OL}	Output Low Voltage (TTL Load)	I _{OL} = +8 mA, V _{CC} = Min		0.4	V	
V _{OH}	Output High Voltage (TTL Load)	I _{OH} = -4 mA, V _{CC} = Min	2.4		V	
I _{LI}	Input Leakage Current	V _{CC} = Max, V _{IN} = GND to V _{CC}	MIL	-10	+10	µA
			IND/COM	-5	+5	
I _{LO}	Output Leakage Current	V _{CC} = Max, $\overline{CE} = V_{IH}$, V _{OUT} = GND to V _{CC}	MIL	-10	+10	µA
			IND/COM	-5	+5	
I _{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$, V _{CC} = Max, f = Max, Outputs Open	MIL	—	40	mA
			IND/COM	—	35	
I _{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$, V _{CC} = Max, f = 0, Outputs Open V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC}	MIL	—	20	mA
			IND/COM	—	15	

N/A = Not applicable

**POWER DISSIPATION CHARACTERISTICS VS. SPEED**

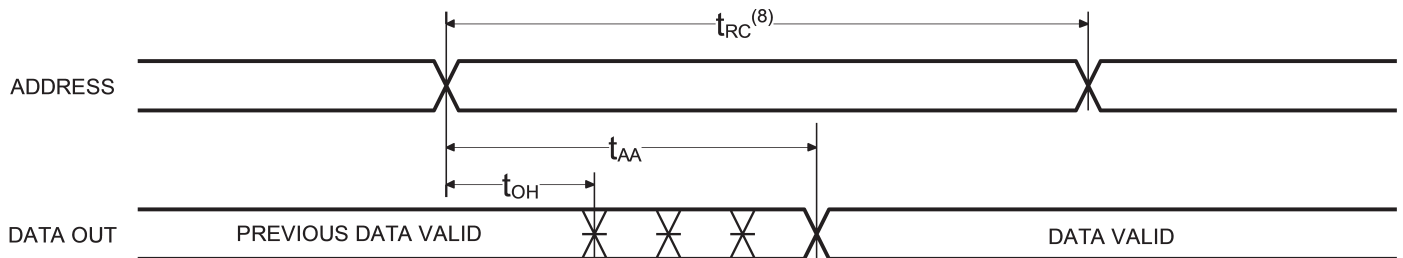
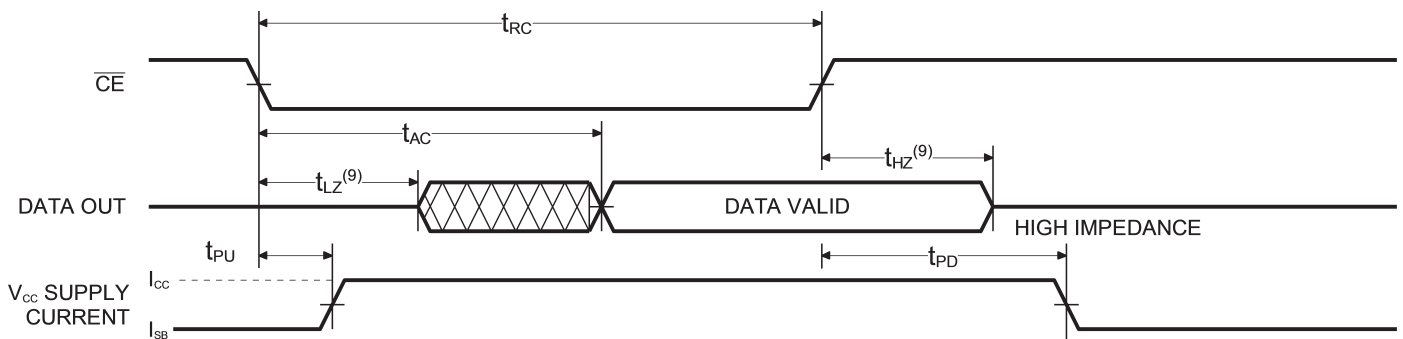
Sym	Parameter	Temperature Range	-12	-15	-20	-25	-35	-45	Unit
I_{CC}	Dynamic Operating Current*	Commercial	170	160	155	150	N/A	N/A	mA
		Industrial	N/A	170	160	155	150	N/A	mA
		Military	N/A	N/A	160	155	150	145	mA

* $V_{CC} = 5.5V$. Tested with outputs open. $f = \text{Max}$. Switching inputs are 0V and 3V. $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Sym	Parameter	-12		-15		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address Access Time		12		15		20		25		35		45	ns
t_{AC}	Chip Enable Access Time		12		15		20		25		35		45	ns
t_{OH}	Output Hold from Address Change	2		2		2		2		2		2		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		2		2		ns
t_{HZ}	Chip Disable to Output in High Z		7		8		10		10		15		15	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down		12		15		20		25		25		30	ns

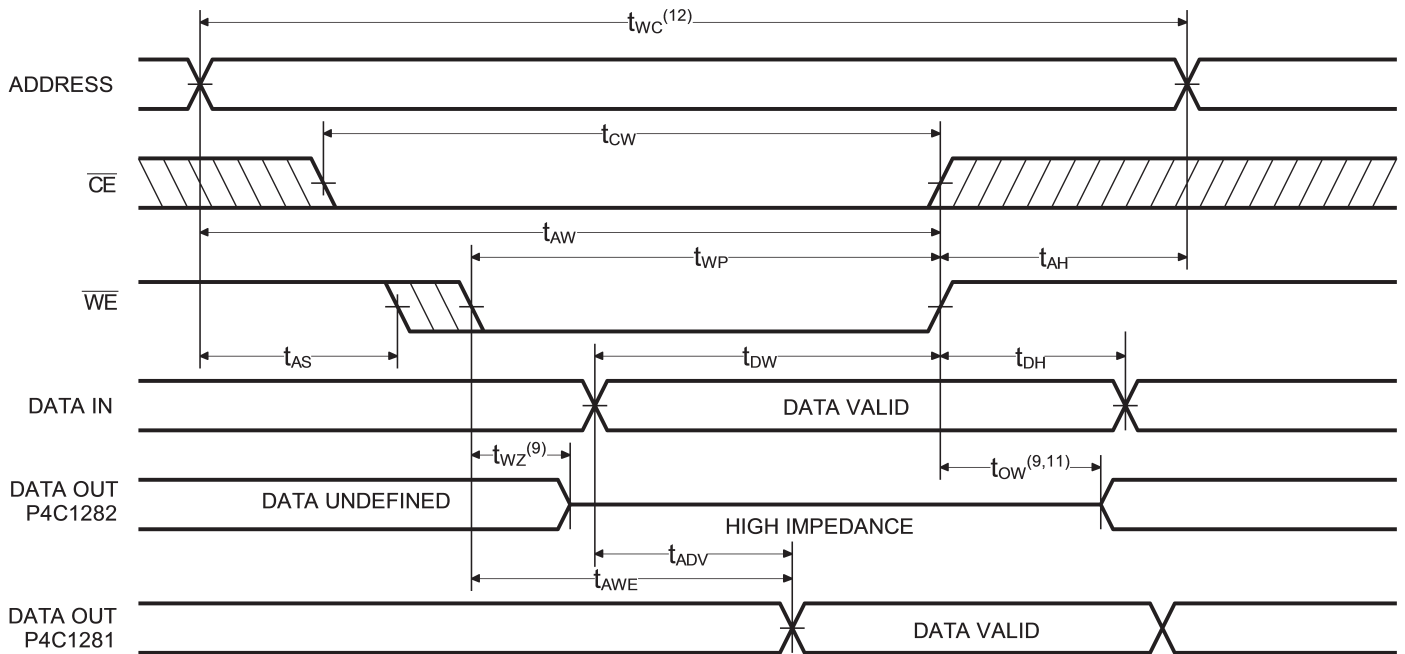
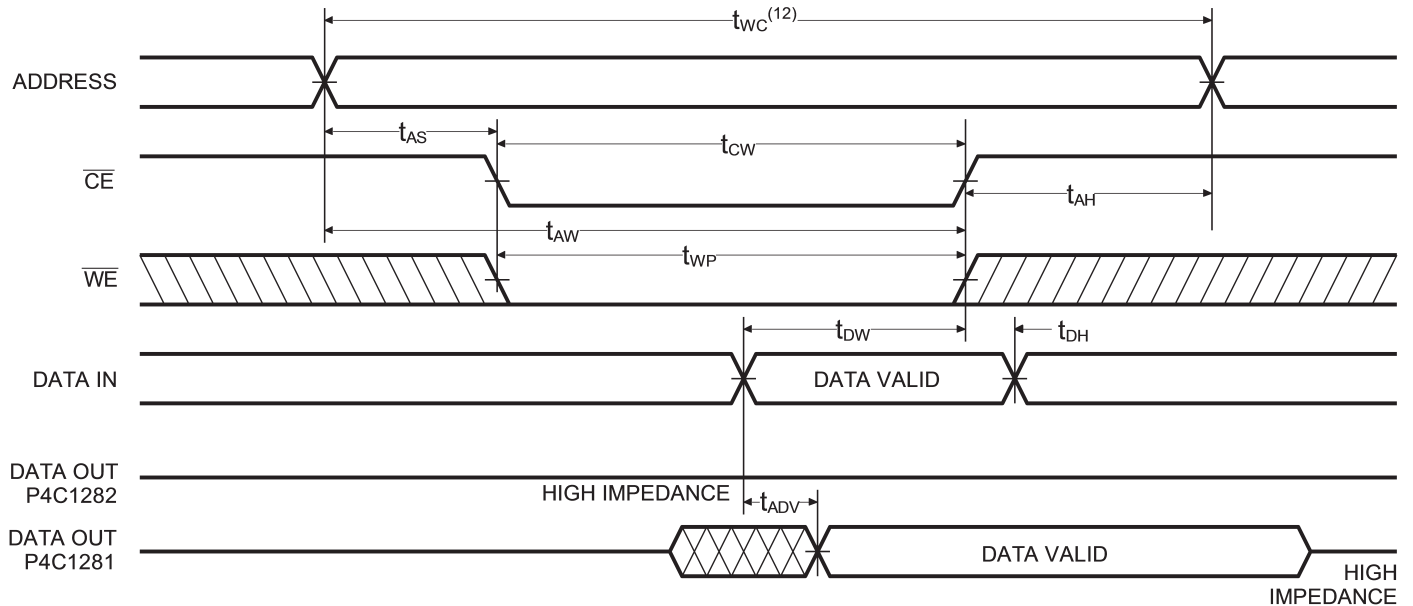
TIMING WAVEFORM OF READ CYCLE NO. 1 (ADDRESS CONTROLLED) ^(5,6)**TIMING WAVEFORM OF READ CYCLE NO. 2 (\overline{CE} CONTROLLED)** ^(5,7,8)

**AC CHARACTERISTICS—WRITE CYCLE** $(V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Sym	Parameter	-12		-15		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12		13		15		20		30		40		ns
t_{CW}	Chip Enable Time to End of Write	8		10		15		20		30		35		ns
t_{AW}	Address Valid to End of Write	8		10		15		20		25		35		ns
t_{AS}	Address Setup Time	0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	9		10		15		20		25		35		ns
t_{AH}	Address Hold Time from End of Write	0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	6		7		10		13		15		20		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		6		7		8		10		10		15	ns
t_{OW}	Output Active from End of Write	2		2		2		2		2		2		ns
t_{AWE}	Write Enable to Data-out Valid (P4C1281)		12		13		18		20		30		35	ns
t_{ADV}	Data-in Valid to Data-out Valid (P4C1281)		12		13		18		20		30		35	ns

Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_L and I_L not more negative than $-3.0V$ and $-100mA$, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.
- \overline{WE} is HIGH for READ cycle.
- \overline{CE} is LOW for READ cycle.
- ADDRESS must be valid prior to, or coincident with \overline{CE} transition LOW.
- Read Cycle Time is measured from the last valid address to the first transitioning address.
- Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED) (10, 11, 12)****TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CE} CONTROLLED) (10, 11, 12)****Notes:**

10. \overline{CE} and \overline{WE} must be LOW for WRITE cycle.
11. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high impedance state

12. Write Cycle Time is measured from the last valid address to the first transitioning address.



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE P4C1281 (P4C1282)

Mode	\overline{CE}	\overline{WE}	I/O	Power
Standby	H	X	High Z	Standby
Read	L	H	D _{OUT}	Active
Write	L	L	D _{IN} (High Z)	Active

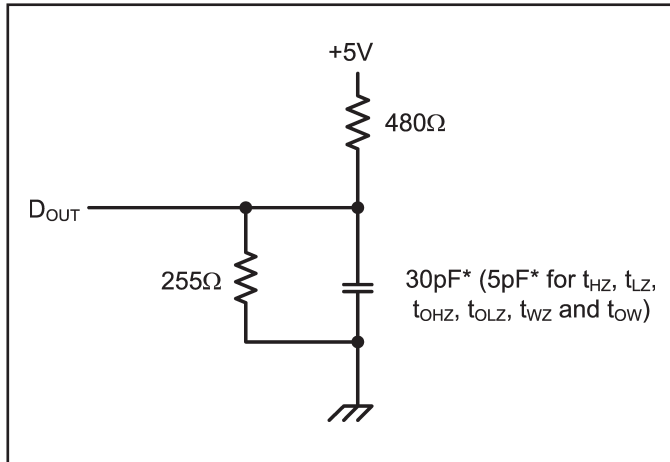


Figure 1. Output Load

* including scope and test fixture.

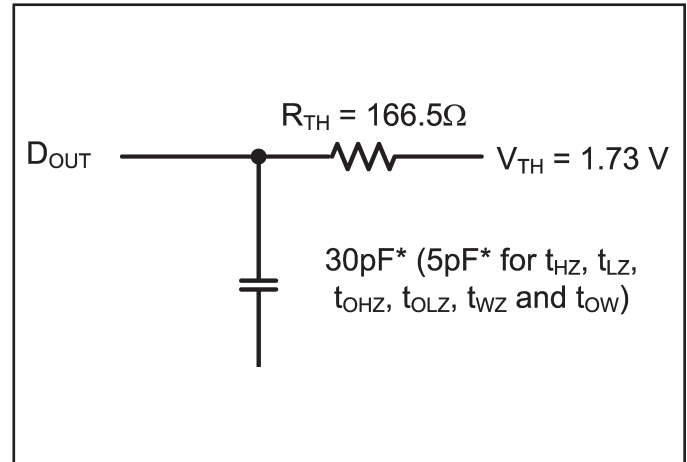


Figure 2. Thevenin Equivalent

Note:

Because of the ultra-high speed of the P4C1281 and P4C1282, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μF high

frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).



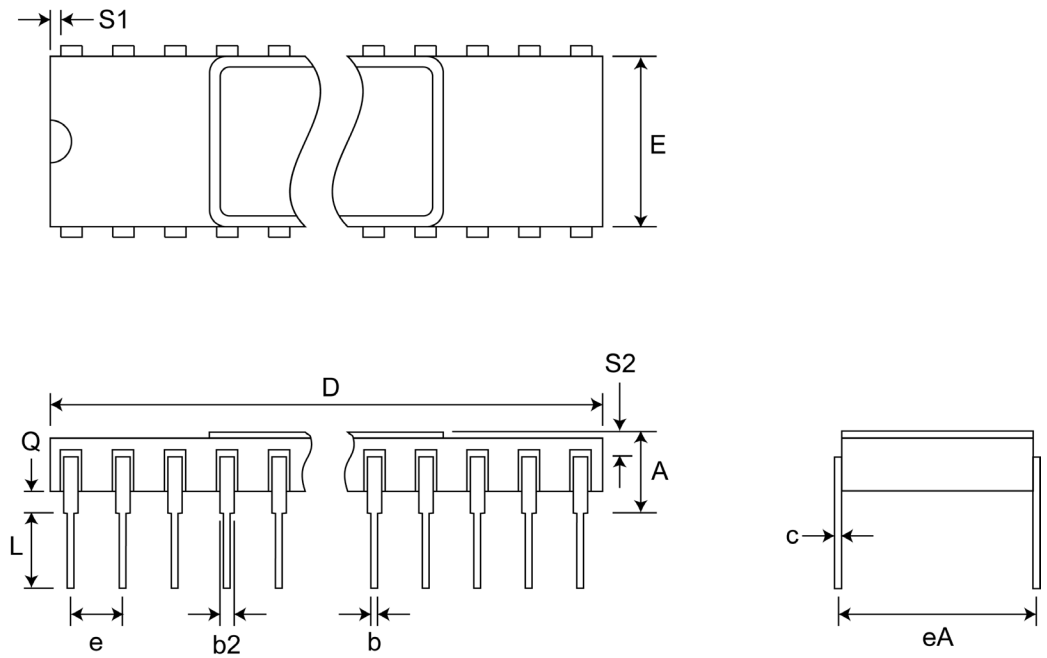
ORDERING INFORMATION

<u>P4C1281</u> <u>P4C1282</u> Device Type	<u>xx</u> Speed	<u>x</u> Package	<u>x</u> Processing	
				C 0°C to +70°C
				I -40°C to +85°C
				M -55°C to +125°C
				MB Mil Temp. with MIL-STD-883 Class B Compliance
				C Ceramic Side Brazed DIP, 300 mil
				D Ceramic DIP (CERDIP), 300 mil
				J Plastic SOJ, 300 mil
				L Ceramic LCC (350 x 550 mil)
				P Plastic DIP, 300 mil
				12, 15, 20, 25, 35, 45 ns
				64K x 4 SRAM



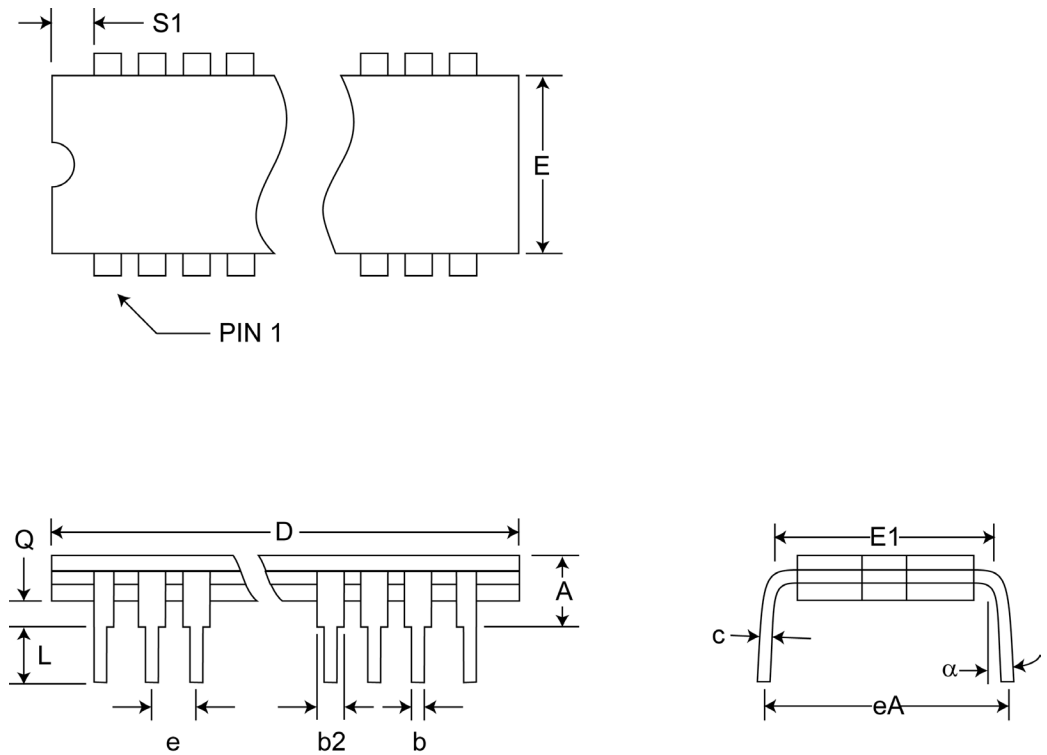
Pkg #	C5	
# Pins	28 (300 mil)	
Symbol	Min	Max
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.485
E	0.240	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



Pkg #	D5-2	
# Pins	28 (300 mil)	
Symbol	Min	Max
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.485
E	0.240	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
α	0°	15°

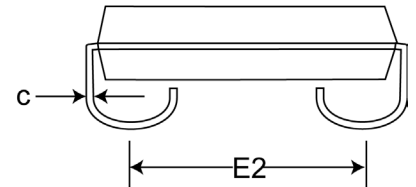
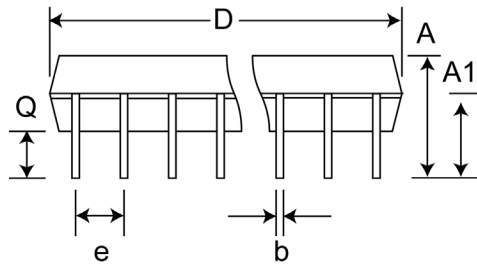
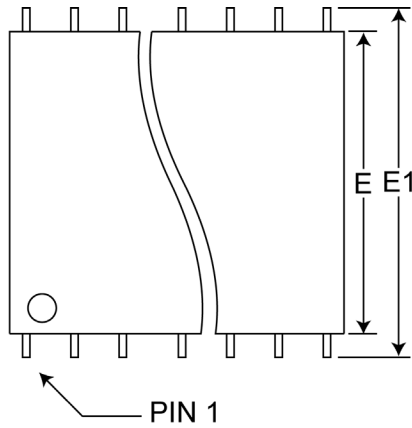
CERDIP DUAL IN-LINE PACKAGE





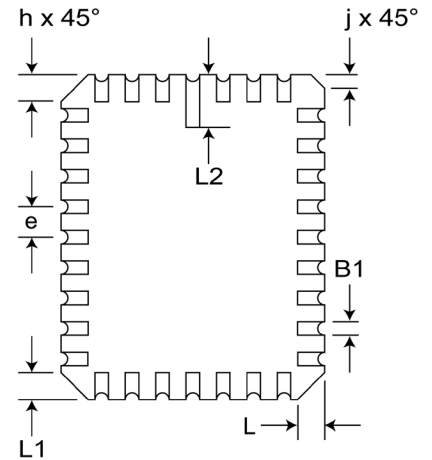
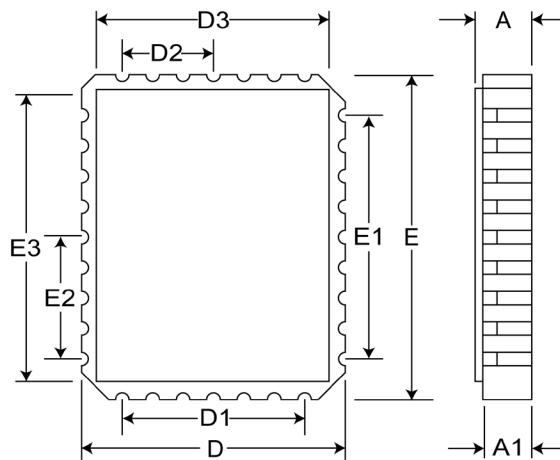
SOJ SMALL OUTLINE IC PACKAGE

Pkg #	J5	
# Pins	28 (300 mil)	
Symbol	Min	Max
A	0.120	0.148
A1	0.078	-
b	0.014	0.020
C	0.007	0.011
D	0.700	0.730
e	0.050 BSC	
E	0.292	0.300
E1	0.335	0.347
E2	0.262	0.272
Q	0.025	-



Pkg #	L5	
# Pins	28	
Symbol	Min	Max
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	-	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	9	

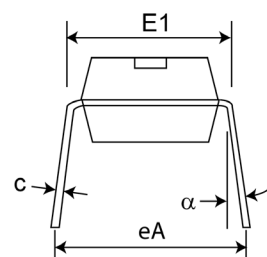
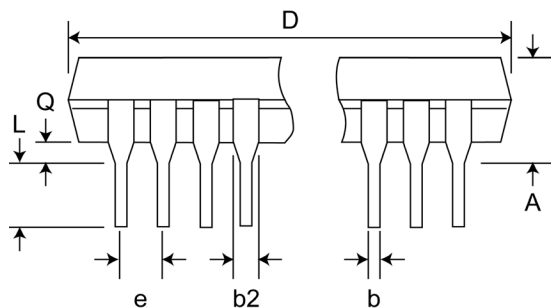
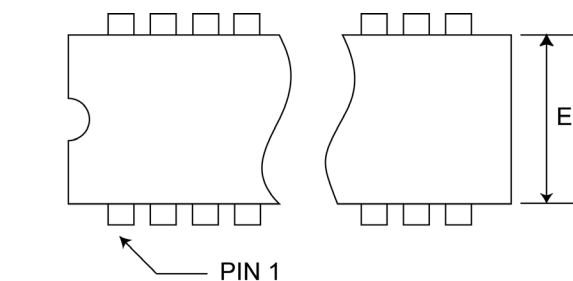
RECTANGULAR LEADLESS CHIP CARRIER





PLASTIC DUAL IN-LINE PACKAGE

Pkg #	P5	
# Pins	28 (300 mil)	
Symbol	Min	Max
A	-	0.210
A1	-	-
b	0.014	0.023
b2	0.045	0.070
C	0.008	0.014
D	1.345	1.400
E1	0.270	0.300
E	0.300	0.380
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
	0°	15°





REVISIONS

DOCUMENT NUMBER	SRAM136
DOCUMENT TITLE	P4C1281/P4C1282 - ULTRA HIGH SPEED 64K x 4 CMOS STATIC RAMS

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	July 10, 2009	JDB	New Data Sheet