P4C1681, P4C1682
ULTRA HIGH SPEED 4K x 4 STATIC CMOS RAMS

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 12/15/20/25 ns (Commercial)**
  - **– 20/25/35ns (Military)**
- **Low Power Operation**
- **Single 5V ± 10%Power Supply**
- **Separate Inputs and Outputs**
  - **– P4C1681 Input Data at Outputs during Write**
  - **– P4C1682 Outputs in High Z during Write**
- **Fully TTL Compatible Inputs and Outputs**
- **Standard Pinout (JEDEC Approved)**
  - **– 24-Pin 300 mil DIP**
  - **– 24-Pin 300 mil SOIC**
  - **– 24-Pin 300 mil SOJ**
  - **– 24-Pin Solder Seal Flat Pack**
  - **– 28-Pin LCC (450 mil x 450 mil)**

DESCRIPTION

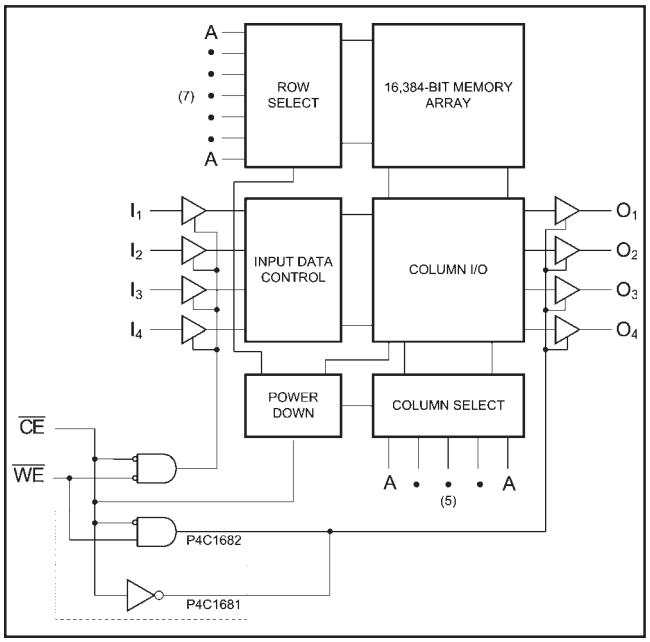
The P4C1681 and P4C1682 are 16,384-bit (4K x 4) ultra high speed static RAMs similar to the P4C168, but with separate data I/O pins. The P4C1681 features a transparent write operation; the outputs of the P4C1682 are in high impedance during the write cycle. All devices have low power standby modes. The RAMs operate from a single 5V ± 10% tolerance power supply.

Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds.

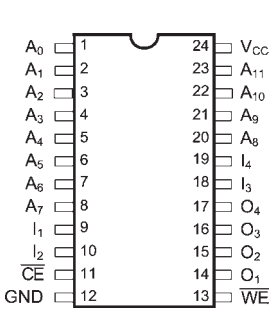
CMOS is used to reduce power consumption.

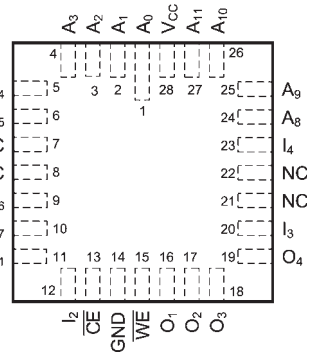
The P4C1681 and P4C1682 are available in 24-pin 300 mil DIP, SOIC, Solder Seal Flatpack, and SOJ packages, as well as a 28-pin LCC package, providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





DIP (P4,C4), SOIC (S4), SOJ (J4)
SOLDER SEAL FLAT PACK (FS-1)

LCC (L5-1)

MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade(2)	Ambient Temperature	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

CAPACITANCES[4]

V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

DC ELECTRICAL CHARACTERISTICS

Over Recommended operating temperature and supply voltages(2)

Sym.	Parameter	Test Conditions		P4C1681 P4C1682 Min	P4C1681 P4C1682 Max	Unit
V_{IH}	Input High Voltage			2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage			–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC} –0.2	V_{CC} +0.5	V
V_{LC}	CMOS Input Low Voltage			–0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min.			0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	I_{OLC} = +100 µA, V_{CC} = Min.			0.2	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.		2.4		V
V_{OHC}	Output High Voltage (CMOS Load)	I_{OHC} = –100 µA, V_{CC} = Min.		V_{CC} –0.2		V
I_{LI}	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	Mil. Comm'l	–10 –5	+10 +5	µA µA
I_{LO}	Output Leakage Current	V_{CC} = Max. $\overline{CE}$ = V_{IH} V_{OUT} = GND to V_{CC}	Mil. Comm'l	–10 –5	+10 +5	µA µA

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

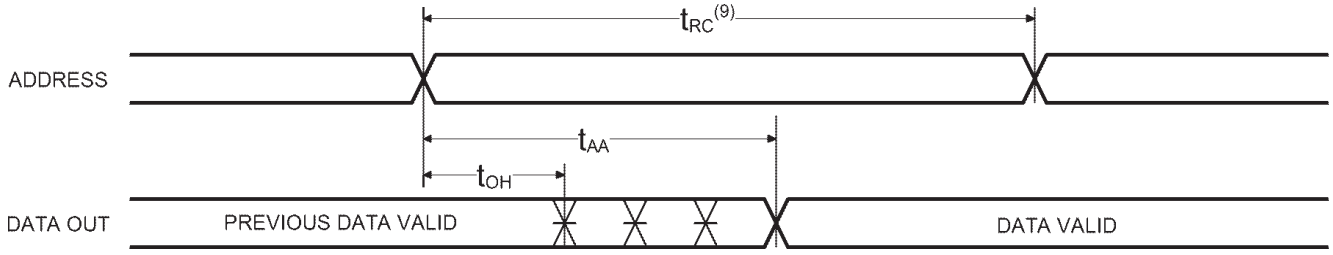
Symbol	Parameter	Test Conditions		P4C1681 P4C1682		Unit
				Min	Max	
I_{CC}	Dynamic Operating Current – 12, 15	V_{CC} = Max., f = Max., Outputs Open	Comm'l	—	130	mA
I_{CC}	Dynamic Operating Current – 20, 25, 35	V_{CC} = Max., f = Max., Outputs Open	Mil. Comm'l	— —	130 100	mA mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$, V_{CC} = Max., f = Max., Outputs Open		—	35	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$, V_{CC} = Max., f = 0, Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$		—	15	mA

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

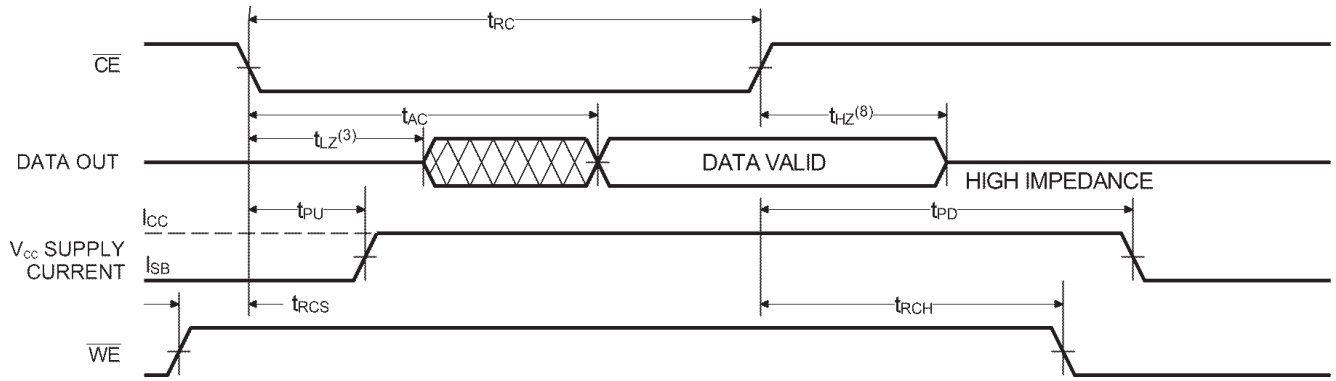
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address Access Time		12		15		20		25		35	ns
t_{AC}	Chip Enable Access Time		12		15		20		25		35	ns
t_{OH}	Output Hold from Address Change	2		2		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		6		7		9		10		15	ns
t_{RCS}	Read Command Setup Time	0		0		0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		0		0		ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		12		15		20		25		25	ns

READ CYCLE NO. 1 (ADDRESS controlled)[5, 6]



READ CYCLE NO. 2 ($\overline{CE}$ controlled)[5, 7]



Notes:

5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with, $\overline{CE}$ transition LOW.
8. Transition is measured ±200mV from steady state voltage prior to change, with loading as specified in Figure 1.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS—WRITE CYCLE

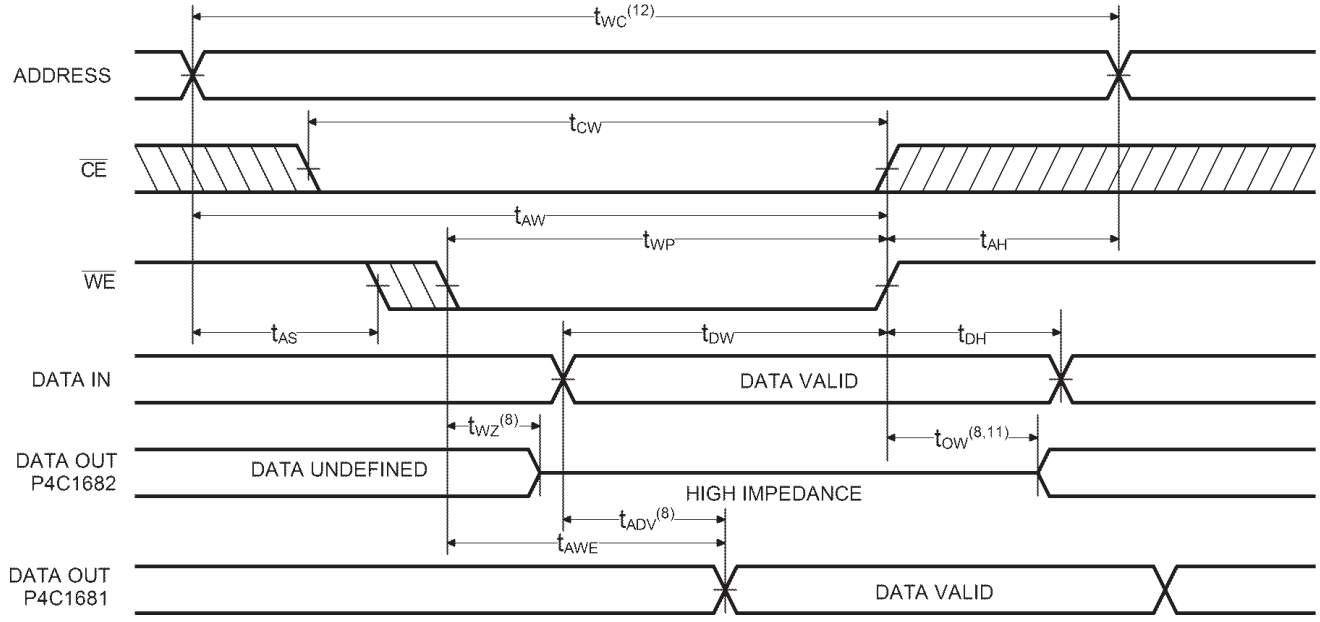
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12		15		18		20		30		ns
t_{CW}	Chip Enable Time to End of Write	12		15		18		20		25		ns
t_{AW}	Address Valid to End of Write	12		15		18		20		25		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		ns
t_{WP}	Write Pulse Width	12		15		18		20		25		ns
t_{AH}	Address Hold Time	0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	7		8		10		10		15		ns
t_{DH}	Data Hold Time	0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z†		4		5		7		7		13	ns
t_{OW}	Output Active to End of Write	0		0		0		0		0		ns
t_{AWE}	Write Enable to Data-out Valid£		12		15		20		25		30	ns
t_{ADV}	Data-in Valid to Data-out Valid		12		15		20		25		30	ns

† P4C1682 only.

£ P4C1681 only.

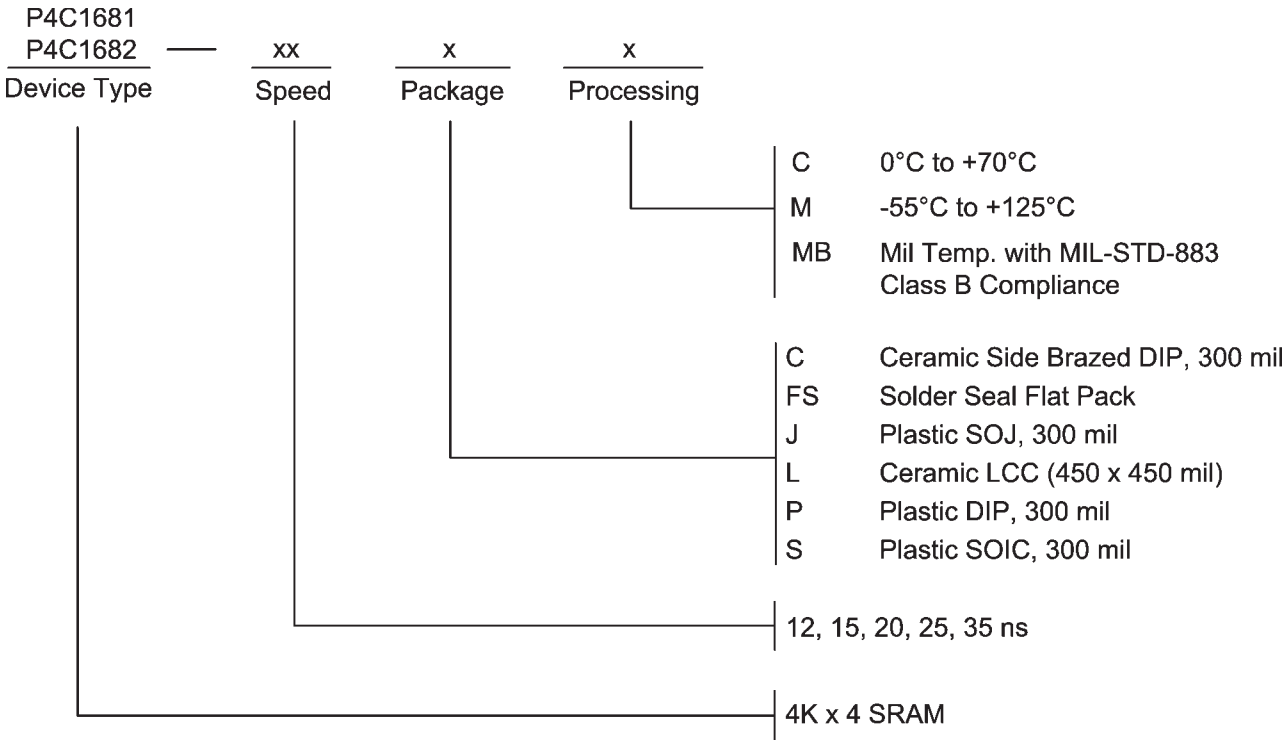
WRITE CYCLE NO. 1 ($\overline{WE}$ controlled)[10]



Notes:

10. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
12. Write Cycle Time is measured from the last valid address to the first transitioning address.

ORDERING INFORMATION



SELECTION GUIDE

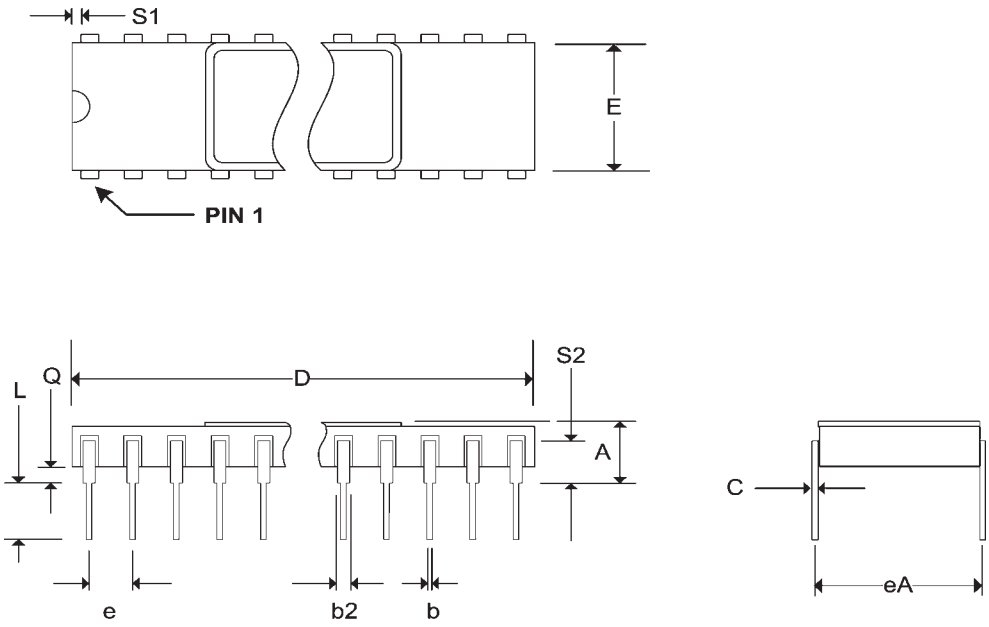
The P4C1681 and P4C1682 are available in the following temperature, speed and package options.

Temperature Range	Package	Speed				
		12	15	20	25	35
Commercial Temperature	Plastic DIP	-12PC	-15PC	-20PC	-25PC	N/A
	Plastic SOIC	-12SC	-15SC	-20SC	-25SC	N/A
	Plastic SOJ	-12JC	-15JC	-20JC	-25JC	N/A
Military Temperature	Side Brazed DIP	N/A	N/A	-20CM	-25CM	-35CM
	Solder Seal Flatpack	N/A	N/A	-20FSM	-25FSM	-35FSM
	LCC	N/A	N/A	-20LM	-25LM	-35LM
Military Processed*	Side Brazed DIP	N/A	N/A	-20CMB	-25CMB	-35CMB
	Solder Seal Flatpack	N/A	N/A	-20FSMB	-25FSMB	-35FSMB
	LCC	N/A	N/A	-20LMB	-25LMB	-35LMB

* Military temperature range with MIL-STD-883 Revision D, Class B processing.
N/A = Not available

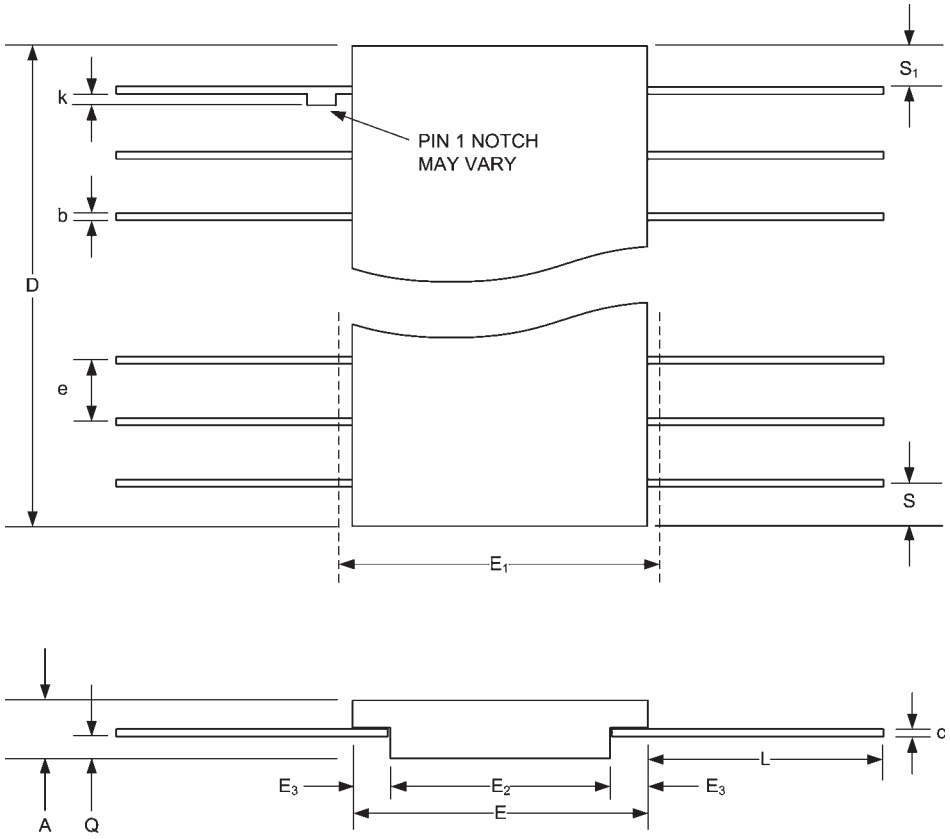
Pkg #	C4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDE BRAZED DUAL IN-LINE PACKAGE



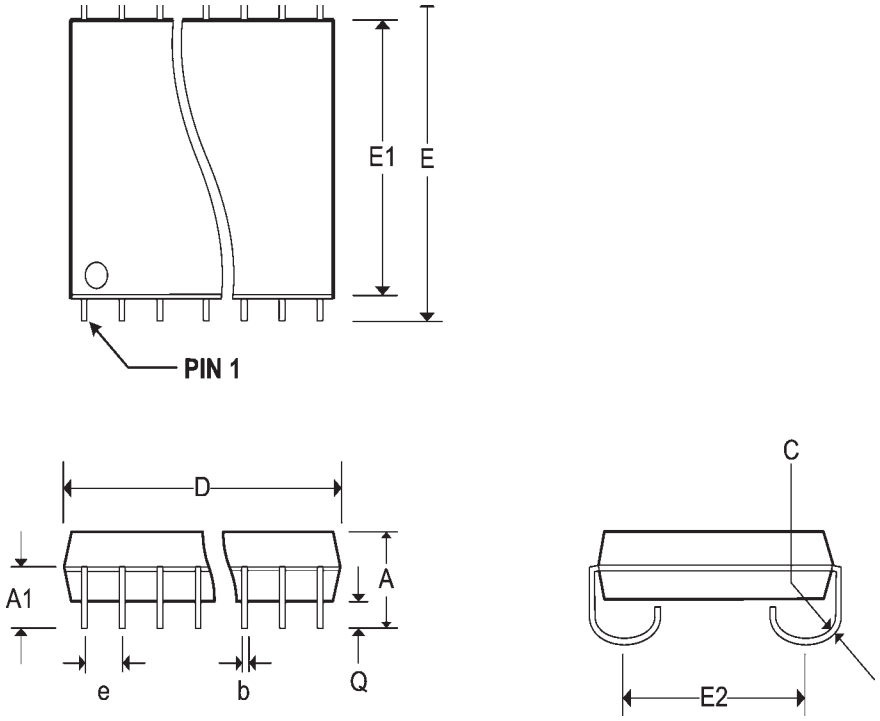
Pkg #	FS-1	
# Pins	24	
Symbol	**Min**	**Max**
A	0.045	0.115
b	0.015	0.022
b1	0.015	0.019
c	0.004	0.009
c1	0.004	0.006
D	-	0.640
E	0.350	0.420
E1	-	0.450
E2	0.180	-
E3	0.030	-
e	0.050 BSC	
k	0.008	0.015
L	0.250	0.370
Q	0.026	0.045
S1	0.000	-
M	-	0.0015
N	24	

SOLDER SEAL FLAT PACK



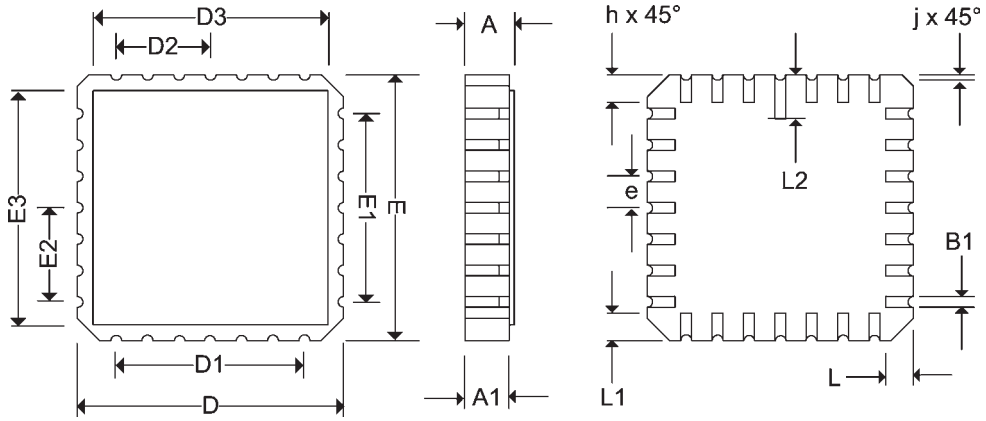
Pkg #	J4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.016	0.020
C	0.007	0.010
D	0.620	0.630
e	0.050 BSC	
E	0.335 BSC	
E1	0.292	0.300
E2	0.267 BSC	
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE



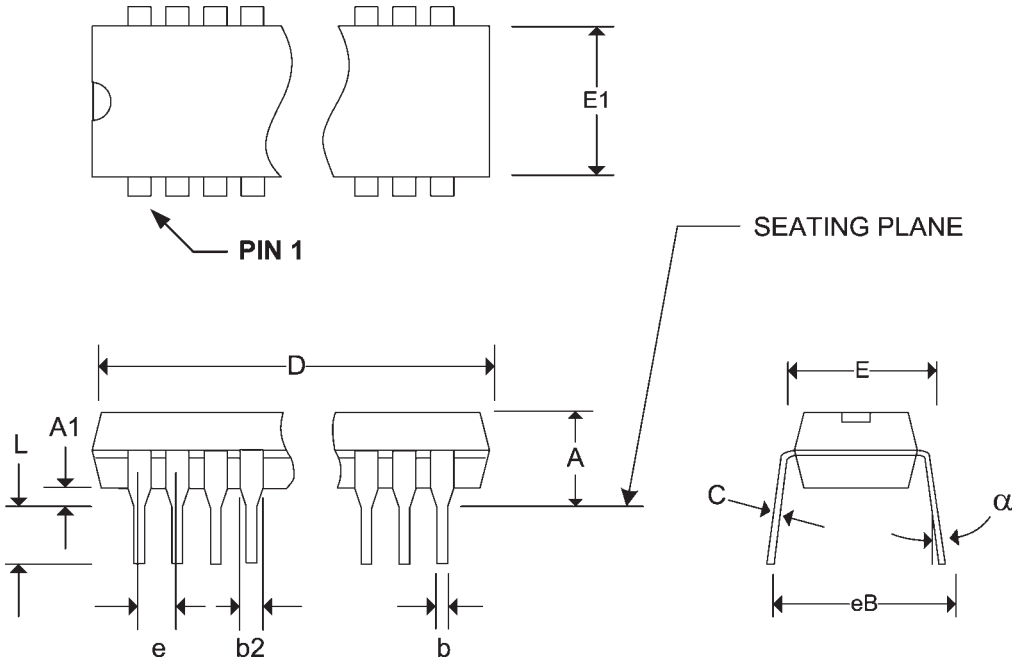
Pkg #	L5-1	
# Pins	28	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D/E	0.442	0.460
D1/E1	0.300 BSC	
D2/E2	0.150 BSC	
D3/E3	-	0.460
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	7	

SQUARE LEADLESS CHIP CARRIER



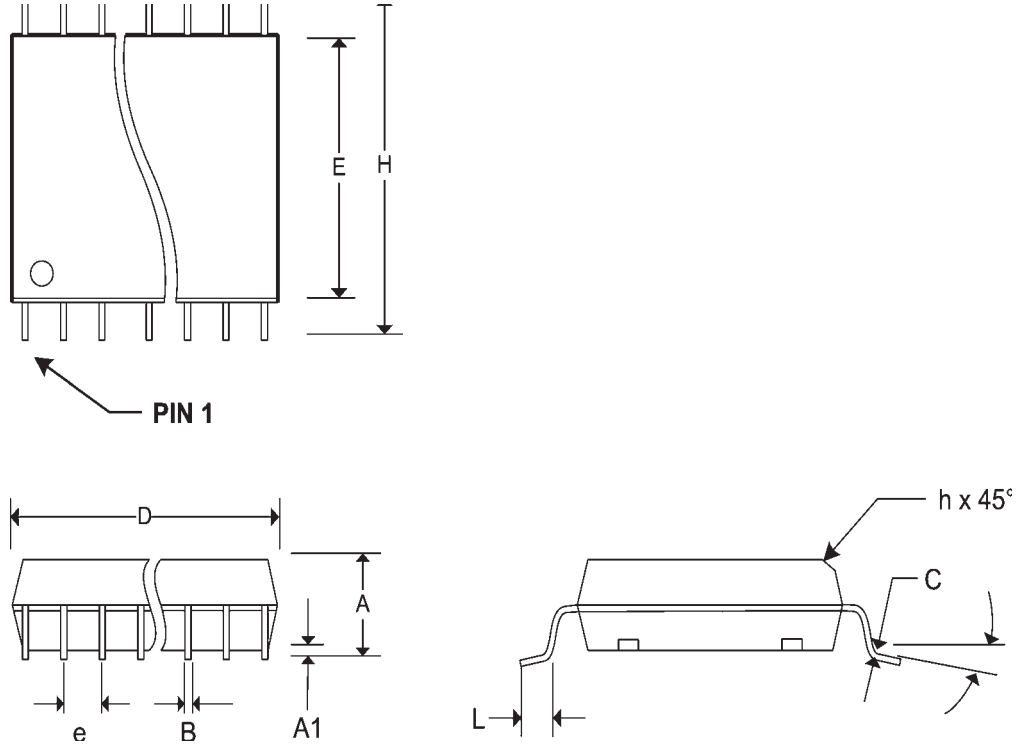
Pkg #	P4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.070
C	0.008	0.014
D	1.230	1.280
E1	0.240	0.280
E	0.300	0.325
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



Pkg #	S4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	0.093	0.104
A1	0.004	0.012
b2	0.013	0.020
C	0.009	0.012
D	0.598	0.614
e	0.050 BSC	
E	0.291	0.299
H	0.394	0.419
h	0.010	0.029
L	0.016	0.050
α	0°	8°

SOIC/SOP SMALL OUTLINE IC PACKAGE



REVISIONS

DOCUMENT NUMBER:	SRAM109
DOCUMENT TITLE:	P4C1681 / P4C1682 ULTRA HIGH SPEED 4K x 4 STATIC CMOS RAMS

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-05	JDB	Change logo to Pyramid