

## USBizi™ Chipset



**LQFP144 package**



**LQFP100 package**

**USBizi™ Chipset**, pronounced as USB easy, is an ARM7 micro-controller from NXP (LPC2388 or LPC2387) with a special firmware developed to host .NET Micro Framework with various HAL drivers. With this sophisticated combination, a developer can easily control the micro-controller's IOs and interfaces such as SPI, UART(Serial Port) and I2C with simple unified managed code (C# code) and enjoy the wide various higher level services offered by NETMF such as file system access. Not to mention GHI's extended features such as PWM, ADC, DAC and full USB host stack.

Everything is implemented on a single-chip making USBizi™ the smallest and least expensive .NET Micro Framework device, and still implements unique features like USB host.

### USBizi™ 100 pin Package

USBizi™ 100 pin chipset is identical to the 144 pin version except it does not contain a USB host. USB device is till available and works exactly the same way.

### What is .NET Micro Framework?

Microsoft's .NET Micro Framework extends the advantages of .NET and Visual Studio to a class of smaller, less expensive, and more resource-constrained devices than the .NET Compact Framework and the standard .NET framework.

### Extended Framework Features

The USBizi™ module supports a complete set of .NET Micro Framework features such as FAT, USB device and many more. In addition, it supports many other exclusive GHI features such as CAN, ADC, DAC and full USB host stack.

### Key Features

- Microsoft .NET Micro Framework
- 72Mhz 32-bit Processor
- 96KB RAM
- 512KB FLASH
- Embedded USB Host(144 pin package only)
- Embedded USB Device
- Native Ethernet TCP/IP support using W5100 (WIZnet Hardwired TCP/IP Embedded Ethernet Controller)
- 71 GPIO
- 35 Interrupt Inputs
- 2 SPI (8/16bit)
- I2C
- 4 UART
- 2 CAN Channels
- 8 10-bit Analog Inputs (6 on 100pin package)
- 10-bit Analog Output
- 4-bit SD/MMC interface
- 6 PWM
- 100 mA everything enabled
- 200 uA Hibernate Modes
- -40°C to +85°C Operational
- RoHS Lead Free

## USBizi™ LQFP 144 Pin-out table

USBizi™ LQFP144 chipset is based on LPC2388 from NXP.

Name				* Interrupt capable input.
No.	LPC2388 H/W	USBizi IO	2 <sup>nd</sup> Feature	USBizi™ Pin Description
8	P0.26	IO22*	ADC3/ DAC	ADC3 (10-Bit Analog to Digital Input) or DAC (Digital to Analog Output)
10	P0.25	IO24*	ADC2	ADC2 (10-Bit Analog to Digital Input)
11	P0.24	IO26*	ADC1	ADC1 (10-Bit Analog to Digital Input)
13	P0.23	IO28*	ADC0	ADC0 (10-Bit Analog to Digital Input)
14	VDDA			Connect to 3.3 volt source
15	VSSA			Connect to Ground
17	VREFA			Connect to 3.3 volt source
18	VDD_1			Connect to 3.3 volt source
22	VSS1			Connect to Ground
23	RTCX1			Connect to real-time crystal circuit pin 1
24	RESET#			Hardware reset signal, Reset state is on Low
25	RTCX2			Connect to real-time crystal circuit pin 2
26	ALARM			Leave unconnected (future use)
27	VBAT			Connect to 3.3 volt back up battery to keep the real-time clock running.
28	P1.31	IO32	ADC5	ADC5 (10-Bit Analog to Digital Input)
29	P0.12	IO30*	ADC6	ADC6 (10-Bit Analog to Digital Input)
30	P1.30	IO29	ADC4	ADC4 (10-Bit Analog to Digital Input)
31	XTAL1			Connect to the system's 12MHz. crystal pin1
32	P0.13	IO27*	ADC7	ADC7 (10-Bit Analog to Digital Input)
33	XTAL2			Connect to the systems 12MHz. crystal pin1
34	P0.28	IO31*	I2C	<b>(open drain pin)</b> I2C Interface SCL
35	P0.27	IO33*	I2C	<b>(open drain pin)</b> I2C Interface SDA
36	USB D+ USB Client Feature			USB positive data line, USB (access) debugging interface and for the USB client feature.
37	USB D- USB Client Feature			USB negative data line, USB (access) debugging interface and for the USB client feature.
38	P3.26	IO69	N/A	General purpose digital I/O
39	P3.25	IO68	N/A	General purpose digital I/O
40	P3.24	IO70	N/A	General purpose digital I/O
41	VDD1			Connect to 3.3 volt source
42	USB D+ USB Host Feature			USB positive data line of the USB hosting feature.
43	USB D- USB Host Feature			USB negative data line of the USB hosting feature.
44	VSS2			Connect to Ground
46	P1.18	IO35	PWM1	PWM1 (Pulse Width Modulation Output)
47	P1.19	IO34	N/A	General purpose digital I/O
48	USB_CON USB Client Feature			Reports the USB cable attachment to the PC USB Host (refer to the reference design schematic for the required circuit).
49	P1.20	IO25	PWM2	PWM2 (Pulse Width Modulation Output)
50	P1.21	IO23	PWM3	PWM3 (Pulse Width Modulation Output)
51	P1.22	IO61	USB_PW R_RD	Related to USB host feature (refer to the reference design schematic for connection)
53	P1.23	IO62	N/A	General purpose digital I/O
54	P1.24	IO63	N/A	General purpose digital I/O
56	P1.25	IO64	N/A	General purpose digital I/O
57	P1.26	IO65	N/A	General purpose digital I/O

No.	Name			USBizi™ Pin Description
	LPC2388 H/W	USBizi IO	2 <sup>nd</sup> Feature	
59	VSS3			Connect to Ground
60	VDD_2			Connect to 3.3 volt source
61	P1.27	IO21	N/A	General purpose digital I/O
62	VDD2			Connect to 3.3 volt source
63	P1.28	IO66	N/A	General purpose digital I/O
64	P1.29	IO67	N/A	General purpose digital I/O
65	VSS4			Connect to Ground
66	P0.0	IO19*	CAN1	RD CAN Channel 1 Data Receive pin (In)
67	P0.1	IO15*	CAN1	TD CAN Channel 1 Data Transmit pin (Out)
69	P0.10	IO39*	N/A	Only general purpose digital I/O
70	P0.11	IO38*	N/A	Only general purpose digital I/O
71	P2.13	IO50*	SD_DAT3	SD card 4-bit data bus, data line no. 3
73	P2.12	IO49*	SD_DAT2	SD card 4-bit data bus, data line no. 2
75	P2.11	IO48*	SD_DAT1	SD card 4-bit data bus, data line no. 1
76	P2.10	IO0*	<b>BL#</b>	General purpose digital I/O. On power up, this pin is used to access GHI boot loader when Low (refer to <a href="#">GHI boot loader section</a> ). This pin is high (no loader) if not connected.
77	VDD3			Connect to 3.3 volt source
79	VSS5			Connect to Ground
80	P0.22	IO47*	SD_DAT0	SD card 4-bit data bus, data line no. 0
82	P0.21	IO46*	MCIPWR	Memory card (SD/MMC) power enable signal (refer to the reference design schematic for connection).
83	P0.20	IO45*	SD_CMD	SD card 4-bit data bus, command line
85	P0.19	IO44*	SD_CLK	SD card 4-bit data bus, clock line
86	P0.18	IO41*	SPI1	SPI master bus interface MOSI signal (Master Out Slave In) for SPI1
87	P0.17	IO40*	SPI1	SPI master bus interface MISO signal (Master In Slave Out) for SPI1
89	P0.15	IO42*	SPI1	SPI master bus interface SCK signal (Clock) for SPI1
90	P0.16	IO43*	N/A	General purpose digital I/O
92	P2.9	IO37*	COM3	Serial port (UART) RXD receive signal (In) for COM3
93	P2.8	IO36*	COM3	Serial port (UART) TXD transmit signal (Out) for COM3
95	P2.7	IO11*	COM2	Serial port (UART) RTS signal for COM2
96	P2.6	IO9*	N/A	Only general purpose digital I/O
97	P2.5	IO7*	PWM6	PWM6 (Pulse Width Modulation Output)
99	P2.4	IO2*	PWM5	PWM5 (Pulse Width Modulation Output)
100	P2.3	IO4*	<b>PWM4/MODE</b>	PWM4 (Pulse Width Modulation Output). On power up, this pin is used to select the access interface for GHI boot loader and debugging, between USB (High) or COM1(Low). (refer to <a href="#">GHI boot loader section</a> ). This pin is high (select USB) if not connected.
102	VDD4			Connect to 3.3 volt source
103	VSS6			Connect to Ground
105	P2.2	IO1*	COM2	Serial port (UART) CTS signal for COM2
106	P2.1	IO3*	COM2	Serial port (UART) RXD receive signal (In) for COM2
107	P2.0	IO5*	COM2	Serial port (UART) TXD transmit signal (Out) for COM2
109	P0.9	IO6*	SPI2	SPI master bus interface MOSI signal (Master Out Slave In) for SPI2
111	P0.8	IO8*	SPI2	SPI master bus interface MISO signal (Master In Slave Out) for SPI2
112	P0.7	IO10*	SPI2	SPI master bus interface SCK signal (Clock) for SPI2
113	P0.6	IO12*	N/A	General purpose digital I/O
114	VDD5			Connect to 3.3 volt source
115	P0.5	IO14*	CAN2	TD CAN Channel 2 Data Transmit pin (Out)
116	P0.4	IO16*	CAN2	RD CAN Channel 2 Data Receive pin (In)
117	VSS7			Connect to Ground

No.	Name			USBizi™ Pin Description
	LPC2388 H/W	USBizi IO	2 <sup>nd</sup> Feature	
				* Interrupt capable input.
118	P4.28	IO13	COM4	Serial port (UART) TXD transmit signal (Out) for COM4
119		VSS8		Connect to Ground
121		VDD_3		Connect to 3.3 volt source
122	P4.29	IO17	COM4	Serial port (UART) RXD receive signal (In) for COM4
123	P1.17	IO60	N/A	General purpose digital I/O
125	P1.16	IO59	N/A	General purpose digital I/O
126	P1.15	IO58	N/A	General purpose digital I/O
128	P1.14	IO57	N/A	General purpose digital I/O
129	P1.10	IO56	N/A	General purpose digital I/O
131	P1.9	IO55	N/A	General purpose digital I/O
132	P1.8	IO54	N/A	General purpose digital I/O
133	P1.4	IO53	N/A	General purpose digital I/O
135	P1.1	IO52	N/A	General purpose digital I/O
136	P1.0	IO51	N/A	General purpose digital I/O
138		VDD6		Connect to 3.3 volt source
139		VSS9		Connect to Ground
141	P0.2	IO18*	COM1	Serial port (UART) TXD transmit signal (Out) for COM1
142	P0.3	IO20*	COM1	Serial port (UART) RXD receive signal (In) for COM1

## USBizi™ LQFP 100 Pin-out table

USBizi LQFP100 chipset is based on LPC2387 from NXP

No.	Name			USBizi™ Pin Description
	LPC2387 H/W	USBizi IO	2 <sup>nd</sup> Feature	
				* Interrupt capable input.
6	P0.26	IO22*	ADC3/ DAC	ADC3 (10-Bit Analog to Digital Input) or DAC (Digital to Analog Output)
7	P0.25	IO24*	ADC2	ADC2 (10-Bit Analog to Digital Input)
8	P0.24	IO26*	ADC1	ADC1 (10-Bit Analog to Digital Input)
9	P0.23	IO28*	ADC0	ADC0 (10-Bit Analog to Digital Input)
10		VDDA		Connect to 3.3 volt source
11		VSSA		Connect to Ground
12		VREFA		Connect to 3.3 volt source
13		VDD_1		Connect to 3.3 volt source
15		VSS1		Connect to Ground
16		RTCX1		Connect to real-time crystal circuit pin 1
17		RESET#		Hardware reset signal, Reset state is on Low
18		RTCX2		Connect to real-time crystal circuit pin 2
19		VBAT		Connect to 3.3 volt back up battery to keep the real-time clock running.
20	P1.31	IO32	ADC5	ADC5 (10-Bit Analog to Digital Input)
21	P1.30	IO29	ADC4	ADC4 (10-Bit Analog to Digital Input)
22		XTAL1		Connect to the system's 12MHz. crystal pin1
23		XTAL2		Connect to the systems 12MHz. crystal pin1
24	P0.28	IO31*	I2C	<b>(open drain pin)</b> I2C Interface SCL
25	P0.27	IO33*	I2C	<b>(open drain pin)</b> I2C Interface SDA
26	P3.26	IO69	N/A	General purpose digital I/O
27	P3.25	IO68	N/A	General purpose digital I/O

No.	Name			USBizi™ Pin Description
	LPC2387 H/W	USBizi IO	2 <sup>nd</sup> Feature	
28	VDD1			Connect to 3.3 volt source
29	USB_D+ USB Client Feature			USB positive data line, USB (access) debugging interface and for the USB client feature.
30	USB_D- USB Client Feature			USB negative data line, USB (access) debugging interface and for the USB client feature.
31	VSS2			Connect to Ground
32	P1.18	IO35	PWM1	PWM1 (Pulse Width Modulation Output)
33	P1.19	IO34	N/A	General purpose digital I/O
34	P1.20	IO25	PWM2	PWM2 (Pulse Width Modulation Output)
35	P1.21	IO23	PWM3	PWM3 (Pulse Width Modulation Output)
36	P1.22	IO61	N/A	General purpose digital I/O
37	P1.23	IO62	N/A	General purpose digital I/O
38	P1.24	IO63	N/A	General purpose digital I/O
39	P1.25	IO64	N/A	General purpose digital I/O
40	P1.26	IO65	N/A	General purpose digital I/O
41	VSS3			Connect to Ground
42	VDD_2			Connect to 3.3 volt source
43	P1.27	IO21	N/A	General purpose digital I/O
44	P1.28	IO66	N/A	General purpose digital I/O
45	P1.29	IO67	N/A	General purpose digital I/O
46	P0.0	IO19*	CAN1	RD CAN Channel 1 Data Receive pin (In)
47	P0.1	IO15*	CAN1	TD CAN Channel 1 Data Transmit pin (Out)
48	P0.10	IO39*	COM3	Serial port (UART) TXD transmit signal (Out) for COM3
49	P0.11	IO38*	COM3	Serial port (UART) RXD receive signal (In) for COM3
50	P2.13	IO50*	SD_DAT3	SD card 4-bit data bus, data line no. 3
51	P2.12	IO49*	SD_DAT2	SD card 4-bit data bus, data line no. 2
52	P2.11	IO48*	SD_DAT1	SD card 4-bit data bus, data line no. 1
53	P2.10	IO0*	BL#	General purpose digital I/O. On power up, this pin is used to access GHI boot loader when Low (refer to <a href="#">GHI boot loader section</a> ) This pin is high (no loader) if not connected.
54	VDD2			Connect to 3.3 volt source
55	VSS4			Connect to Ground
56	P0.22	IO47*	SD_DAT0	SD card 4-bit data bus, data line no. 0
57	P0.21	IO46*	MCIPWR	Memory card (SD/MMC) power enable signal (refer to the reference design schematic for connection).
58	P0.20	IO45*	SD_CMD	SD card 4-bit data bus, command line
59	P0.19	IO44*	SD_CLK	SD card 4-bit data bus, clock line
60	P0.18	IO41*	SPI1	SPI master bus interface MOSI signal (Master Out Slave In) for SPI1
61	P0.17	IO40*	SPI1	SPI master bus interface MISO signal (Master In Slave Out) for SPI1
62	P0.15	IO42*	SPI1	SPI master bus interface SCK signal (Clock)for SPI1
63	P0.16	IO43*	N/A	General purpose digital I/O
64	USB_CON USB Client Feature			Reports the USB cable attachment to the PC USB Host (refer to the reference design schematic for the required circuit).
65	P2.8	IO36*	N/A	Only general purpose digital I/O.
66	P2.7	IO11*	COM2	Serial port (UART) RTS signal for COM2
67	P2.6	IO9*	N/A	General purpose digital I/O
68	P2.5	IO7*	PWM6	PWM6 (Pulse Width Modulation Output)
69	P2.4	IO2*	PWM5	PWM5 (Pulse Width Modulation Output)
70	P2.3	IO4*	PWM4/ MODE	PWM4 (Pulse Width Modulation Output), On power up, this pin is used to select the communication interface for GHI boot loader and debugging, between USB (High) or COM1(Low). (refer to <a href="#">GHI boot loader section</a> ) This pin is high (select USB) if not connected.

No.	Name			USBizi™ Pin Description
	LPC2387 H/W	USBizi IO	2 <sup>nd</sup> Feature	
71		VDD3		Connect to 3.3 volt source
72		VSS5		Connect to Ground
73	P2.2	IO1*	COM2	Serial port (UART) CTS signal for COM2
74	P2.1	IO3*	COM2	Serial port (UART) RXD receive signal (In) for COM2
75	P2.0	IO5*	COM2	Serial port (UART) TXD transmit signal (Out) for COM2
76	P0.9	IO6*	SPI2	SPI master bus interface MOSI signal (Master Out Slave In) for SPI2
77	P0.8	IO8*	SPI2	SPI master bus interface MISO signal (Master In Slave Out)for SPI2
78	P0.7	IO10*	SPI2	SPI master bus interface SCK signal (Clock)for SPI2
79	P0.6	IO12*		General purpose digital I/O
80	P0.5	IO14*	CAN2	TD CAN Channel 2 Data Transmit pin (Out)
81	P0.4	IO16*	CAN2	RD CAN Channel 2 Data Receive pin (In)
82	P4.28	IO13	COM4	Serial port (UART) TXD transmit signal (Out) for COM4
83		VSS7		Connect to Ground
84		VDD_3		Connect to 3.3 volt source
85	P4.29	IO17	COM4	Serial port (UART) RXD receive signal (In) for COM4
86	P1.17	IO60	N/A	General purpose digital I/O
87	P1.16	IO59	N/A	General purpose digital I/O
88	P1.15	IO58	N/A	General purpose digital I/O
89	P1.14	IO57	N/A	General purpose digital I/O
90	P1.10	IO56	N/A	General purpose digital I/O
91	P1.9	IO55	N/A	General purpose digital I/O
92	P1.8	IO54	N/A	General purpose digital I/O
93	P1.4	IO53	N/A	General purpose digital I/O
94	P1.1	IO52	N/A	General purpose digital I/O
95	P1.0	IO51	N/A	General purpose digital I/O
96		VDD4		Connect to 3.3 volt source
97		VSS6		Connect to Ground
98	P0.2	IO18*	COM1	Serial port (UART) TXD transmit signal (Out) for COM1
99	P0.3	IO20*	COM1	Serial port (UART) RXD receive signal (In) for COM1

Note: IO27, IO30, IO36 and IO70 are not supported in 100 package.



**For further Information:**

USBizi™ Prototyping and Evaluation:

<http://www.ghielectronics.com/product/113>

Related Documents:

[USBizi™ Module User Manual](#)

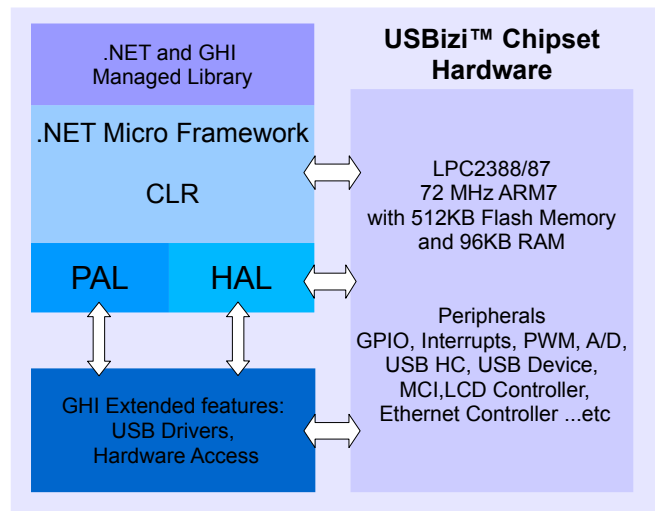
Weblinks:

<http://www.ghielectronics.com/>

<http://www.usbizi.com/>

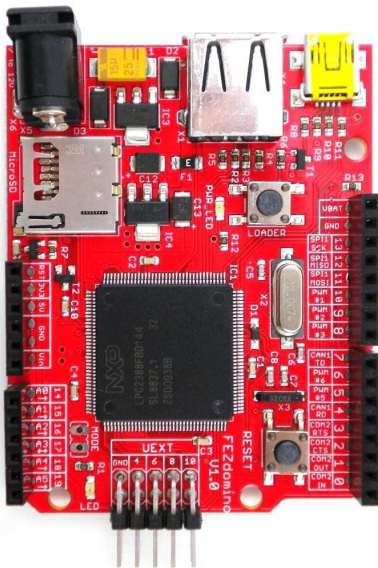
Customer Support:

<http://www.ghielectronics.com/forum>

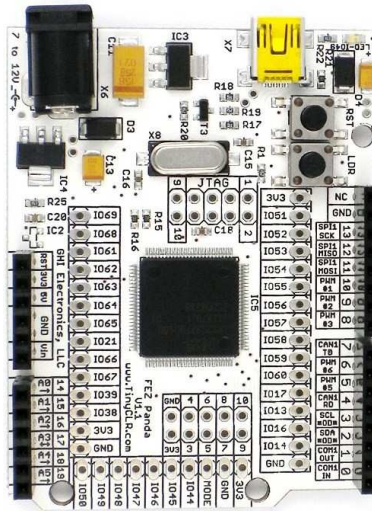
**Block Diagram****Recommended Hardware and Tutorials**

GHI Electronics offers an open source hardware development platform for beginners powered by USBizi™.

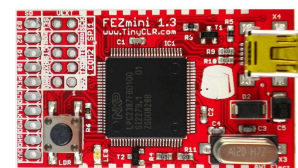
From the ground up, FEZ Mini, FEZ Panda, and FEZ Domino boards are designed with help of USBizi™ chipsets to be extremely easy to learn. For more details about these products visit [www.tinyclr.com](http://www.tinyclr.com). This website also offers a free eBook for .NET Micro Framework beginners in addition to the FEZ (USBizi™) tutorials.



**FEZ Domino Based on USBizi™  
LQFP144**



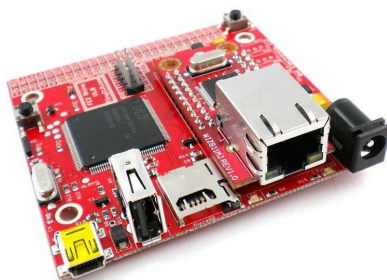
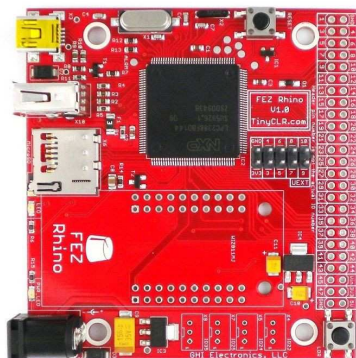
**FEZ Panda Based on USBizi™  
LQFP100**



**FEZ Mini Based on USBizi™  
LQFP100**

## USBizi™ OEM solution

GHI Electronics offers **FEZ Rhino** as an OEM solution using USBizi™ 144. It has all the peripherals and signals exposed. Also it is ready to host WIZ811MJ Ethernet module and SPI mono color displays. GHI also provides an optional plastic enclosure for this OEM board.



For more information about FEZ Rhino:

[http://www.tinyclr.com/downloads/Rhino/Broch\\_FEZ\\_Rhino.pdf](http://www.tinyclr.com/downloads/Rhino/Broch_FEZ_Rhino.pdf)



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