Data sheet

BMA150
Digital, triaxial acceleration sensor

Bosch Sensortec

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BMA150: Data sheet

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BMA150

DIGITAL, TRIAXIAL ±2G/±4G/±8G ACCELERATION SENSOR

Key features

• Three-axes accelerometer	
• Temperature output	
• Small package	LGA package Footprint 3mm x 3mm, height 0.90mm
• Digital interface	SPI (4-wire, 3-wire), I^2C, interrupt pin
• Programmable functionality	g-range ±2g/±4g/±8g, bandwidth 25-1500Hz, internal acceleration evaluation for interrupt trigger also enabling stand-alone capability (without use of microcontroller), self-test
• Ultra-low power ASIC	Low current consumption, short wake-up time, advanced features for system power management
• Eco-friendly	RoHS compliant , Halogen-free (technical reference codes: 0 273 141 043, 0 273 141 081)

Typical applications

- HDD protection
- Menu scrolling, tap sensing function
- Gaming
- Pedometer/step-counting
- Drop detection for warranty logging
- Display profile switching
- Advanced system power management for mobile applications
- Shock detection

General Description

The BMA150 is a triaxial, low-g acceleration sensor IC with digital output for consumer market applications. It allows measurements of acceleration in perpendicular axes as well as absolute temperature measurement.
An evaluation circuitry converts the output of a three-channel micromechanical acceleration-sensing structure that works according to the differential capacitance principle.
Package and interface have been defined to match a multitude of hardware requirements. Since the sensor IC has small footprint and flat package it is attractive for mobile applications. The sensor IC can be programmed to optimize functionality, performance and power consumption in customer specific applications.
The BMA150 senses tilt, motion and shock vibration in cell phones, handhelds, computer peripherals, man-machine interfaces, virtual reality features and game controllers.

The BMA150 is the LGA package version of the SMB380 triaxial acceleration sensor which is available in a 3mm x 3mm x 0.9mm QFN package.

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1. Specification

If not stated otherwise, the given values are maximum values over lifetime and full performance temperature and voltage ranges, and min./max. values represent 3-sigma limits.

Table 1: Operating range, output signal and mechanical specifications of BMA150

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OPERATING RANGE						
Acceleration range	g_{FS2g}	Switchable via serial digital interface	-2		2	g
	g_{FS4g}		-4		4	g
	g_{FS8g}		-8		8	g
Supply voltage analogue	V_{DD}		2.4		3.6	V
Supply voltage for digital I/O	V_{DDIO}	$V_{DDIO} \leq V_{DD}$	1.62		3.6	V
Supply current in normal mode	I_{DD}	Digital and analog		200	290	µA
Supply current in stand-by mode *	I_{DDsbm}	Digital and analog		1	2	µA
Operating temperature	T_A		-40		+85	°C
ACCELERATION OUTPUT SIGNAL						
Acceleration output resolution		Format: 2's complement			10	Bit
Sensitivity	S_{2g}	g-range ±2g	246	256	266	LSB/g
	S_{4g}	g-range ±4g	122 **	128	134 **	LSB/g
	S_{8g}	g-range ±8g	61 **	64	67 **	LSB/g
Zero-g offset	Off	T_A=25°C, calibrated	-60		60	mg
Zero-g offset	Off	T_A=25°C , over lifetime ***	-150		150	mg
Zero-g offset temperature drift		Over T_A		1		mg/K
Power supply rejection ratio	PSRR	Over V_{DD}			0.2	LSB/V

* For more details on the BMA150's current consumption during wake-up mode, please refer to chapter 7.2 & 7.3
** Values here are given as indications for reference only
*** The offset can deviate from the original calibration mainly due to stress effects during soldering depending on the soldering process. For many applications it is beneficial to re-calibrate the offset after PCB assembly (see application note BST-MAS-AN014-01.pdf "In-line offset re-calibration").

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Bandwidth	bw	2nd order analog filter		1500		Hz
		Digital filter *		25, 50, 100, 190, 375, 750		Hz
Acceleration data refresh rate (all axes)	f_rate		2700	3000	3300	Hz
Nonlinearity	NL	Best fit straight line	-0.5		0.5	%FS
Output noise	n_{rms}	Rms		0.5		mg/√Hz
TEMPERATURE SENSOR IC						
Sensitivity	S_T	Preliminary data	0.475	0.5	0.525	K/LSB
Temperature measurement range	T_S		-30		97.5	°C
Temperature offset	Off_T	Calibrated at 30°C		1		K
MECHANICAL CHARACTERISTICS						
Cross axis sensitivity	$\bar{S}$	Relative contribution between 3 axes			2	%
POWERING UP CHARACTERISTICS						
Wake-up time	t_{wu}	From stand-by		1	1.5	ms
Start-up time	t_{su}	From power-off		3		ms

* Please refer to chapter 3.1.3 for more detailed explanations

2. Maximum ratings

Table 2: Maximum ratings specified for the BMA150

Parameter	Condition	Min	Max	Unit
Supply Voltage	V_{DD} and V_{DDIO}	-0.3	4.25	V
Voltage at any pad	V_{pad}	GND-0.3	V_{DDIO}+0.3	V
Storage Temperature range		-50	+150	°C
EEPROM write cycles	Same Byte	1000		cycles
EEPROM retention	At 55°C, after 1000 cycles	10		years
Mechanical Shock	Duration ≤ 100µs		10,000	g
	Duration ≤ 1.0ms		2,000	g
	Free fall onto hard surfaces		1.5	m
ESD	HBM, at any pin		2	kV
	CDM		500	V

Note:
Stress above these limits may cause damage to the device. Exceeding the specified electrical limits may affect the device reliability or cause malfunction.

3. Global memory map

The global memory map of BMA150 has three levels of access:

Table 3: Three levels of access

Memory Region	Content	Access Level
Operational Registers	Data registers, control registers, status registers, interrupt settings	Direct access via serial interface
Default Setting Registers	Default values for operational registers, acceleration and temperature trimming values	Access blocked by default; Access enabled by setting control bit in operational registers via serial interface
Bosch Sensortec Reserved Registers	Internal trimming registers	Protected

The memory of BMA150 is realized in diverse physical architectures. Basically BMA150 uses volatile memory registers to operate. The volatile part of the memory can be changed and read quickly. Part of the volatile memory ("image") is a copy of the non-volatile memory (EEPROM).

The EEPROM can be used to set default values for the operation of the sensor IC. The EEPROM is write only. The register values are copied to the image registers after power on or soft reset. The download of all EEPROM bytes to image registers is also done when the content of one EEPROM byte has been changed by a write command.

All operational and default setting registers are accessible through serial interface with a standard protocol:

Table 4: Standard protocol

Type of Register	Function of Register	Command	Volatile / non-volatile
Data Registers	– Chip identification, chip version – Acceleration data, temperature	Read Read	non-volatile (hard coded) volatile
Control Registers	– Activating self test, soft reset, switch to sleep mode etc.	Read / Write	volatile
Status Registers	– Interrupt status and self test status – Customer usable status bytes	Read Read / Write	volatile volatile
Setting Register	– Functional settings (range, bandwidth) – Interrupt settings	Read / Write Read / Write	volatile volatile
EEPROM	– Default settings of functional and interrupt settings – Trimming values – Customer reserved data storage – Bosch Sensortec Reserved Memory	Write Write Write Write	non-volatile non-volatile non-volatile non-volatile

Memory Region	Register Address (hexadecimal)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	type	Default setting	
Bosch Sensortec Reserved Registers	50h to 7Fh									BST reserved	NA	
	43h to 49h									not used	NA	
	42h									BST reserved	NA	EEPROM
	41h									BST reserved	NA	
	40h									BST reserved	NA	
	3Fh									BST reserved	NA	
	3Eh									BST reserved	NA	
Default Setting Registers	3Dh	offset_T (msb)								trimming	NA	
	3Ch	offset_z (msb)								trimming	NA	
	3Bh	offset_y (msb)								trimming	NA	
	3Ah	offset_x (msb)								trimming	NA	
	39h	offset_T (lsb)		gain_T						trimming	NA	
	38h	offset_z (lsb)		gain_z						trimming	NA	
	37h	offset_y (lsb)		gain_y						trimming	NA	
	36h	offset_x (lsb)		gain_x						trimming	NA	
	35h	SPI4	enable_adv_INT	new_data_INT	latch_INT	shadow_dis	wake_up_pause		wake_up	control	1 0 0 0 0 0 0 0b	
	34h	reserved			range<1:0>		bandwidth<2:0>			control	xxx 01 110b	
	33h	customer_reserved 2 <7:0>								status	13	
	32h	customer_reserved 1 <7:0>								status	162	
	31h	any_motion_dur		HG_hyst<2:0>			LG_hyst<2:0>			settings	00 000 000b	
	30h	any_motion_thres<7:0>								settings	0	
	2Fh	HG_dur<7:0>								settings	150	
	2Eh	HG_thres<7:0>								settings	160	
	2Dh	LG_dur<7:0>								settings	150	
	2Ch	LG_thres<7:0>								settings	20	
	2Bh	alert	any_motion	counter_HG		counter_LG		enable_HG	enable_LG	control	0 0 00 00 1 1b	
	24h to 2Ah									not used	NA	
	23h									BST reserved	NA	
	22h									BST reserved	NA	
	21h									BST reserved	NA	
	20h									BST reserved	NA	Image
	1FH									BST reserved	NA	
	1Eh									BST reserved	NA	
	1Dh	offset_T								trimming	NA	
	1Ch	offset_z								trimming	NA	
	1Bh	offset_y								trimming	NA	
	1Ah	offset_x								trimming	NA	
	19h	offset_T		gain_T						trimming	NA	
	18h	offset_z		gain_z						trimming	NA	
	17h	offset_y		gain_y						trimming	NA	
	16h	offset_x		gain_x						trimming	NA	
Operational Registers	15h	SPI4	enable_adv_INT	new_data_INT	latch_INT	shadow_dis	wake_up_pause		wake_up	control	1 0 0 0 0 0 0 0b	
	14h	reserved			range<1:0>		bandwidth<2:0>			control	xxx 01 110b	
	13h	customer_reserved 2 <7:0>								status	13	
	12h	customer_reserved 1 <7:0>								status	162	
	11h	any_motion_dur		HG_hyst<2:0>			LG_hyst<2:0>			settings	00 000 000b	
	10h	any_motion_thres<7:0>								settings	0	
	0Fh	HG_dur<7:0>								settings	150	
	0Eh	HG_thres<7:0>								settings	160	
	0Dh	LG_dur<7:0>								settings	150	
	0Ch	LG_thres<7:0>								settings	20	
	0Bh	alert	any_motion	counter_HG		counter_LG		enable_HG	enable_LG	control	0 0 00 00 1 1b	
	0Ah	reserved	reset_INT	update_image	ee_w	self_test_1	self_test_0	soft_reset	sleep	control	x 0 0 0 0 0 0 0b	
	09h	st_result	not used		alert_phase	LG_latched	HG_latched	status_LG	status_HG	status	NA	
	08h	temp<7:0>								data	NA	
	07h	acc_z<9:2> (msb)								data	NA	
	06h	acc_z<1:0> (lsb)		unused					new_data_z	data	NA	
	05h	acc_y<9:2> (msb)								data	NA	
	04h	acc_y<1:0> (lsb)		unused					new_data_y	data	NA	
	03h	acc_x<9:2> (msb)								data	NA	
	02h	acc_x<1:0> (lsb)		unused					new_data_x	data	NA	
	01h	al_version<3:0>				ml_version<3:0>				data	NA	
	00h	unused					chip_id<2:0>			data	----- 010b	

Figure 1: Global memory map of BMA150

Important notes:

1) Bits 5, 6 and 7 of register addresses 14h and 34h do contain critical sensor individual calibration data which must not be changed or deleted by any means.

In order to properly modify addresses 14h and/or 34h for range and/or bandwidth selection using bits 0, 1, 2, 3 and 4, it is highly recommended to read-out the complete byte, perform bit-slicing and write back the complete byte with unchanged bits 5, 6 and 7.

Otherwise the reported acceleration data may show incorrect results.

2) Bit 7 of register 0Ah should be left at a value of “0”.

3) A minimum pause of 14msec. between two consecutive EEPROM write-cycles must be kept.

3.1 Operational registers

3.1.1 SPI4

The SPI4 bit ((address 15h, bit 7) is used to select the correct SPI protocol (three-wire or four-wire, SPI-mode 3). The default value stored in the non-volatile part of the memory is SPI4=1 (four-wire SPI is default value !). After power on reset or soft reset or writing to EEPROM the SPI4 EEPROM setting (35h) is downloaded to the image register SPI4 and the corresponding SPI protocol is selected.
If the desired SPI is three-wire, the microcontroller must first write SPI4 to 0 (in image register only or in EEPROM). This first writing is possible because only CSB, SCK and SDI are required for a write sequence and the 3 bit timing diagrams are identical in three-wire and four-wire configuration.
Since EEPROM has limited write cycle lifetime (minimum 1000 cycles specified) it is recommended to use one of the following procedures.

Procedure 1 (recommended): Set SPI4 in image to correct value (SPI4=0 for SPI three-wire, SPI4=1 for SPI four-wire (=default)) every time after power on reset, soft reset or EEPROM write command.

Procedure 2: Verify chip-ID (address 00h) after every power on reset, soft reset or EEPROM write command to be chip_ID=02h. If chip_ID=FFh or chip_ID=00h unlock EEPROM (section 3.3.3) and set SPI4 to correct interface in EEPROM at 35h. Lock EEPROM. Optionally verify chip_ID after delay of >30ms.

Procedure 3: Set SPI4 once to correct interface in the EEPROM at 35h during final test procedure at customer.

3.1.2 Range

These two bits (address 14h, bits 4 and 3) are used to select the full scale acceleration range. Directly after changing the full scale range it takes 1/(2*bandwidth) to overwrite the data registers with filtered data according to the selected bandwidth.

range<1:0>	Full scale acceleration range
00	+/- 2g
01	+/- 4g
10	+/- 8g
11	Not authorised code

Figure 2: Settings of full scale range register

Important note:

Please refer to the comment in chapter 3 of how to protect bits 5, 6 and 7 when modifying other bits of register 14h.

3.1.3 Bandwidth

These three bits (address 14h, bits 2-0) are used to setup the digital filtering of ADC output data to obtain the desired bandwidth. A second order analogue filter defines the max. bandwidth to 1.5kHz. Digital filters can be activated to reduce the bandwidth down to 25Hz in order to reduce signal noise. The digital filters are moving average filters of various length with a refresh rate of 3kHz.

Since the bandwidth is reduced by a digital filter for the factor ½ , ¼, ... of the analogue filter frequency of 1.5kHz the mean values of the bandwidth are slightly deviating from the rounded nominal values. Table 4 shows the corresponding data:

Bandwidth<2:0>	Nominal selected bandwidth [Hz]	Min.	Mean bandwidth[Hz]	Max.
000	25	-10%	23	+10%
001	50		47	
010	100		94	
011	190		188	
100	375		375	
101	750		750	
110	1500		1500	
111	Not authorised code	-	-	-

Figure 3: Settings of bandwidth

At wake-up from sleep mode to normal operation, the bandwidth is set to its maximum value and then reduced to bandwidth setting as soon as enough ADC samples are available to fill the whole digital filter.

Important note:
Please refer to the comment in chapter 3 of how to protect bits 5, 6 and 7 when modifying other bits of register 14h.

3.1.4 Wake_up

This bit (address 15h, bit 0) makes BMA150 automatically switching from sleep mode to normal mode after the delay defined by wake_up_pause (section 3.1.5). When the sensor IC goes from sleep to normal mode, it starts acceleration acquisition and performs interrupt verification (section 3.2). The sensor IC automatically switches back from normal to sleep mode again if no fulfilment of programmed interrupt criteria has been detected. The IC wakes-up for a minimum duration which depends on the number of required valid acceleration data to determine if an interrupt should be generated.
If a latched interrupt is generated, this can be used to wake-up a microprocessor. The sensor IC will wait for a reset_INT command and restart interrupt verification. BMA150 can not go back to sleep mode if reset_INT is not issued after a latched interrupt.
If a not-latched interrupt is generated, the device waits in the normal mode till the interrupt condition disappears. The minimum duration of interrupt activation is 330µs. If no interrupt is generated, the sensor IC goes to sleep mode for a defined time (wake_up_pause).

For more details on the wake-up functionality, please refer to chapter 7.3.

3.1.5 Wake_up_pause

These bits (address 15h, bit 2 and 1) define the sleep phase duration between each automatic wake-up.

wake_up_pause<1:0>	Sleep phase duration
00	20 ms
01	80 ms
10	320 ms
11	2560 ms

Figure 4: Settings of wake_up_pause

Note:
The accuracy of the wake-up timer is about ±30%.

3.1.6 Shadow_dis

BMA150 provides the possibility to block the update of data MSB while LSB are read out. This avoids a potential mixing of LSB and MSB of successive conversion cycles. When this bit (address 15h, bit 3) is at 1, the blocking procedure for MSB is not realized and MSB only reading is possible.

3.2 Interrupt settings

Five different types of interrupts can be programmed. When the corresponding criterion becomes valid, the interrupt pin is triggered to a high level. All interrupt criteria are combined and drive the interrupt pad with an Boolean <OR> condition.

Interrupt generations may be disturbed by changes of EEPROM, image or other control bits because some of these bits influence the interrupt calculation. As a consequence, no write sequence should occur when microprocessor is triggered by interrupt or the interrupt should be deactivated on the microprocessor side when write sequences are operated.

Interrupt criteria are using digital code coming from digital filter output. As a consequence all thresholds are scaled with range selection (section 3.1.3.2). Timings used for high acceleration and low acceleration debouncing are absolute values (1 LSB of HG_dur and LG_dur registers corresponds to 1 millisecond, timiming accuracy is proportional to oscillator accuracy = +/-10%), thus it does not depend on selected bandwidth. Timings used for any motion interrupt and alert detection are proportional to bandwidth settings (section 3.1.3).

3.2.1 Enable_LG

This bit (address 0Bh, bit 0) enables the LG_thres criteria to generate an interrupt.

3.2.2 Enable_HG

This bit (address 0Bh, bit 1) enables the HG_thres criteria to generate an interrupt.

3.2.3 Enable_adv_INT

This bit (address 15h, bit 6) is used to disable advanced interrupt control bits (any_motion, alert). If enable_adv_INT=0, writing to these bits has no effect on sensor IC function.

3.2.4 Any_motion

This bit (address 0Bh, bit 6) enables the any motion criteria to generate directly an interrupt. It can not be turned on simultaneously with alert. This bit can be masked by enable_ adv_INT, the value of this bit is ignored when enable_adv_INT=0 (section 3.2.3).

3.2.5 Alert

If this bit (address 0Bh, bit 7) is at 1, the any_motion criterion will set BMA150 into alert mode (section 3.2.9). This bit can be masked by enable_adv_INT, the value of this bit is ignored when enable_adv_INT=0 (section 3.2.3).

3.2.6 Latch_INT

If this bit (address 15h, bit 4) is at 1, interrupts are latched. The INT pad stays high until microprocessor detects it and writes reset_INT control bit to 1 (section 3.3.1). When this bit is at 0, interrupts are set and reset directly by BMA150 according to programmable criteria (sections 3.2.7 and 3.2.8).

3.2.7 LG_thres, LG_hyst, LG_dur, counter_LG

LG_thres (address 0C, bits 7-0 / low-g threshold) and LG_hyst (address 11h, bits 2-0 / low-g threshold hysteresis) are used to detect a free fall. The threshold and duration codes define one criterion for interrupt generation when absolute value of acceleration is low for long enough duration.

Data format is unsigned integer.

LG_thres criterion_x is true if $|acc\_x| \leq$ LG_thres / 255 * range

LG_thres interrupt is set if (LG_thres criterion_x AND LG_thres criterion_y AND LG_thres criterion_z) AND interrupt counter = (LG_dur+1)

LG_thres criterion_x is false if $|acc\_x| >$ (LG_thres + 32*LG_hyst) / 255 * range

LG_thres interrupt is reset if NOT(LG_thres criterion_x AND LG_thres criterion_y AND LG_thres criterion_z)

LG_thres and LG_hyst codes must be chosen to have (LG_thres + 32*LG_hyst) < 511.

When LG_thres criterion becomes active, an interrupt counter is incremented by 1 LSB/ms. When the low-g interrupt counter value equals (LG_dur+1), an interrupt is generated.
Depending on counter_LG (address 0Bh, bit 3 and 2) register, the counter could also be reset or count down when LG_thres criterion is false.

counter_LG<1:0>	**low acceleration interrupt counter status when LG_thres criteria is false**
00	reset
01	Count down by 1 LSB/ms
10	Count down by 2 LSB/ms
11	Count down by 3 LSB/ms

Figure 5: Description of debouncing counter counter_LG

If latch_INT=0, the interrupt is not a latched interrupt and then it is reset as soon as LG_thres criteria becomes false. When interrupt occurs, the interrupt counter is reset.

The LG_thres criteria is set with an AND condition on all three axes to be used for free fall detection.

3.2.8 HG_thres, HG_hyst, HG_dur, counter_HG

HG_thres (address 0Eh, bits 7-0 / high-g threshold) and HG_hyst (address 11h, bits 5-3 / high-g threshold hysteresis) define the high-G level and its associated hysteresis. HG_dur (high-g threshold qualification duration) and counter_HG (address 0Bh, bits 5 and 4 / high-g counter down register) are used for debouncing the high-g criteria.
Threshold and duration codes define a criterion for interrupt generation when absolute value of acceleration is high for long enough duration.

The data format is unsigned integer.

HG_threshold criterion_x is true if	|acc_x| ≥ HG_thres / 255 * range
HG_threshold interrupt is set if	(HG_thres criterion_x OR HG_thres criterion_y OR HG_thres criterion_z) AND interrupt counter = (HG_dur+1)
HG_threshold criterion_x is false if	|acc_x| < (HG_thres - 32*HG_hyst) / 255 * range
HG_threshold interrupt is reset if	NOT(HG_thres criterion_x OR HG_thres criterion_y OR HG_thres criterion_z)

HG_thres and HG_hyst codes must be chosen to have (HG_thres - 32*HG_hyst) > 0.

When HG_thres criterion becomes active, a counter is incremented by 1 LSB/ms. When the high-g acceleration interrupt counter value equals (HG_dur+1), an interrupt is generated. Depending on counter_HG register value, the counter could also be reset or count down when HG_thres criterion is false.

counter_HG<1:0>	**High acceleration interrupt counter status when HG_thres criterion is false**
00	reset
01	Count down by 1 LSB/ms
10	Count down by 2 LSB/ms
11	Count down by 3 LSB/ms

Figure 6: Description of debouncing counter_HG

If latch_INT=0, the interrupt is not a latched interrupt and then it is reset as soon as HG_thres criterion becomes false. When interrupt occurs, the interrupt counter is reset.

3.2.9 Any_motion_thres, any_motion_dur

For the evaluation using “any motion” criterion successive acceleration data from digital filter output are stored and moving differences for all axes are built. To calculate the difference the acceleration values of all axes at time t0 are compared to values at t0+3/(2*bandwidth). The difference of both values is equal to the difference of two successive moving averages (from three data points).
The differential value is compared to a global critical threshold any_motion_thres (address 10h, bits 7-0). Interrupt can be generated when the absolute value of measured difference is higher than the programmed threshold for long enough duration defined by any_motion_dur (address 11h, bits 7 and 6).

Any_motion_thres and any_motion_dur data are unsigned integer. Any_motion_thres LSB size corresponds to 15.6mg for +/- 2g range and scales with range selection (section 3.1.2).

Any motion criterion is valid if	|acc(t0)-acc(t0+3/(2*bandwidth))| ≥ any_motion_thres.
An interrupt is set if	(any motion criterion_x OR any motion criterion_y OR any motion criterion_z) for any_motion_dur consecutive times.
The any motion interrupt is reset if	NOT(any_motion criterion_x OR any_motion criterion_y OR any_motion criterion_z) for any_motion_dur consecutive times.

any_motion_dur<1:0>	**Number of required consecutive conditions to set or reset the any motion interrupt**
00	1
01	3
10	5
11	7

Figure 7: any_motion_dur settings

Any_motion_dur is used to filter the motion profile and also to define a minimum interrupt duration because the reset condition is also filtered.

Any_motion_thres can be used to generate an any_motion interrupt or to put BMA150 in alert mode to preload the low-g or high-g threshold logic (enables reduction of reaction time in tumbling mode); this is selected by alert bit (section 3.2.5). These two modes (any_motion and alert) can not be turned on simultaneously.

Figure 8: Any motion criterion (middle graph) is determined from digital filter output (upper graph) and depends on bandwidth settings: for example for any_motion_dur=01b and bandwidth=110b (1.5kHz), we have 2*bandwidth=3ksamples/s which leads to reaction for interrupt activation of 3*333μs = 1ms and a minimum any motion interrupt duration of 3*333us = 1ms (see lower graph).
If lower bandwidth is selected i) the digitally filtered values (lower noise) are taken for the verification of the any motion criterion and ii) the time scale to evaluate the criterion is stretched. Thus adjusting the bandwidth, the any motion threshold, the any motion duration as well as the full scale range enables to tailor the sensitivity of the any motion algorithm.

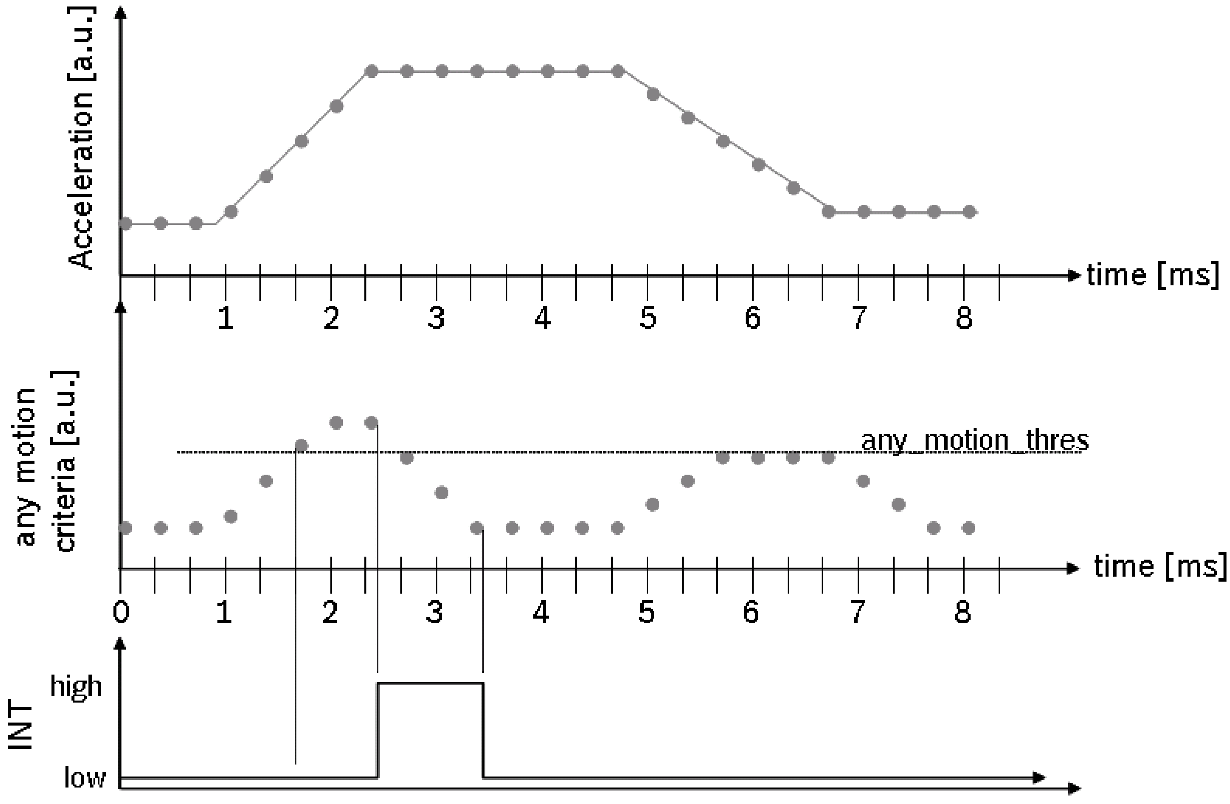

Figure 8: Any motion graph

3.2.10 New_data_int

If this bit (address 15h, bit 5) is set to 1, an interrupt will be generated when all three axes acceleration values are new, i.e. BMA150 updated all acceleration values after latest serial read-out. Interrupt generated from new data detection is a latched one; microcontroller has to write reset_INT at 1 after interrupt has been detected high (section 3.3.1). This interrupt is also reset by any acceleration byte read procedure (read access to address 02h to 07h).
New data interrupt always occurs at the end of the z-axis value update in the output register (3kHz rate). Following figure shows two examples of x-axis read out and the corresponding interrupt generation.

Figure 9: Explanation of new data interrupt.

left side - read out command of x-axis prior to next x-axis conversion
→ new data interrupt after completion of current conversion cycle after z-axis conversion
right side - read out of x-axis send after x-axis conversion
→ new data interrupt at the end of next period when x-axis has been updated

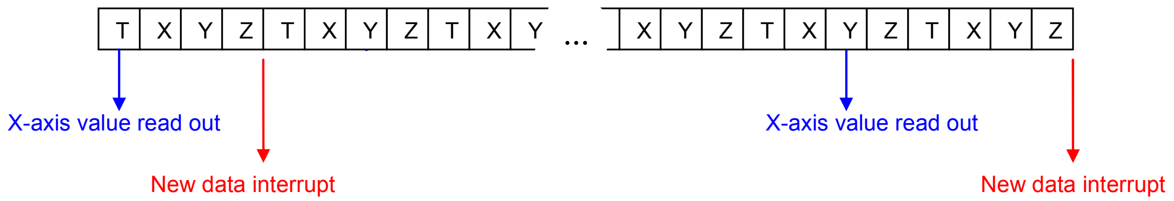

Figure 9: New data interrupt

Please refer to chapter 8.1 for more details.

Note:
When using the I^2C interface for data transfer, the data read out phase can be longer than 330µs (depending on I^2C clock frequency and the amount of data transmitted). Starting a new data read out sequence may lead to the situation that the new_data_int may not be cleared right in time. This must be considered and taken care of properly.

3.3 Control registers

All single control bits are active at 1.

3.3.1 Reset_INT

This interrupt (address 0Ah, bit 6) is reset (interrupt pad goes to low) each time this bit is written to 1.

3.3.2 Update_image

When this bit (address 0Ah, bit 5) is set at 1, an image update procedure is started: all EEPROM content is copied to image registers. The bit update_image is turned at 0 when the procedure is finished. No write or read to image registers and EEPROM write is allowed during their update from EEPROM. An automatic update image procedure also occurs after power on reset and after soft_reset has been written to 1.
The update_image procedure may overwrite the SPI4 setting (section 3.1.1). Thus the correct interface configuration may have to be updated.

3.3.3 Ee_w

ee_w (address 0Ah, bit 4) is used to enable/disable the access to default setting registers.

This bit must first be written to 1 to enable write access to 16h to 3D and to enable read access to 16h to 22h. When this bit is at 0, any access to addresses from 16h to 7Fh has no effect; any read to these addresses set SDO to tri-state (4-wire SPI) or SDI to tri-state (3-wire SPI and I²C). This is valid for all serial interface (I²C, SPI 3-wire or SPI 4-wire).

I²C acknowledgement procedure for access to non-protected or blocked memory regions:

- I²C slave address:	if correct, the BMA150 sets acknowledge.
- I²C register address (I²C write):	The BMA150 sets acknowledge for both unprotected and protected registers.
- I²C write data (I²C write):	The BMA150 sets acknowledge for both unprotected and protected resisters; no write is done for protected register.
- I²C read data (I²C read):	acknowledge is set by master; no error detection is possible; SDI is set to Hi-Z for protected register (0xFF is sent)

After power on reset ee_w=0. So EEPROM and all addresses from 16h to 7Fh can not be directly written or read.

3.3.4 Selftest_0

The self-test command (address 0Ah, bit 2) uses electrostatic forces to move the MEMS common electrode. The result from selftest can be verified by reading st_result (section 3.4.1). During the selftest procedure no external change of the acceleration should be generated.

3.3.5 Selftest_1

This self test bit (address 0Ah, bit3) does not generate any electrostatic force in the MEMS element but is used to verify the interrupt function is working correctly and that microprocessor is able to react to the interrupts.

0g acceleration is emulated at ADC input and the user can detect the whole logic path for interrupt, including the PCB path integrity. The LG_thres register must be set to about 0.4g while LG_dur = 0 to generate a low-g interrupt

3.3.6 Soft_reset

BMA150 is reset each time this bit (address 0Ah, bit 1) is written to 1. The effect is identical to power-on reset. Control, status and image registers are reset to values stored in the EEPROM. After soft_reset or power-on reset BMA150 comes up in normal mode or wake-up mode. It is not possible to boot BMA150 to sleep mode.

No serial transaction should occur within 10µs after soft_reset command.

The soft_reset procedure may overwrite the SPI4 setting (section 3.1.1). Thus the correct interface configuration may have to be updated.

3.3.7 Sleep

This bit (address 0Ah, bit 0) turns the sensor IC in sleep mode. Control and image registers are not cleared.
When BMA150 is in sleep mode no operation can be performed but wake-up the sensor IC by setting sleep=0 or soft_reset. As a consequence all write and read operations are forbidden when the sensor IC is in sleep mode except command used to wake up the device or soft_reset command. After sleep mode removal, it takes 1ms to obtain stable acceleration values (>99% data integrity). User must wait for 10ms before first EEPROM write. For the same reason, BMA150 must not be turned in sleep mode when any update_image, self_test or EEPROM write procedure is ongoing.

3.4 Status registers

3.4.1 St_result

This is the self test result bit (address 09h, bit 7). It can be used together with selftest_0 control bit (section 3.3.4). After selftest_0 has been set, self-test procedure starts. At the end selftest_0 is written to 0 and microcontroller can react by reading st_result bit. When st_result=1 the self test passed successfully.
The result of the st_result can be taken into account to evaluate the basic function of the sensor.
Note: Evaluation of the st_result bit should only be understood as one part of a wider functionality test. It should not be taken into consideration as the only criterion.

3.4.2 Alert_phase

This status bit (address 09h, bit 4) is set when BMA150 has been set to alert mode (section 3.2.5) and an any motion criterion has been detected. During alert phase, HG_dur and LG_dur variables are decreased to have a smaller reaction time when HG_thres and LG_thres thresholds are crossed; the decrease rate is by 1 ms per ms.

The alert mode is reset when an interrupt generated due to a high threshold or a low threshold event or when both HG_dur and LG_dur variables are at 0. When alert is reset, HG_dur and LG_dur variables come back to their original values stored in image registers.

3.4.3 LG_latched, HG_latched

These status bits (address 09h, bit 3 and address 09h, bit 2) are set when the corresponding criteria have been issued. They are latched and thus only the microcontroller can reset them. When both high acceleration and low acceleration thresholds are enabled, these bits can be used by microprocessor to detect which criteria generated the interrupt.

3.4.4 Status_LG, status_HG

These status bits (address 09h, bit 1 and address 09h, bit 0) are set when the corresponding criteria have been issued; they are automatically reset by BMA150 when the criteria disappear.

3.4.5 Customer_reserved 1, customer_reserved 2

Both bytes (address 12h, bit 7-0 and address 13h, bit 7-0) can be used by customer. Writing or reading of these registers has no effect on the sensor IC functionality.
If information has to be stored in a non-volatile memory addresses 32h and 33h have to be used. The write access to EEPROM takes ca. 30ms. Since EEPROM has limited write cycle lifetime special care has to be taken to this issue.

3.5 Data registers

3.5.1 Temp

A thermometer (address 08h, bit 7-0) is embedded in BMA150. Temperature resolution is 0.5°C/LSB. Code 00h stands for lowest temperature which is -30°C. This minimum value can be corrected by trimming of the offset of the temperature sensor IC (not described in this data sheet).

3.5.2 Acc_x, acc_y, acc_z

Acceleration values are stored in the following registers to be read out through serial interface.
acc_x (02h, 7-6; 03h, 7-0)
acc_y (04h, 7-6; 05h, 7-0)
acc_z (06h, 7-6; 07h, 7-0)

The description of the digital signals acc_x, acc_y and acc_z is "2's complement".

From negative to positive accelerations, the following sequence for the ±2g measurement range can be observed (±4g and ±8g correspondingly):

-2.000g	:	10 0000 0000
-1.996g	:	10 0000 0001
...		
-0.004g	:	11 1111 1111
0.000g	:	00 0000 0000
+0.004g	:	00 0000 0001
...		
+1.992g	:	01 1111 1110
+1.996g	:	01 1111 1111

Data is periodically updated (rate 3kHz) with values from the digital filter output. LSB acceleration bytes must be read first. After an acceleration LSB byte read access, the corresponding MSB byte update can optionally be blocked until it is also accessed for read. Thus, MSB / LSB mix from different samples can be avoided (section 3.1.6).
It is not possible to read-out only MSB bytes if shadow_dis=0, an LSB byte must first be read out. To be able to read out only MSB byte, shadow_dis must be written to 1.

new_data_* flags on bits 0 of acc_x (LSB), acc_y (LSB) and acc_z (LSB) can be used to detect if acceleration values have already been read out (section 3.5.3).
If systematic acceleration values read out is planned (for signal processing by the microcontroller), the interrupt pad can be programmed to flag the new data (section 3.2.10). Every time all temperature plus three axes values have been updated, the interrupt goes high and microcontroller can read out data. With this method, microcontroller accesses are synchronized with internal sensor IC updates.

Synchronization of read-out sequence has several advantages:

- it enables a constant phase shift between acceleration conversion and its corresponding digital value read by microprocessor
- it reduces interface communication by avoiding over-sampling.
- potential noise due to serial interface activity perturbation would always be generated during a less critical phase of the conversion cycle. The maximum delay advised to start read out acceleration data is 20µs after INT high (window 0 - 80µs).

3.5.3 New_data_x, new_data_y, new_data_z

These bits (New_data_x (02h, 0), new_data_y (04h, 0), new_data_z (06h, 0)) are flags which are turned at 1 when acceleration registers have been updated. Reading acceleration data MSB or LSB registers turns the flags at 0. The flag value can be read by microprocessor.

3.5.4 Al_version, ml_version, chip_id

chip_id (address 00h, bit 2-0) is used by customer to be able to recognize BMA150. This code is fixed to 010b.

4. Digital interface

BMA150 is capable to be adjusted to customer's specific hardware requirements. It provides three different digital interfaces (SPI 4-wire, SPI 3-wire, I²C) and an interrupt output pin.

The digital interface is used for regular reading of data registers (acceleration and temperature). For a complete read out of acceleration data two successive read cycles are required. The 10 bit coded data word is split into 8 MSB and 2 LSB. The most significant bit (MSB) is transferred first during address and data phases.
The serial interface is also used for verifying status registers or writing to control registers or customized EEPROM programming.

4.1 SPI

The SPI interfaces using three wire or four wire bus provide 16-bit protocols. Multiple read out is possible.
The communication is opened with a read/write control bit (R/W=0 for writing, R/W=1 for reading) followed by 7 address bits and at least 8 data bits (see figure 6 and figure 7). For a complete readout of 10 bit acceleration data from all axes the sensor IC provides the option to use an automatic incremented read command to read more than one byte (multiple read). This is activated when the serial enable pin CSB (chip select) stays active low after the read out of a data register. Thus, read out of data LSB will also cause read out of MSB if the CSB stays low for further 8 cycles of system clock.

The customer has the possibility to communicate with operational registers at addresses 00h-15h via SPI interface (chip identification Bytes, data Bytes, status and control registers with setting parameters). Access to the residual part of the memory map is locked (section 3.3.3). If the master addresses outside the range 00h-15h then SDI will go to tri-state enabling the communication of a second device on the same CSB and SDI line.
The CSB input has an internal 120kΩ pull-up resistor to V_{DDIO}.

4.1.1 4-wire SPI interface

The 4-wire SPI is the default serial interface. The customer can easily activate the 3-wire SPI by writing a control bit (SPI4=0). The 4-wire SPI interface uses SCK (serial clock), CSB (chip select), SDI (serial data in) and SDO (serial data out).

CSB is active low. Data on SDI is latched by BMA150 at SCK rising edge and SDO is changed at SCK falling edge (SPI mode 3). Communication starts when CSB goes to low and stops when CSB goes to high; during these transitions on CSB, SCK must be high. While CSB=1, no SDI change is allowed when SCK=1.

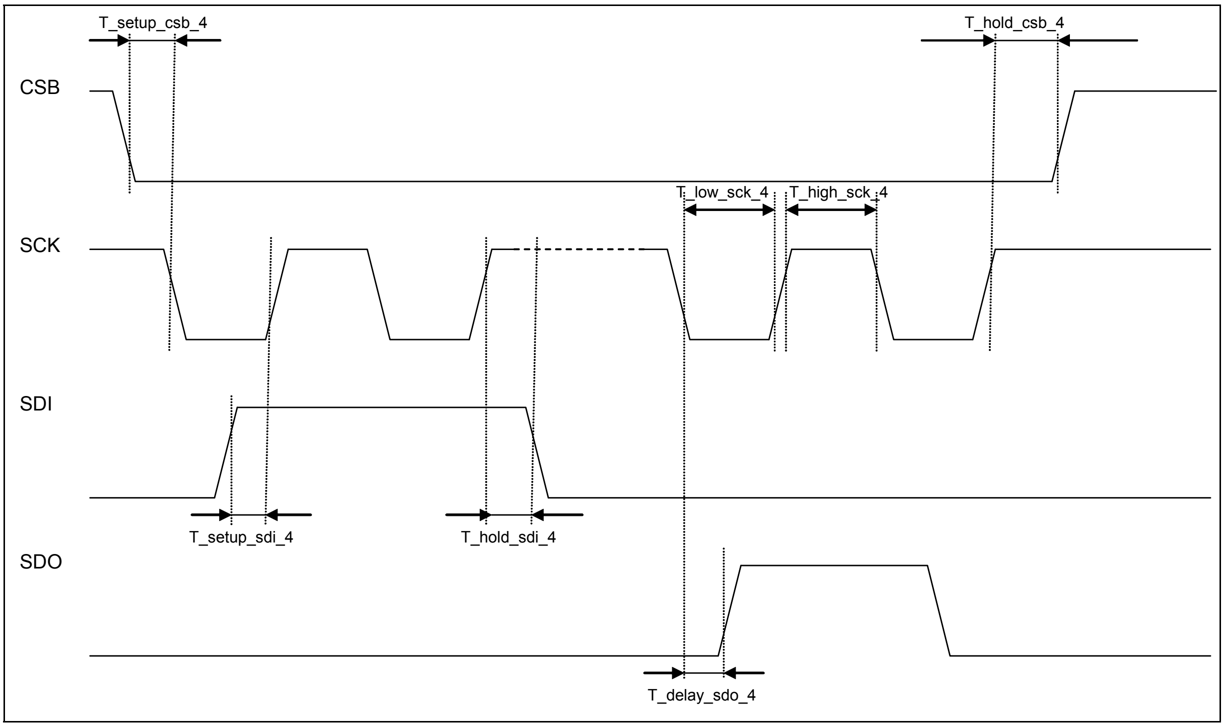

Figure 10: Timing diagram for 4-wire SPI interface

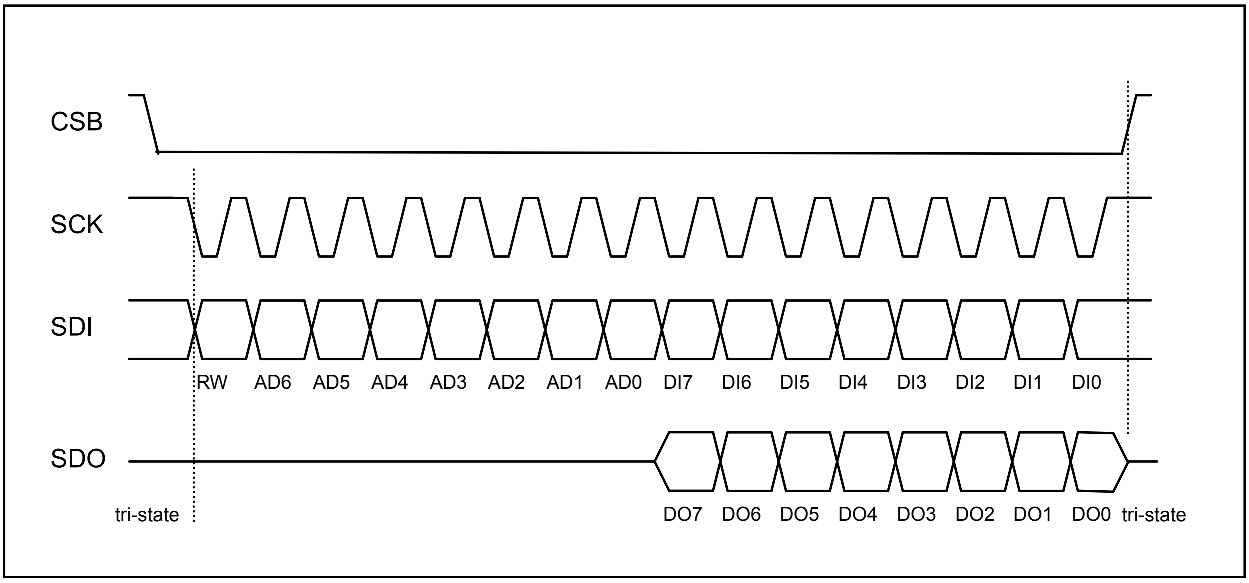

Figure 11: 4-wire SPI bit transfer

Table 5: Specification of 4-wire SPI serial interface

Interface parameters		Conditions	Min.	Typ.	Max.	Unit
Input - low level	Vil_si	V_{DDIO}=1.62V to 3.6V			0.3*V_{DDIO}	V
Input - high level	Vih_si	V_{DDIO}=1.62V to 3.6V	0.7*V_{DDIO}			V
Output – low level	Vol_SDI	V_{DDIO}=1.8V, iol=3 mA			0.4	V
Output – high level	Voh_SDI	V_{DDIO}=1.8V, ioh=1mA	1.4			V
Load capacitor (on SDO)	Csdo_spi	For 10MHz SPI transfer			25	pF
CSB pull-up resistor	CSB_pull_up	Internal pull-up resistance to V_{DDIO}	70	120	190	kΩ
4-WIRE SPI TIMINGS						
SPI clock input frequency	Fspi_4				10	MHz
SCK low pulse	Tlow_sck_4		5			ns
SCK high pulse	Thigh_sck_4		5			ns
SDI setup time	Tsetup_sdi_4		5			ns
SDI hold time	Thold_sdi_4		5			ns
SDO output delay	Tdelay_sdo_4				25	ns
CSB setup time	Tsetup_csb_4		5			ns
CSB hold time	Thold_csb_4		5			ns

	Control byte								Data byte								Control byte								Data byte								
Start	RW	Register adress (16h)							Data register - adress 1Eh								RW	Register adress (0Bh)							Data register - adress 02h								Stop
CSB = 0	0	0	0	1	0	1	1	0	X	X	X	X	X	X	X	X	0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	CSB = 1

Figure 12: When write is required, sequences of 2 bytes are necessary: control byte to define the address to be written and the data byte. 1

	Control byte								Data byte								Data byte								Data byte								
Start	RW	Register adress (02h)							Data register - adress 02h								Data register - adress 03h								Data register - adress 04h								Stop
CSB = 0	1	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CSB = 1

Figure 13: When read access is required, the sequence consists of 1 control byte to define first address to be read followed by data bytes.
Addresses are automatically incremented as long as CSB stays active low.

4.1.2 3-wire SPI interface

3-wire SPI is not the default serial interface. The customer can easily activate the 3-wire SPI by setting a control bit (SPI4=0). The 3-wire SPI interface uses SCK (serial clock), CSB (chip select, active low) and SDA (serial data in/out). A maximum clock frequency up to 70MHz can be handled.

The protocol data acquisition by the sensor IC occurs at the rising edge of SCK. The output data provided by the sensor IC is synchronized also on the rising edges of SCK. The 3-wire read protocol needs one extra clock cycle between address byte and data output byte.

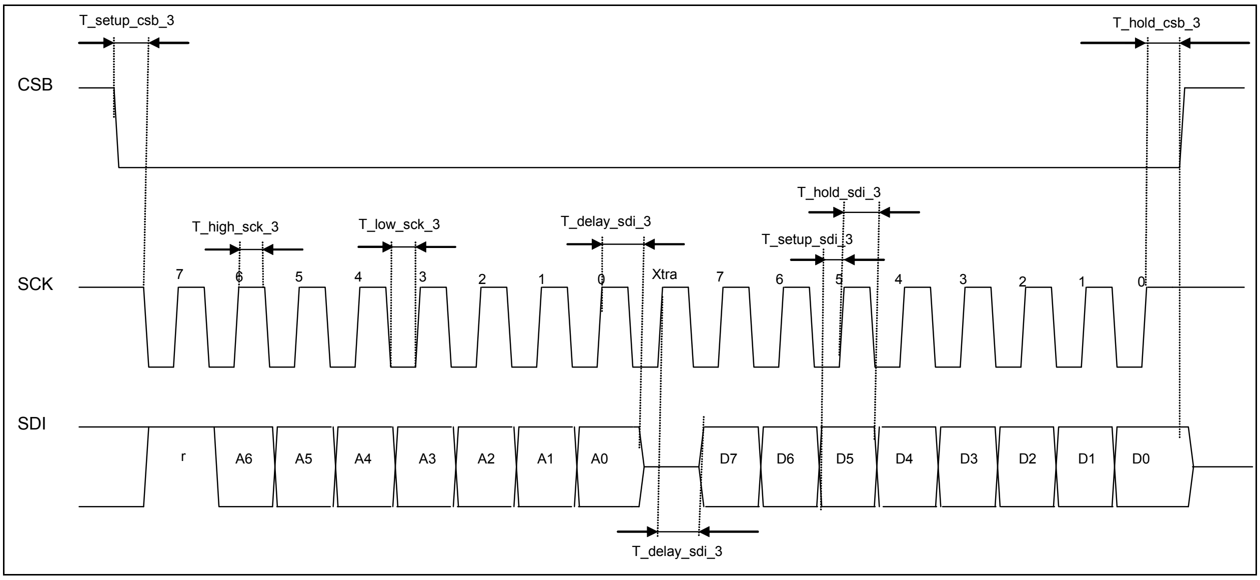

Figure 14: Timing diagram for 3-wire SPI interface (SDI = SDA)

Table 6: Specification of 3-wire SPI serial interface

		Conditions	Min.	Typ.	Max.	Unit
Input - low level	Vil_si	V_{DDIO}=1.62V to 3.6V			0.3*V_{DDIO}	V
Input - high level	Vih_si	V_{DDIO}=1.62V to 3.6V	0.7*V_{DDIO}			V
Output – low level	Vol_SDI	V_{DDIO}=1.8V, iol=3 mA			0.4	V
Output – high level	Voh_SDI	V_{DDIO}=1.8V, ioh=1mA	1.4			V
CSB pull-up resistor	CSB_pull_up	Internal pull-up resistance to V_{DDIO}	70	120	190	kΩ
Load capacitor (on SDO)	Csdo_spi	for 70MHz SPI transfer			10	pF
3-WIRE SPI TIMINGS						
SPI clock input frequency	Fspi_3				70	MHz
SCK low pulse	Tlow_sck_3		5			ns
SCK high pulse	Thigh_sck_3		5			ns
SDI setup time	Tsetup_sdi_3		3.8			ns
SDI hold time	Thold_sdi_3		2			ns
SDI output delay	Tdelay_sdi_3	when SDI is an output for read			10.5	ns
CSB setup time	Tsetup_csb_3		5			ns
CSB hold time	Thold_csb_3		5			ns

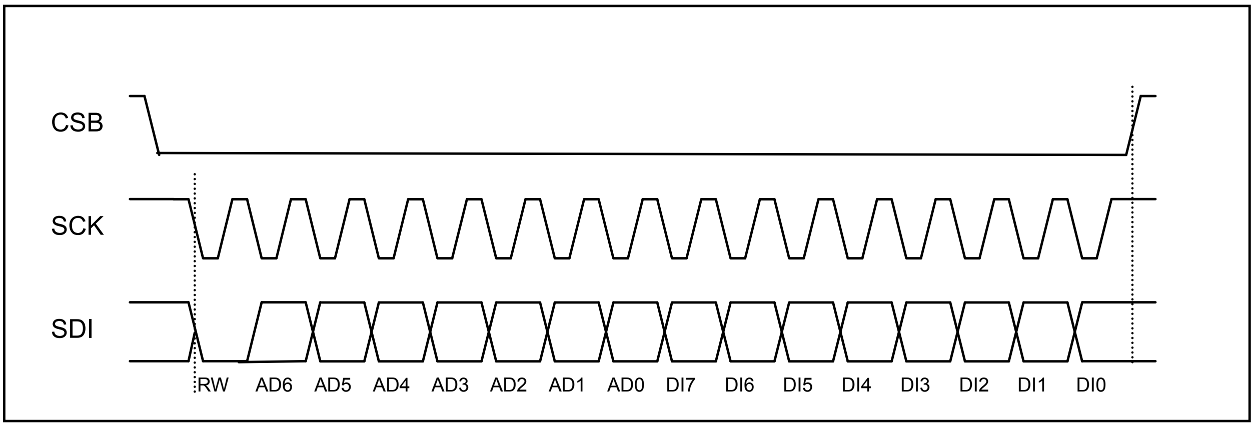

Figure 15: The 3-wire SPI write protocol is identical to four wire bus

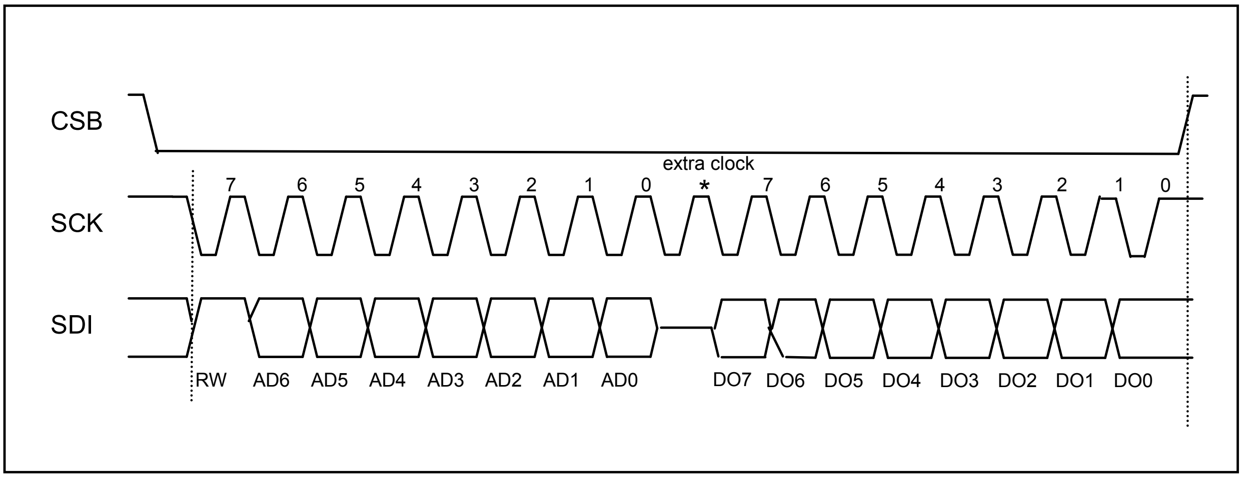

Figure 16: For 4-wire read protocol one extra clock between address byte and data out byte is required. Output data are changed on SDI (SDI=SDA) by SCK rising edge and should be latched by microprocessor during next SCK rising edge.

4.2 I²C interface

The I²C bus uses SCK (serial clock) and SDA (=SDI, serial data input/output). SDA is bi-directional with open drain; it must be connected externally to V_{DDIO} via a pull-up resistor. CSB is not used and must be connected to V_{DDIO}.

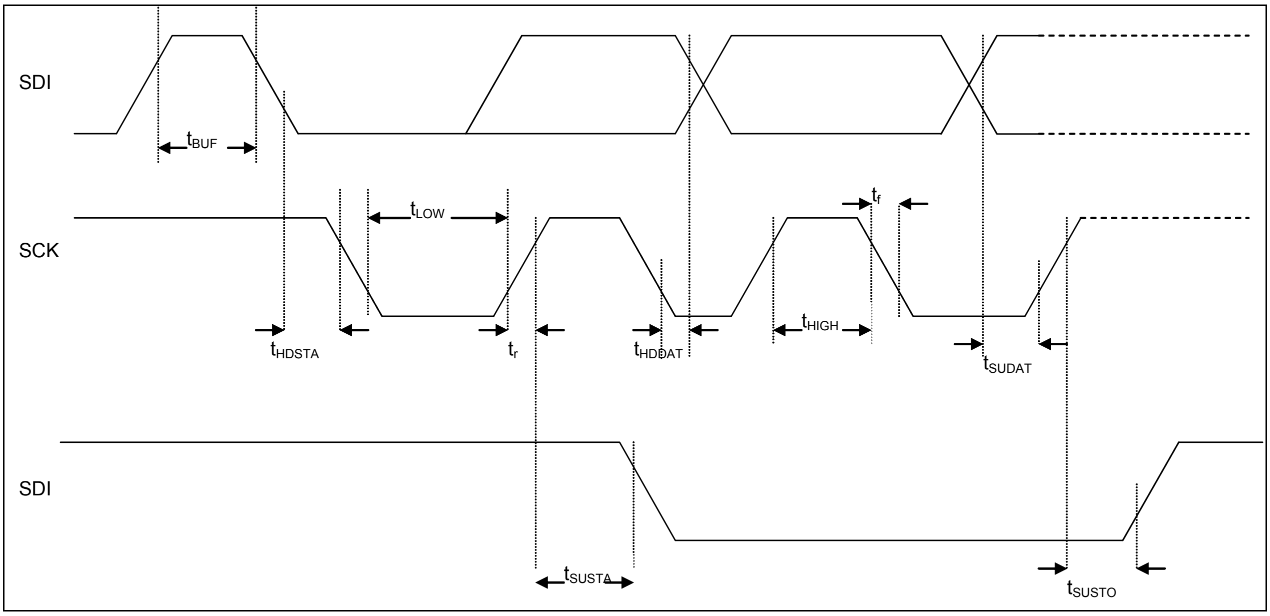

Figure 17: Timing diagram for I²C interface (SDI=SDA)

Table 7: Specification of I²C serial interface (SDI=SDA)

Interface parameters		Conditions	Min.	Typ.	Max.	Unit
Input - low level	Vil_si	V_{DDIO}=1.62V to 3.6V			0.3*V_{DDIO}	V
Input - high level	Vih_si	V_{DDIO}=1.62V to 3.6V	0.7*V_{DDIO}			V
Output – low level	Vol_SDI	V_{DDIO}=1.8V, iol=3 mA			0.4	V
Output – high level	Voh_SDI	V_{DDIO}=1.8V, ioh=1mA	1.4			V
I²C bus load capacitor	Cb	On SDI and SCK			100	pF
I²C TIMINGS						
SCK frequency	FI²C				3.4	MHz
SCK low period	Tlow		160			ns
SCK high period	Thigh		60			ns
SDI setup time	Tsudat		10			ns
SDI hold time	Thddat		0		70	ns
Setup time for a repeated start condition	Tsusta		160			ns
Hold time for a start condition	Thdsta		160			ns
Setup time for a stop condition	Tsusto		160			ns
Time before a new transmission can start	Tbuf		100			ns

Start and stop conditions:
Data transfer begins by a falling edge on SDA when SCK is high (start condition (S) indicated by I²C bus master). Stop condition (P) is a rising edge on SDA when SCK is high (see figure 18).

Bit transfer:
One data bit is transferred during each SCK pulse. Data on SDA line must remain stable during high period of SCK pulse (see figure 19).

Acknowledge:
After start condition each byte of data transfer is followed by an acknowledge bit. The transmitter let the SDA line high (no pull down) and generates a high SCK pulse. If BMA150 has been addressed and data transfer has performed correctly it generates a low SDA level (active pull down). Then SDA line is let free enabling the next transfer (see figure 20).

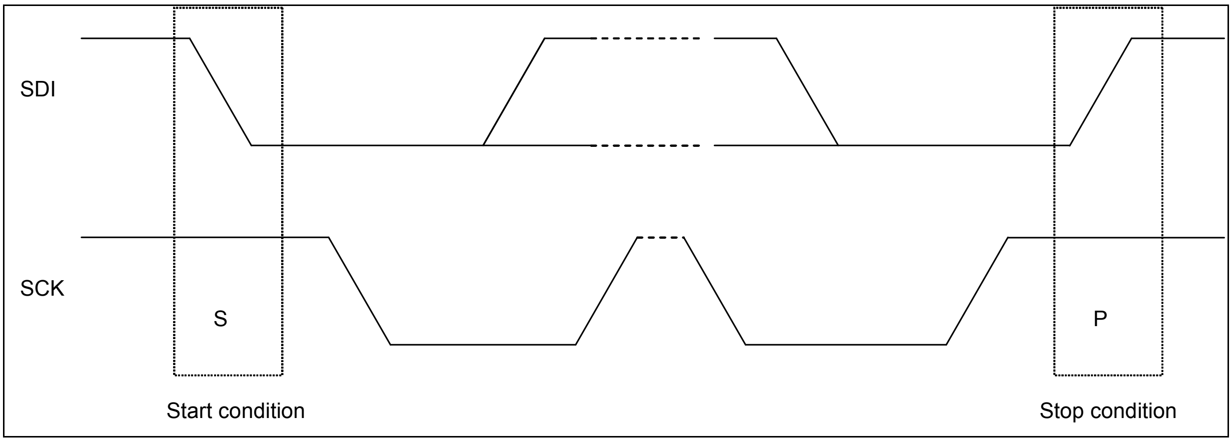

Figure 18: T iming diagram for I²C start and stop condition (SDI=SDA)

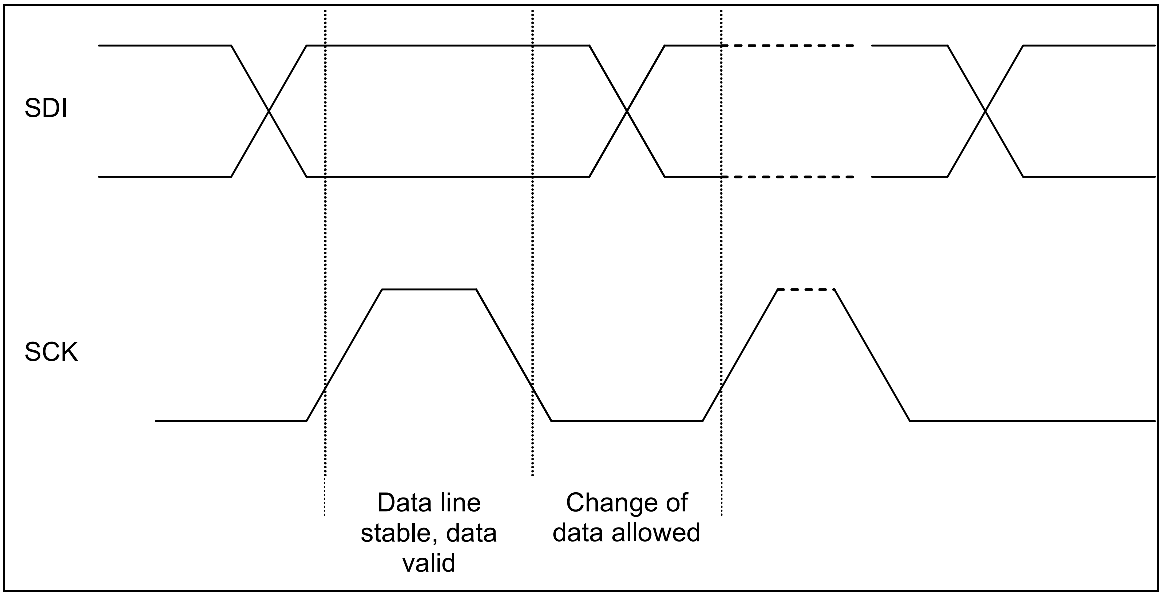

Figure 19: Timing diagram for one bit transfer with I²C interface (SDI=SDA)

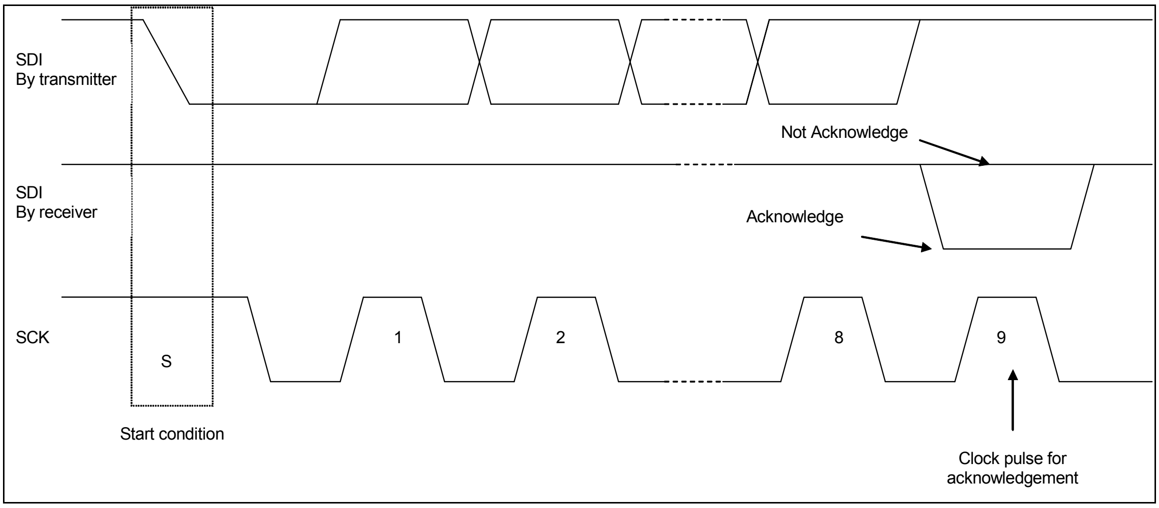

Figure 20: Timing diagram for I²C acknowledgement on SDI (SDI=SDA)

4.2.1 I²C protocol

The BMA150 I²C slave address is coded on 7 bits (0111000b=38h) fixed by a metal option. Thus I²C write address is 01110000b (=70h), read address is 01110001b (=71h).
After a start condition, the slave address + RW bit must be send. If the slave address does not match with BMA150 there is no acknowledgement and the following data transfer will not affect the chip. If the slave address corresponds to BMA150 it will acknowledge (pull SDA down during 9th clock pulse) and data transfer is enabled. The 8th bit RW sets the chip in read or write mode, RW=1 for reading, RW=0 for writing.
After slave address and RW bit, the master sends 1 control byte: the 7-bit register address and one dummy bit.

When BMA150 is accessed in write mode, sequences of 2 bytes (= 1 control byte to define which address will be written and 1 data byte) must be sent:

Figure 21: I²C multiple write protocol

To be able to access registers in read mode, first address has to be send in write mode. Then a stop and a start conditions are issued and data bytes are transferred with automatic address increment:

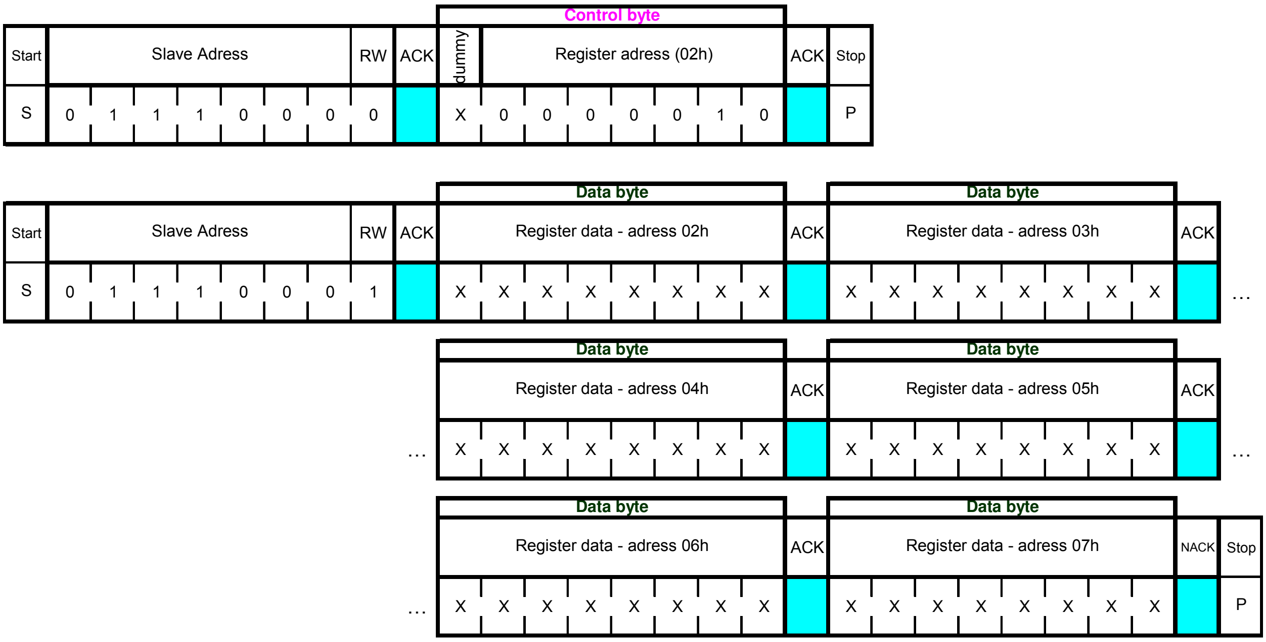

Figure 22: I²C multiple read protocol. Address register is first written to BMA150, the RW=0 (lowest acceleration data located at address 02h). I²C transfer is stopped and restarted with RW=1, address is automatically incremented and the 6 bytes can be sequentially read out.

5. Package

5.1 Outline dimensions

The BMA150 is packaged in a 3mm x 3mm x 0.9mm LGA package following JEDEC MO-229.

Basic outline geometry is based on:

– Mold package footprint	3mm x 3mm (tolerance ±0.1mm)
– Height	0.9mm
– No. of leads	12 - 8 used for electrical connection - 2 not used / reserved - 2 additional metal features on front edges without electrical functionality (not available on first engineering samples)
– Lead pitch	0.5mm

Please note:
In addition to the LGA package, the BMA150 is also available in a QFN-type package, codenamed “SMB380”. The QFN and LGA packages are 100% pin compatible.

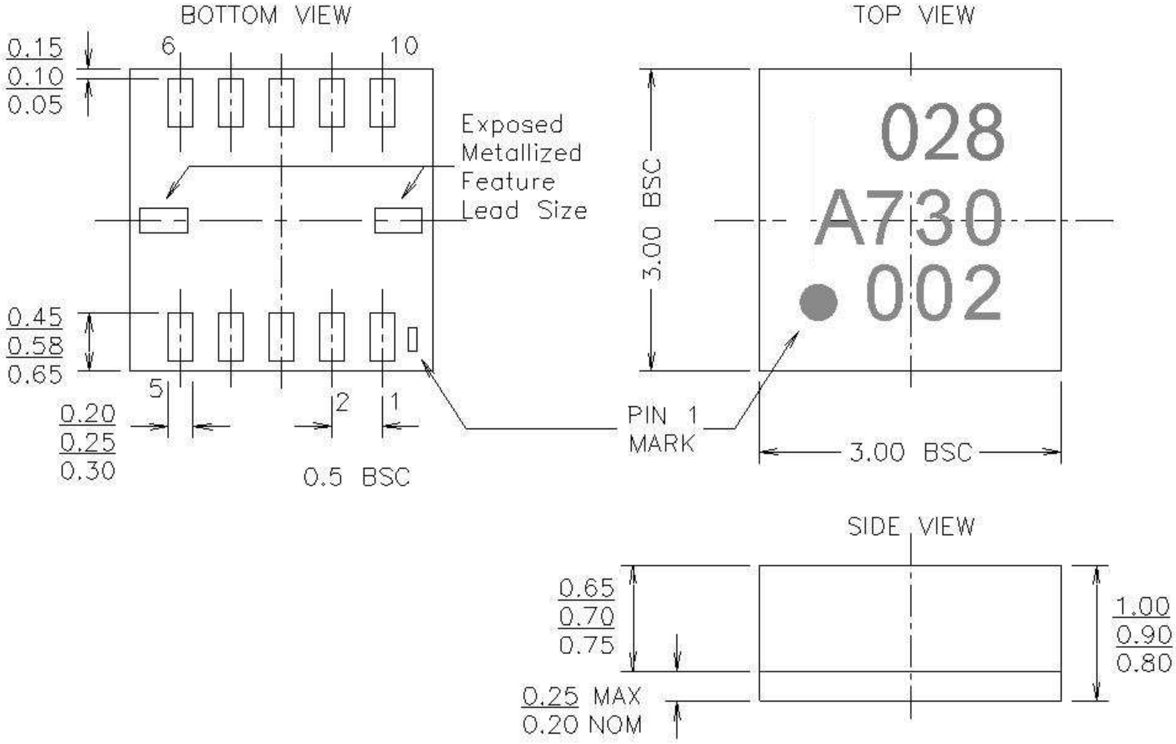

Figure 23: Top, bottom and side views of the 3mm x 3mm x 0.9mm LGA package outline drawing (dimensions in mm)

Note related to figure 23:
For the halogen-free versions of BMA150 (technical reference codes 0 273 141 043 and 0 273 141 081) the number on top of the package marking is “043” or “081”, respectively instead of “028”.

5.2 Axes orientation

The following diagram describes the orientation of the package with respect to the axes of acceleration measurement.

Axes orientation of the BMA150

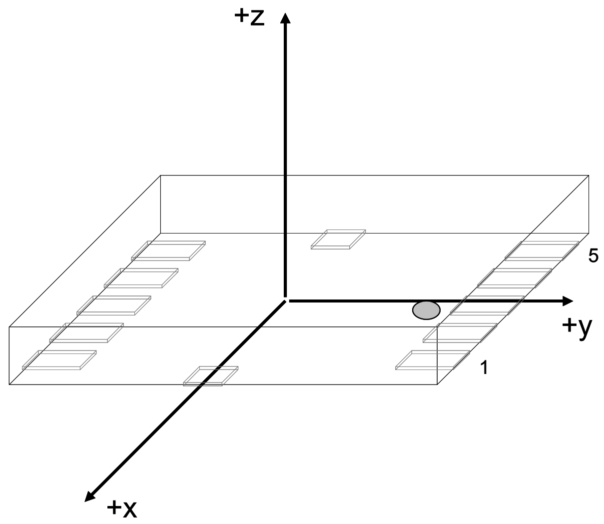

Figure 24: Axes orientation of the BMA150

5.3 Landing pattern recommendations

As for the design of the landing patterns, the following recommendations can be given:

Note:
This information is valid for QFN (SMB380) as well as for LGA packages (BMA150).

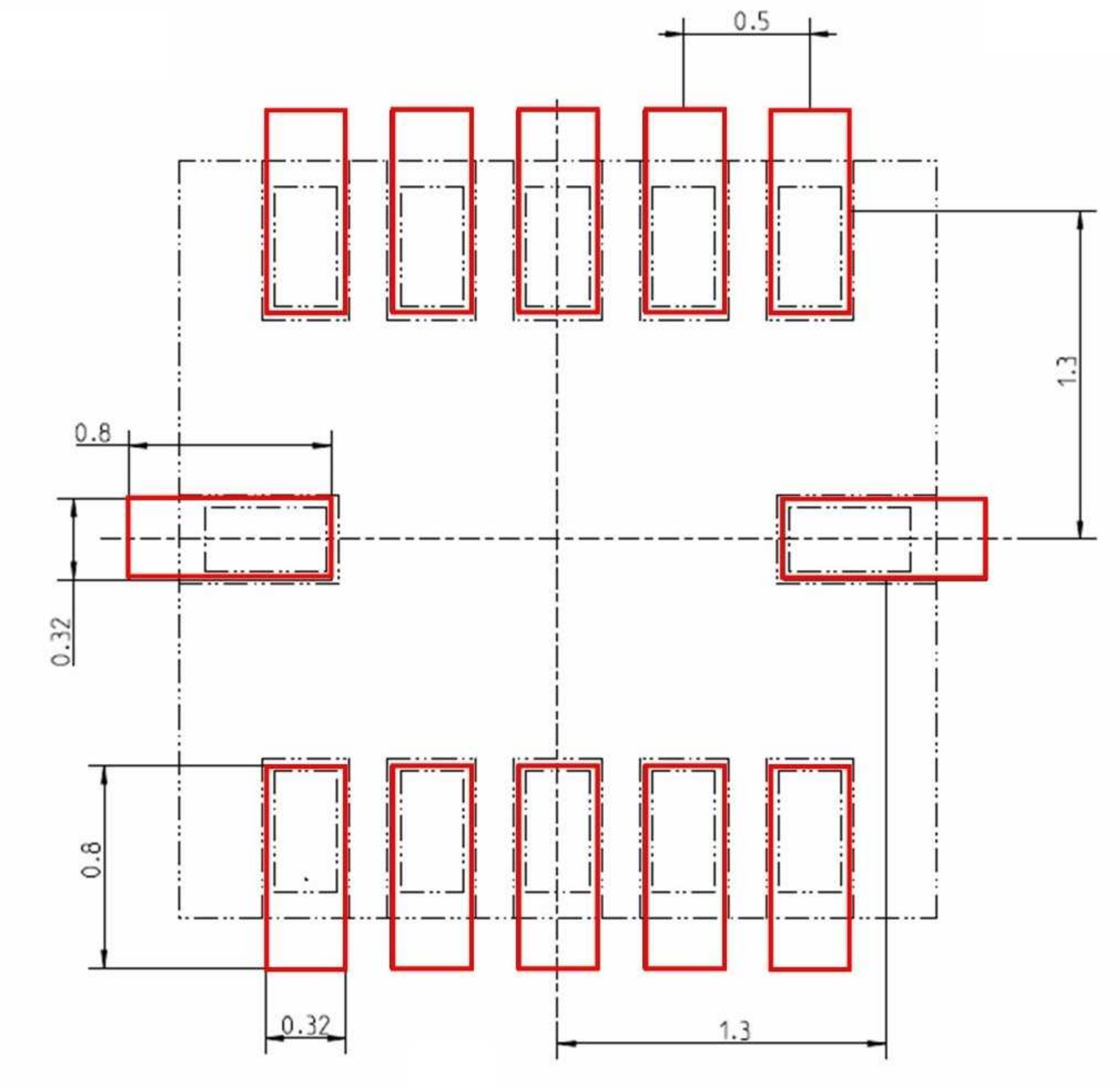

Figure 25: Landing patterns for the BMA150 relative to the device pins, dimensions are in mm

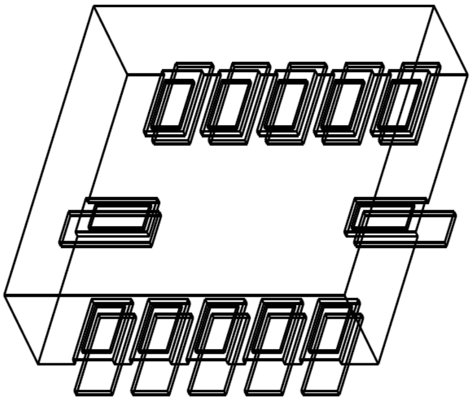

Figure 26: Perspective view of the BMA150 relative to the PCB landing pattern

5.4 Moisture sensitivity level and soldering

The moisture sensitivity level (MSL) of the BMA150 sensor IC corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020C "Joint Industry Standard: Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices"
- IPC/JEDEC J-STD-033A "Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices".

The sensor IC fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e. reflow soldering with a peak temperature up to 260°C.

5.5 RoHS compliancy

The BMA150 sensor IC meets the requirements of the EC restriction of hazardous substances (RoHS) directive, see also
"Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment".

The BMA150 with the technical reference codes 0 273 141 043 and 0 273 141 081 are also halogen free.

5.6 Note on internal package structures

Within the scope of Bosch Sensortec's ambition to improve its products and secure the product supply while in mass production, Bosch Sensortec qualifies additional sources for the LGA package of the BMA150.

While Bosch Sensortec took care that all of the technical package parameters as described above are 100% identical for both sources, there can be differences in the chemical analysis and internal structural between the different package sources.

However, as secured by the extensive product qualification processes of Bosch Sensortec, this has no impact to the usage or to the quality of the BMA150 product.

6. Pin-out and connection diagram

Note: The pin-out schemes of the BMA150 and the SMB380 in QFN package are identical.

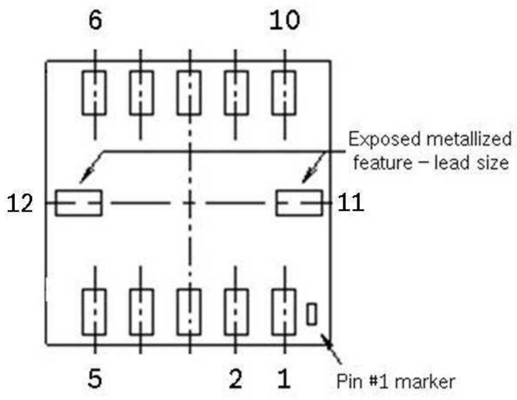

Figure 27: Pin-out of the BMA150 (bottom view)

Table 8: Pin-out description of the BMA150

Pin No	Name	Type	Description	Connect to (in SPI 4w)	Connect to (in SPI 3w)	Connect to (in I²C)	Stand alone (without µC)
1	reserved		Do not connect	NC	NC	NC	NC
2	V_{DD}	Power	Analogue power supply	V_{DD}	V_{DD}	V_{DD}	V_{DD}
3	GND	Power	Ground	GND	GND	GND	GND
4	INT	Output	Interrupt	INT / NC	INT / NC	INT / NC	INT
5	CSB	Input	Chip select	CSB	CSB	V_{DDIO}	V_{DD}
6	SCK	Input	Serial clock	SCK	SCK	SCK	GND
7	SDO	Output	Serial data out	SDO	GND	GND	GND
8	SDI	Input / Output	Serial data in / out	SDI	SDA	SDA	GND
9	V_{DDIO}	Power	Digital interface power supply	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DD}
10	reserved		Do not connect	NC	NC	NC	NC
11	reserved		Do not connect	NC	NC	NC	NC
12	reserved		Do not connect	NC	NC	NC	NC

Recommendation for decoupling: between GND and V_{DD} (pin 1 or 2) a 22nF capacitor and between GND and V_{DDIO} (pin 9) a 100nF capacitor should be connected.

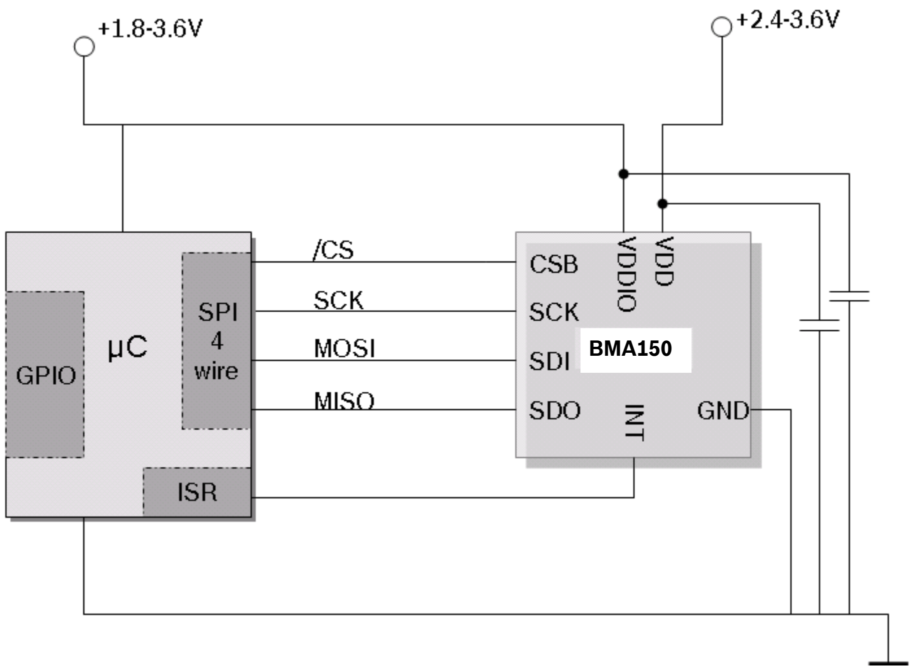

Figure 28: Connection diagram for use with 4-wire SPI interface

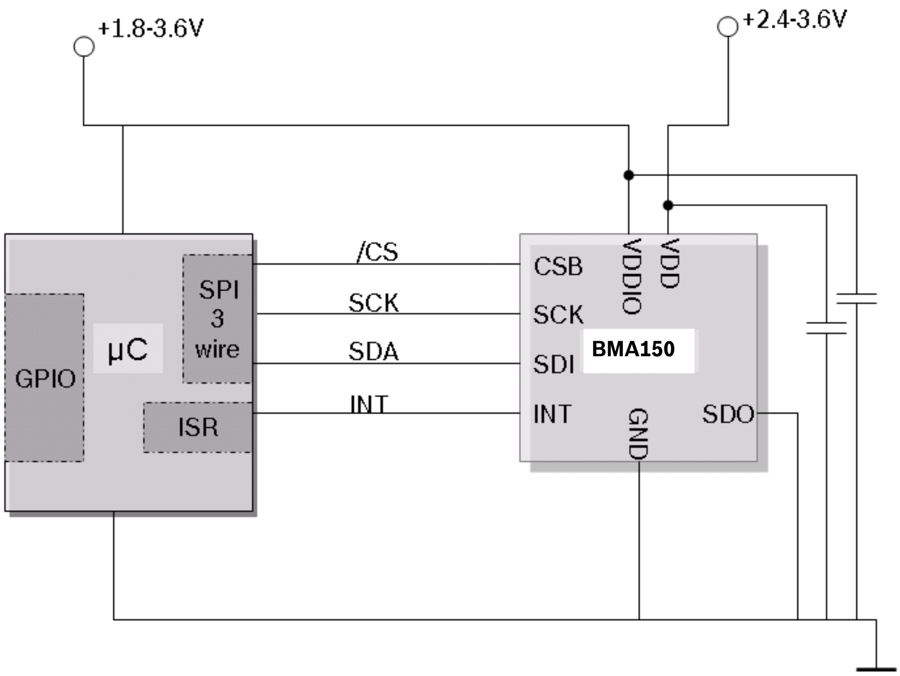

Figure 29: Connection diagram for use with 3-wire SPI interface

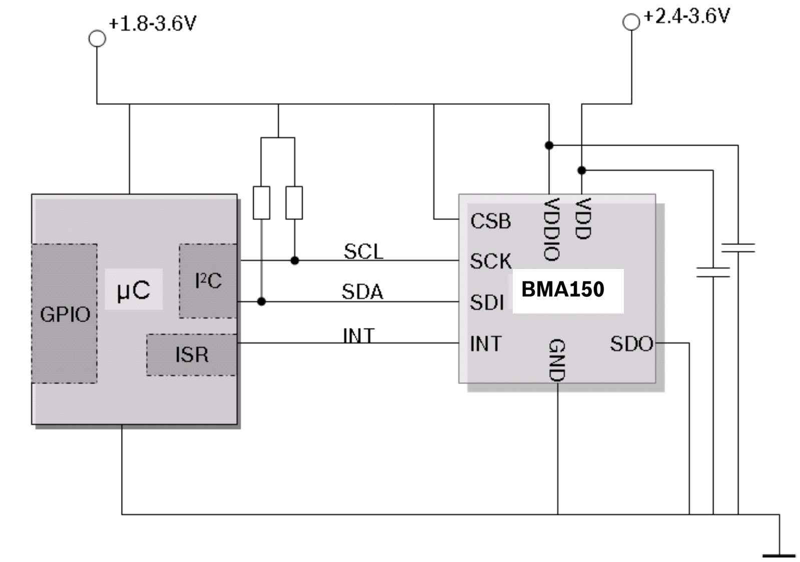

Figure 30: Connection diagram for use with I²C interface

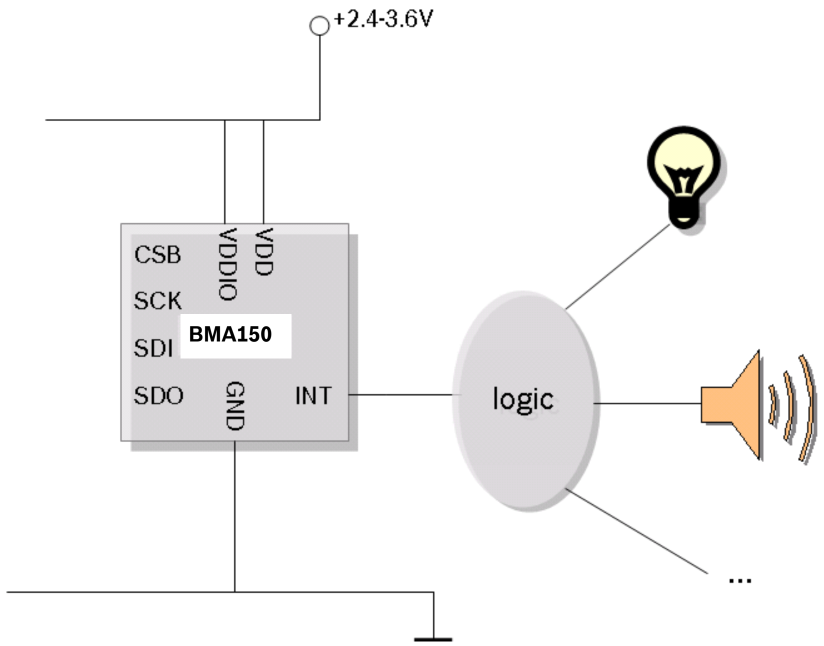

Figure 31: Connection diagram for stand alone use without microcontroller

7. Operation modes

7.1 Normal operational mode

In normal operational mode the sensor IC can be addressed via digital interface. Data and status registers can be read out and control registers and EEPROM values can be read and changed. In parallel to normal operation the user has the option to activate several internal logic paths and set criteria to trigger the interrupt pin. BMA150 is designed to enable low current consumption of 200µA in operational mode.
A self-test procedure can be started in operational mode for testing of the complete signal evaluation path including the micro-machined sensor IC structure, the evaluation ASIC and the physical connection to the host system.

7.2 Sleep mode

Sleep mode is activated by setting a control bit. In sleep mode no communication with the sensor IC is possible – all read and write commands are forbidden. The recommended command to switch to operational mode is the wake-up call.

Wake-up time from sleep to operational mode is 1ms.

In case of a soft-reset, it is recommended to do this reset after having switched from sleep to operational mode. In this case the total typical wake-up and reset time at maximum bandwidth is "switching to operational mode = 1ms" and "time after soft reset until acceleration data is available = 1.3ms", i.e. 2.3ms in total.
In case a soft-reset is activated during sleep mode it can take up to 30ms until normal operation has resumed.

The current consumption in sleep mode is 1µA.

7.3 Wake-up mode

In general BMA150 is attributed to low power applications and can contribute to the system power management.

- Current consumption 200µA operational
- Current consumption 1µA sleep mode
- Wake-up time 1ms
- Start-up time 3ms
- Data ready indicator to reduce unnecessary interface communication
- Wake-up mode to trigger a system wake-up (interrupt output to master) when motion detected
- Low current consumption in wake-up mode

The BMA150 provides the possibility to wake up a system master when specific acceleration values are detected. Therefore the BMA150 stays in an ultra low power mode and periodically evaluates the acceleration data with respect to interrupt criteria defined by the user. An interrupt output can be generated and trigger the system master. The wake-up mode is used for ultra-low power applications where inertial factors can be an indicator to change the activity mode of the system.

The following table shows values calculated for the average current consumption during the wake-up mode of the BMA150. The power consumption in wake-up mode is dependent on the duration of the interrupt algorithm (number of data acquisitions) and the bandwidth (for more details on setting of the bandwidth please refer to chapter 3.1.3).

Table 9: Average current consumption in self wake-up mode using high-g or low-g interrupt

	Current consumption during BMA150 wake-up mode [µA] **(depending on bandwidth, calculated using typical values)**						
Pause [ms]	(@ 1,500Hz)	(@ 750Hz)	(@375Hz)	(@190Hz)	(@100Hz)	(@50Hz)	(@25Hz)
20	16.3	21.8	31.8	48.4	71.6	102.9	134.7
80	5.1	6.6	9.7	15.4	25.0	42.3	68.4
360	1.9	2.3	3.0	4.4	6.9	12.0	21.3
2,560	1.1	1.2	1.3	1.5	1.9	2.6	4.1

Durations of the pause values can vary for about ±30% due to the accuracy of the ultra-low-power oscillator implemented within the sensor.

For estimating the typical current consumption in wake-up mode the following formula can be applied:

i_self_wake_up = (i_DD • t_active + i_DDsbm • wake-up-pause) / (t_active + wake-up-pause)

With the approximation:

t_active = 1ms + 0.333ms • (4 · 750 / bandwidth) + 0.333ms · (1500 / bandwidth) · n

With the following parameters:

i_DD	Current in normal mode
i_DDsm	Current in sleep mode
wake_up_pause	Setting of wake-up pause
n	number of data points in any-motion logic (n=0 for high-g threshold and low-g threshold interrupt, n=3 for any-motion logic)
Bandwidth	Setting of bandwidth (750-25 Hz), for 1500Hz *t_active = 1ms + 0.333ms • (1500/bandwidth) • n*

So, the relevant parameters for power consumption in self-wake up mode are:

- the current consumption in normal mode
- the current consumption in sleep mode
- the self-wake up pause duration
- the bandwidth (ie. length of digital filter to be filled for one data point)
- the interrupt criteria (determines the duration of normal operation):
    - high-g and low-g criteria (ie. acquisition of one data point)
    - any-motion criterion (ie. four data points)

As some of these parameters have certain deviations from the typical value results of various example Monte Carlo Simulations on the current consumption are shown in figures 32, 33 and 34.

The graphs provide an indication on the expected current consumption for different settings.

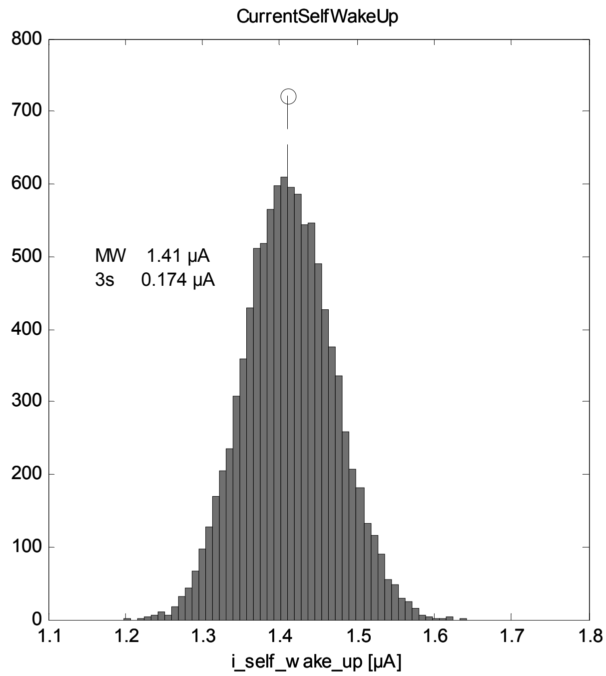

Figure 32: Estimation of current consumption using Monte Carlo simulation, example #1: Bandwidth 750Hz, 2560ms wake-up setting, any-motion interrupt

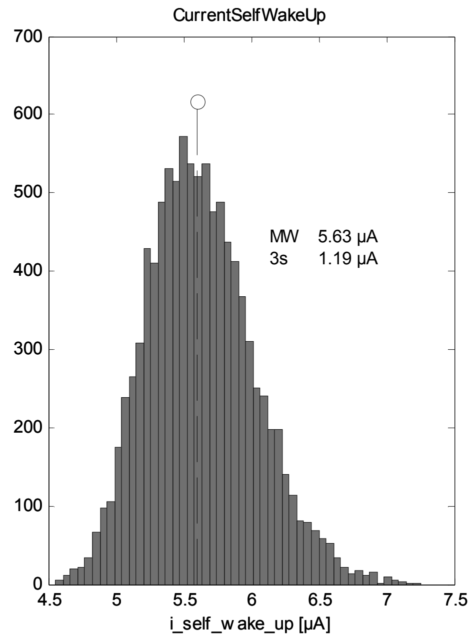

Figure 33: Estimation of current consumption using Monte Carlo simulation, example #2: Bandwidth 47Hz, 2560ms wake-up setting, any-motion interrupt

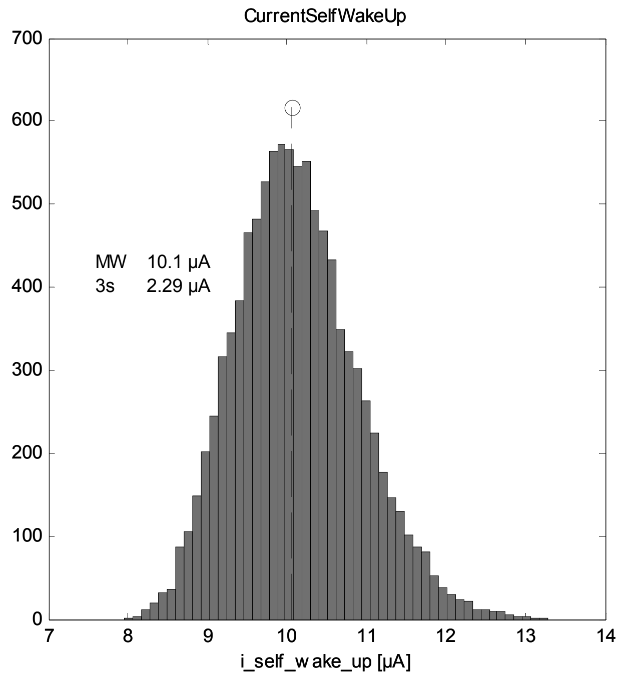

Figure 34: Estimation of current consumption using Monte Carlo simulation, example #3: Bandwidth 23Hz, 2560ms wake-up setting, any-motion interrupt

8. Data conversion

8.1 Acceleration data

Acceleration data are converted by a 10bit ADC. The description of the digital signal is "2's complement". The 10 bit data are available as LSB (at lower register address) and MSB. It is possible to read out MSB only (8 bit) and LSB/MSB (16 bits with 10 data bits and 1 data ready bit) while LSB- and MSB-data are closely linked to avoid unintentional LSB/MSB mixing when read out and data conversion overlap accidentally (section 3.5.2).

The update rate of data registers is 3 kHz, independent of the digital filter. The acceleration data is filtered by a second order analog filter at 1.5 kHz. Additionally the data can be processed by digital averaging filters (moving average) to reduce the noise level (750Hz – 25Hz).
The transfer function of the mechanical element is designed to avoid resonance effects at frequencies below the bandwidth of the ASIC.

The availability of new data can be checked in two ways:

- Bit 0 from the LSB data registers is an indicator whether the data have already been read out or the data are new (Bit0=1) (section 3.5.3).
- The interrupt pin can be configured to indicate new data availability (not possible in parallel to internal interrupt logic). The synchronization of data acquisition and data read out enables the customer to avoid unnecessary interface traffic in order to reduce the system power consumption and the crosstalk between interface communication and data conversion. For a detailed explanation see Figure 9. (section 3.2.10)

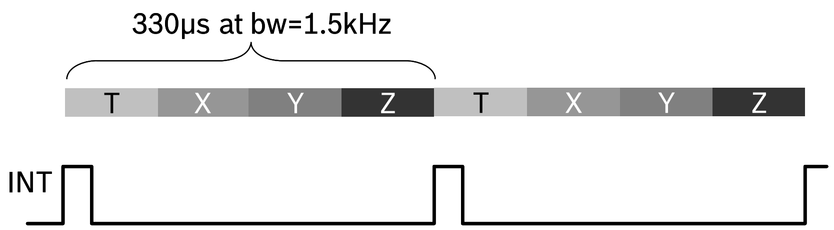

Figure 35: Explanation of data ready interrupt: For a bandwidth of e.g. 1.5 kHz the data refresh cycle takes 330µs to update all data registers. After the final conversion of z-axis the INT pad will be set high. New data can be read out via interface (recommendation: read out within 20µs after interrupt is high during the conversion of the next temperature value). The interrupt resets automatically after read out.

8.2 Temperature measurement

Temperature data are converted to an 8bit data register. The temperature output range can be adapted to customer's requirements by offset correction.

9. Internal logic functions

The sensor IC can inform the host system about specific conditions (e.g. new data ready flag or acceleration thresholds passed) by setting an interrupt pin high even if interface communication is not taking place. This feature can be used as “freefall indicator”, “wake-up” or “data ready flag” for instance.
The interrupt performance can be programmed by means of control bits. Thus the criteria to identify a special event can be tailored to a customer’s application and the sensor IC output can be defined specifically.

9.1 Freefall logic

For freefall detection the absolute value of the acceleration data of all axes are investigated (global criteria). A freefall situation is likely to occur when all axes fall below a lower threshold value (“LG_thres”). The interrupt pin will be raised high if the threshold is passed for a minimum duration. The duration time can be programmed in units of ms (max. 255ms).
The function “Freefall Interrupt” can be switched on/off by a control bit which is located within the image of the non-volatile memory. Thus this functionality can be stored as default setting of the sensor IC (EEPROM) but can also rapidly be changed within the image.
The reset of the freefall interrupt can be accomplished by means of a master reset of the interrupt flag (latched interrupt) or the reset can be triggered by the acceleration signal itself (validation of a programmable “hysteresis”).

See also section 3.2.7.

9.2 High-g logic

For indicating high-g events an upper threshold can be programmed. This logic can also be activated by a control bit. Threshold, duration and reset behaviour can be programmed. The high-g and freefall criteria can be logically combined with an <OR>.

See also section 3.2.8.

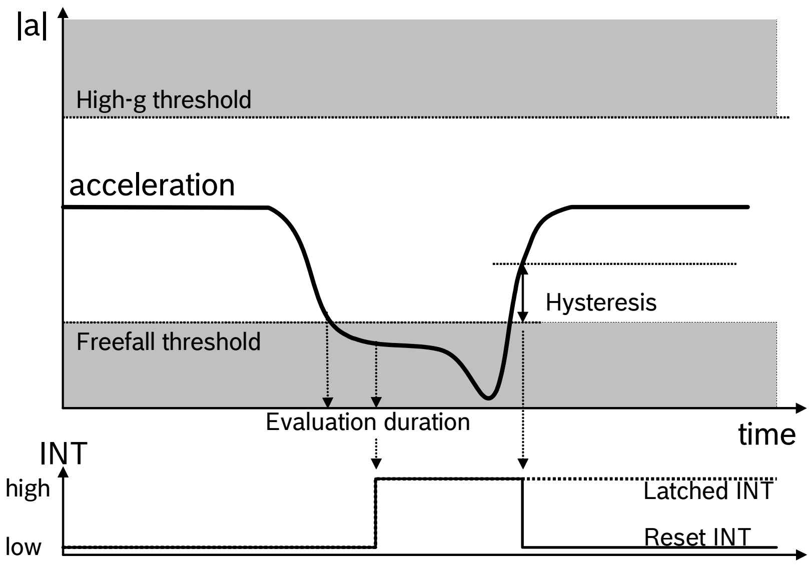

Figure 36: Explanation of freefall and high-g detection. Please see explanation within the text

9.3 Any motion detection

The “any motion algorithm” can be used to detect changes of the acceleration. Thus it provides a relative evaluation of the acceleration signals. The criterion is kind of a gradient threshold of the acceleration over time. Thus one can distinguish between fast events with strong inertial dynamic (e.g. shock), instant changes of force balance (e.g. drop, tumbling) and even slight changes (e.g. touch of a mobile device).
Due to a high bandwidth and a fast response MEMS device the BMA150 is capable to detect shock situations. The “any motion interrupt” or a high-g criterion setting can be used to give a shock alert. The phase shift between onset of mechanical shock and interrupt output is defined by the mechanical transfer function of the chassis and internal mounting interfaces (e.g. PDA shell) and the data output rate of the sensor IC (currently 330µsec, 100µsec under consideration).

See also section 3.2.9.

9.4 Alert Mode

Using the BMA150 it is possible to combine the “any motion criterion” with low-g and high-g interrupt logic to improve the reaction time for e.g. free-fall identification.

See also sections 3.2.9 and 3.4.2.

10. Legal disclaimer

10.1 Engineering samples

Engineering Samples are marked with an asterisk (*) or (e) or (E). Samples may vary from the valid technical specifications of the product series contained in this data sheet. They are therefore not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a product series. Bosch Sensortec assumes no liability for the use of engineering samples. The Purchaser shall indemnify Bosch Sensortec from all claims arising from the use of engineering samples.

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10.3 Application examples and hints

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11. Document history and modification

Rev. No	**Chapter**	**Description of modification/changes**	**Date**
1.0		Document creation	2006-12-29
1.1	1, 4.1.1, 4.1.2, 4.2	Min. V_{DDIO} = 1.62V	2007-05-14
	5.1, 5.2, 5.3	New package diagram, axes vs. package orientation	2007-05-14
	10	Added “e” as marker for engineering samples	2007-05-14
	3	Added warning about overwriting calibration data	2007-05-14
	3.1.2	Corrected typo (correct address 14h)	2007-05-14
	1	Added wake-up and start-up time	2007-05-14
	4.2.1	Corrected slave address in figures 15 and 16	2007-05-14
	1	Zero-g Offset updated to ±60mg	2007-05-21
1.2	1	BMA150 version	2007-07-17
	5.1, 5.3	LGA package (versus QFN package of SMB380)	2007-07-17
1.3	1	Inserted reference to ANA016 application note	2007-10-19
	7.3	Added current consumption values during wake-up mode	2007-10-19
	2	Mechanical shock (10,000g duration)	2007-10-19
	5.5	Halogen content of BMA150	2007-10-19
	3	Extension of global memory map (figure 1)	2007-10-19
	6	Table 12: Do not connect pin 1 and pin 10	2007-10-19
	4.1.1, 4.1.2	Default SPI interface is 4-wire	2007-10-19
	3	Added new note related to register 0Ah	2007-10-19
	3.4.1	Use of self-test result bit	2007-10-19
	5.6	Note on internal package structures	2007-10-19
	6	Added description of pins 11 and 12	2007-10-19
1.4	7.3	Updated current consumption values and added timing data during wake-up mode	2008-01-14
1.5	Title page	Included second, halogen-free part number/order code 0 273 141 043	2008-05-30
	5.1	New package outline drawing with correct product code “028”	2008-05-30
	1	Re-categorized sensitivity min./max. values as indications for reference (±4g/±8g range)	2008-05-30
	1	Inserted max. indication for wake-up time	2008-05-30
	1	Added comment on digital filter	2008-05-30
	3	Minimum pause between EEPROM write cycles	2008-05-30
	3.1.3	Added additional information and data	2008-05-30
	3.1.4	Modified chapter on wake_up	2008-05-30
	3.1.5	Added comment on accuracy of wake-up timer	2008-05-30
	3.2.10	Added comments for “new_data_int”; re-worked figure 3	2008-05-30
	4.2	Modified wording	2008-05-30
	7.2	Modified chapter on sleep mode	2008-05-30
	7.3	Re-worked complete chapter	2008-05-30
1.6	2	Table 2: Added new line “voltage at any pad”	2008-10-30

	4	Figure 5: SDO signal is tri-state	2008-10-30
	5.3	Figure 19: Increased size of the figure	2008-10-30
1.7	All	Introduced additional technical reference code: 0 273 141 081	2010-06-29
	1	Updated link to BST-MAS-AN014-01.pdf	2010-06-29
	1	Added comment on 3-sigma levels	2010-06-29
	3.4.4	Corrected typo: status_HG	2010-06-29
	3.5.4	Update	2010-06-29
	4.2	Corrected typo in table 11, Thddat	2010-06-29
	5.1	Deleted vertical bar on marking picture (figure 17)	2010-06-29

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